AN3979

Implementing Perpetual PoE and Fast PoE

Introduction

This application note describes how to implement Perpetual PoE (PPoE) and Fast PoE with Microchip's PD69210/PD69220 controller with the PD69208T4/PD69204T4/PD69208M Manager or PD39210 controller with the PD39208 Manager.

Perpetual PoE

PPoE supplies uninterrupted power to the connected Power Device (PD) even when the Power Sourcing Equipment (PSE) switch is rebooting.

Fast PoE

Fast PoE stores the last PoE power settings and switches on power when the AC power is plugged in (within a few seconds of switching on the power) without waiting for the host switch to boot up.

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1. Hardware Support

This section describes the hardware requirements to support PPoE and Fast PoE.

1.1 Reset Pin

The Reset pin of the controller must stay high during host reboot. This can be implemented by using a tri-state buffer output from the host and a pull-up resistor to 3.3 V on the controller xRESET pin. The xRESET is pin 26 on the PD69210 and PD39210 and pin 19 on the PD69220.

1.2 Disable Ports Pin

The Disable Ports pin of the controller must stay high during host reboot. This can be implemented by using a tri-state buffer output from the host and a pull-up resistor to 3.3 V on the controller xDISABLE_PORTS pin. xDISABLE_PORTS is pin 4 on PD69210 and PD39210 and pin 31 on PD69220.

If the xDISABLE_PORTS pin is not used, keep it pulled up to 3.3 V.

After the host controller finishes the reboot, it should not reset the PoE system or pull the above signals low.

To support Fast PoE, the above signals must be pulled high immediately after power-up to allow the PoE controller to initialize and start powering ports before the host controller finishes the reboot cycle.

Figure 1-1. Disable Ports Pin Setting—Schematic Diagram
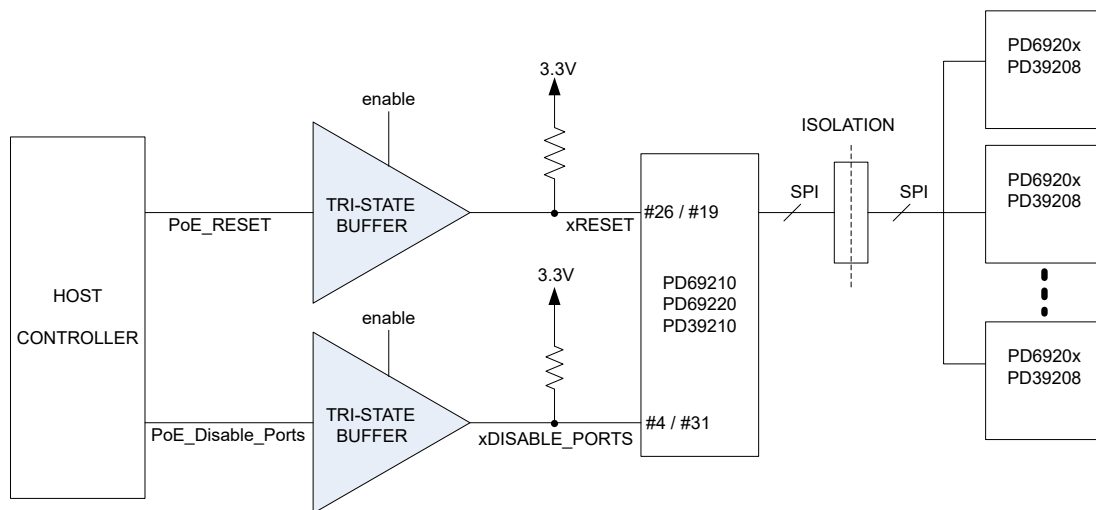
2.   Software Support

This section describes the host software requirements that must be implemented to support PPoE and Fast PoE.

2.1   Power-up and Reboot

The host must distinguish between power-up and reboot. To avoid momentary disconnect of PoE power to the ports, the host must not reconfigure the PoE system parameters if the system reset has not been completed.

The system reset can be achieved by using host indications or utilizing the Private Label field in the PD692x0 communication protocol to detect if the PoE system has experienced a Reset event.

Set the Private Label value by using the Set System Status command for AT or the Set Private Label command for BT, as shown in the following tables.

Table 2-1. Set System Status for at/af Firmware

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x00	##	0x07	0x3D	0x01 to 0xFF	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Command	—	Global	System Status	Private Label	N	N	N	N	N	N	N	N

Table 2-2. Set Private Label for bt Firmware

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x00	##	0x07	0x3D	0x01 to 0xFF	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Command	—	Global	System Status	RAM Private Label	N	N	N	N	N	N	N	N

This command assists in verifying that a reset has occurred.

RAM Private label: The private label value is 0x00 after reset. It is recommended that any value higher than 0x00 is used when the Host wants to use this field.

The Private Label value can be read by using **Get System Status for bt Firmware** request (see Table 2-4).

Use the Get System Status command to generate the Private Label value, as shown in the following tables.

Table 2-3. Get System Status for at/af Firmware

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x02	##	0x07	0x3D	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Request	—	Global	System Status	N	N	N	N	N	N	N	N	N
0x03	##	Val	Val	Val	Val	Val	Val	Val	Val	Val	Val	—
Telemetry	—	CPU Status1	CPU Status2	Factory Default	GIE	Private Label	User Byte	Device Fail	Temp Disco	Temp Alarm	Interrupt Register	—

Table 2-4. Get System Status for bt Firmware

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x02	##	0x07	0xD0	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Request	—	Global	BT System Status	N	N	N	N	N	N	N	N	N
0x03	##	Val	Val	Val	Val	Val	Val	0x4E	0x4E	0x4E	Val
Telemetry	—	0x00	CPU Status2 Error Codes	Factory Default	0x00	RAM Private Label	NVM User Byte	Found Devices	N	N	N	Event Exist

2.2 Flash Memory

To support Fast PoE, the PoE settings must be saved in PD69210/PD69220/PD39210 Flash memory. Next time the system will power-up, the latest configuration settings will immediately be loaded by PD692x0 from the Flash memory. Microchip recommends auto-saving the settings every time the user changes the PoE settings. Another option is to allow the user to save the settings manually by command.

To save the settings in the Flash memory, execute the Save System Settings command, as shown in the following table.

Table 2-5. Save System Setting

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x01	##	0x06	0x0F	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Program	—	E2	SaveConfig	N	N	N	N	N	N	N	N	N

The Save System Settings command saves the current user values into the non-volatile memory. These user values become the default values after each reset.

Use the Restore Factory Defaults command to change the default values to the initial factory values. For instance, if the host sets the power limit to 400 and this value is a default value, then the Save System Settings command must be executed.

Notes:
- After setting this command, the host must not access the MCU controller using I^{2}C or UART for at least 50 ms.
- The Save System Settings command is not supported by PD69200M.

Important Notes:
- After the firmware update, all settings are reset to the factory defaults and must be saved again.
- Based on Microchip's PD69210/PD69220/PD39210, and not PD69200M.

3.   Schematics

For detailed schematics of the PoE system, see application note AN3361.

4.   Revision History

Revision	Date	Description
A	04/2021	Document converted to the Microchip format. Document number changed from PD-000362841 to DS-00003979.
2.0	08/2019	PD69220 support was added.
1.0	04/2019	Initial revision.

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