带有可选展频时钟 (SSC) 的时钟缓冲器/时钟倍乘器

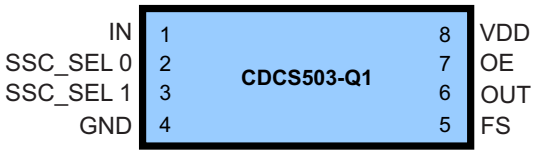
查询样品: CDCS503-Q1

特性

- 符合汽车应用要求
- 具有下列结果的 **AEC-Q100** 测试指南：
  - 器件温度 **2** 级
  - **-40°C** 至 **105°C** 环境温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C3B**
- 带有可选展频时钟 **(SSC)** 的易于使用的时钟生成器产品的一部分
- 带有可选输出频率和可选 **SSC** 的时钟倍乘器
- 通过两个外部引脚可控制 **SSC**
  - **±0%，±0.5%，±1%，±2%** 中心展频
- 可使用一个外部控制引脚来选择 **x1** 或者 **x4** 的频率倍乘
- 通过控制引脚进行输出禁用
- 单一 **3.3V** 器件电源
- 宽温度范围 **-40°C** 至 **105°C**
- 节省空间的 **8** 引脚薄型小外形尺寸 **(TSSOP)** 封装

应用范围

- 要求通过 **SSC** 和/或者时钟倍乘来减少电磁干扰 **(EMI)** 的车载应用



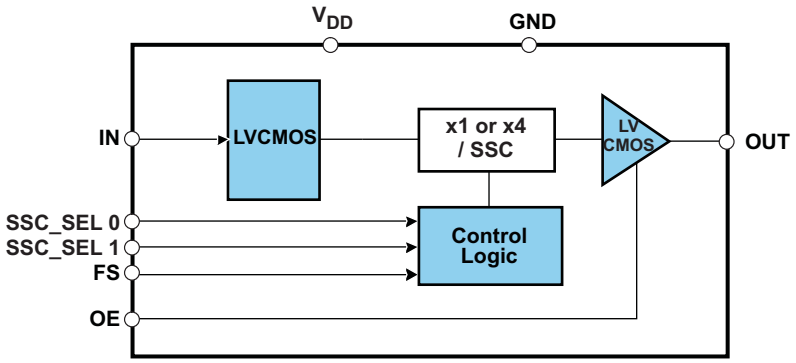


图 **1.** 方框图

说明

CDCS503-Q1 是一款带有可选频率倍乘的可展频、LVCMOS 输入时钟缓冲器。

它与 CDCS502 共用主要的功能性，但是它使用一个 LVCMOS 输入级而不是 CDCS502 所使用的晶振输入级，并且 CDCS503-Q1 有一个输出使能引脚。

此器件在输入上接受一个 3.3V LVCMOS 信号。

这个输入信号由一个锁相环路 (PLL) 处理，此环路的输出频率或者与输入频率相等或者被乘以因子 4。

PLL 还可通过三角调制将时钟信号以输出时钟频率为中心扩展 ±0%，±0.5%，±1% 或者 ±2%。

这样，此器件可生成介于 8MHz 和 108MHz 之间带有或者不带有 SSC 的输出频率。

一个独立的控制引脚可被用于启用或者禁用输出。 CDCS503-Q1 运行在一个 3.3V 环境中。

器件额定运行温度介于 -40°C 至 105°C 之间，并采用 8 引脚 TSSOP 封装。

表 **1.** 功能表

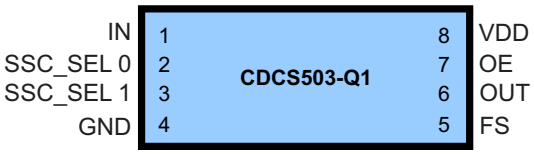
OE	FS	SSC_SEL 0	SSC_SEL 1	SSC 数量	f_{OUT}/f_{IN}	f_{in}=27MHz 时的 f_{OUT}
0	x	x	x	x	x	三态
1	0	0	0	±0.00%	1	27MHz
1	0	0	1	±0.50%	1	27MHz
1	0	1	0	±1.00%	1	27MHz
1	0	1	1	±2.00%	1	27MHz
1	1	0	0	±0.00%	4	108MHz
1	1	0	1	±0.50%	4	108MHz
1	1	1	0	±1.00%	4	108MHz
1	1	1	1	±2.00%	4	108MHz

这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

DEVICE INFORMATION

PACKAGE



PIN FUNCTIONS

SIGNAL	PIN	TYPE	DESCRIPTION
IN	1	I	LVCMOS clock input
OUT	6	O	LVCMOS clock output
SSC_SEL 0, 1	2, 3	I	Spread selection pins, internal pullup
OE	7	I	Output enable, internal pullup
FS	5	I	Frequency multiplication selection, internal pullup
VDD	8	Power	3.3-V power supply
GND	4	Ground	Ground

ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP	2000	CDCS503TPWRQ1	CS503Q

PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE

over operating free-air temperature range (unless otherwise noted)(1)

PW 8-PIN TSSOP			THERMAL AIRFLOW (CFM)				UNIT
			0	150	250	500	
$R_{\theta JA}$	High K		149	142	138	132	°C/W
	Low K		230	185	170	150	
$R_{\theta JC}$	High K	65					°C/W
	Low K	69					

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

THERMAL INFORMATION

THERMAL METRIC(1)		CDCS503TPWRQ1	UNIT
		PW (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	179.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	64.9	
θ_{JB}	Junction-to-board thermal resistance	108.7	
ψ_{JT}	Junction-to-top characterization parameter	9	
ψ_{JB}	Junction-to-board characterization parameter	107	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：SPRA953）。

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 4.6	V
V_{IN}	Input voltage range	–0.5 to 4.6	V
V_{out}	Output voltage range	–0.5 to 4.6	V
I_{IN}	Input current ($V_I < 0$, $V_I > V_{DD}$)	20	mA
I_{out}	Continuous output current	50	mA
T_{ST}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C
ESD Rating	Human-body model (HBM) AEC-Q100 classification level H2	1.5	kV
	Charged-device model (CDM) AEC-Q100 classification level C3B	750	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3		3.6	V
f_{IN}	Input frequency	FS = 0	8		32	MHz
		FS = 1	8		27	
V_{IL}	Low-level input voltage LVCMOS				0.3 V_{DD}	V
V_{IH}	High-level input voltage LVCMOS		0.7 V_{DD}			V
V_I	Input voltage threshold LVCMOS			0.5 V_{DD}		V
C_L	Output load test LVCMOS				15	pF
I_{OH}/I_{OL}	Output current				±12	mA
T_A	Operating free-air temperature		–40		105	°C

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Device supply current	f_{out} = 20 MHz; FS = 0, no SSC		19		mA
		f_{out} = 70 MHz; FS = 1, SSC = 2%		22		
f_{OUT}	Output frequency	FS = 0	8		32	MHz
		FS = 1	32		108	
I_{IH}	LVCMOS input current	$V_I = V_{DD}$; V_{DD} = 3.6 V			10	µA
I_{IL}	LVCMOS input current	V_I = 0 V; V_{DD} = 3.6 V			–10	µA
V_{OH}	LVCMOS high-level output voltage	I_{OH} = - 0.1 mA	2.9			V
		I_{OH} = - 8 mA	2.4			
		I_{OH} = - 12 mA	2.2			
V_{OL}	LVCMOS low-level output voltage	I_{OL} = 0.1 mA			0.1	V
		I_{OL} = 8 mA			0.5	
		I_{OL} = 12 mA			0.8	
I_{OZ}	High-impedance-state output current	OE = Low	–2		2	µA
$t_{JIT(C-C)}$	Cycle to cycle jitter(1)	f_{out} = 108 MHz; FS = 1, SSC = 1%, 10000 Cycles		110		ps
t_r/t_f	Rise and fall time(1)	20%–80%		0.75		ns
O_{dc}	Output duty cycle(2)		45%		55%	
f_{MOD}	Modulation frequency			30		kHz

(1) Measured with Test Load, see Figure 3.
(2) Not production tested.

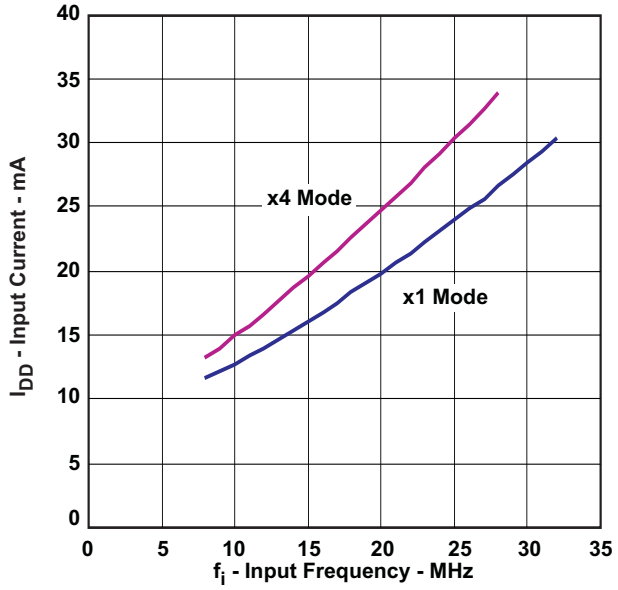


Figure 2. I_{DD} vs Input Frequency, V_{CC} = 3.3 V, SSC = 2%, Output Loaded With Test Load

APPLICATION INFORMATION

SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS503-Q1 device uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using one of the below formulas chosen by frequency multiplication mode.

FS = 0: $f_{mod} = f_{IN} / 708$

FS = 1: $f_{mod} = f_{IN} / 620$

PARAMETER MEASUREMENT INFORMATION

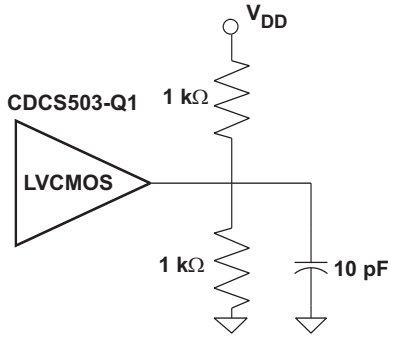


Figure 3. Test Load

PARAMETER MEASUREMENT INFORMATION (continued)

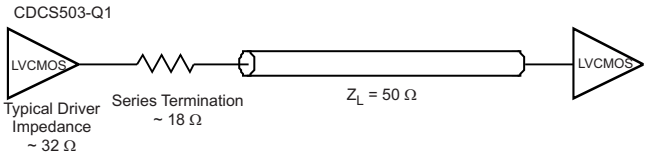


Figure 4. Load for 50-Ω Board Environment

REVISION HISTORY

Changes from Revision A (June 2012) to Revision B	Page
• 在 FAD 中将符合 AEC Q100 标准改为了 AEC Q100 测试指南	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCS503TPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	CS503Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CDCS503-Q1 :

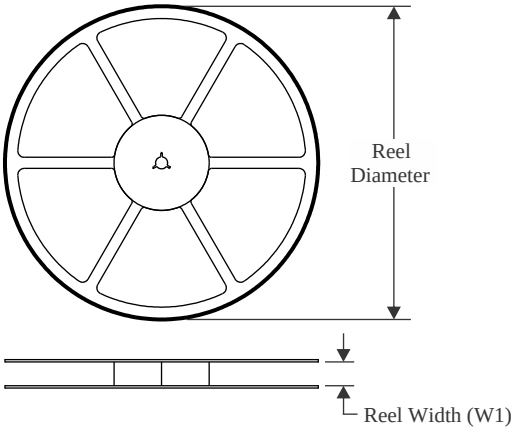
- Catalog: CDCS503

NOTE: Qualified Version Definitions:

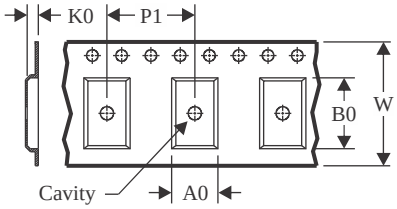
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

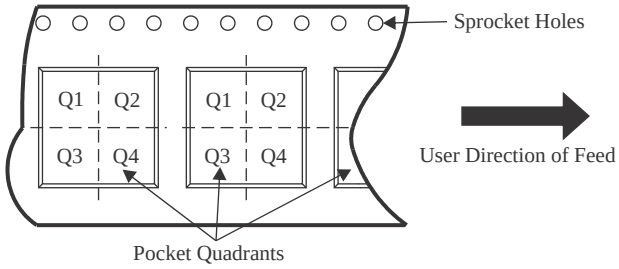


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

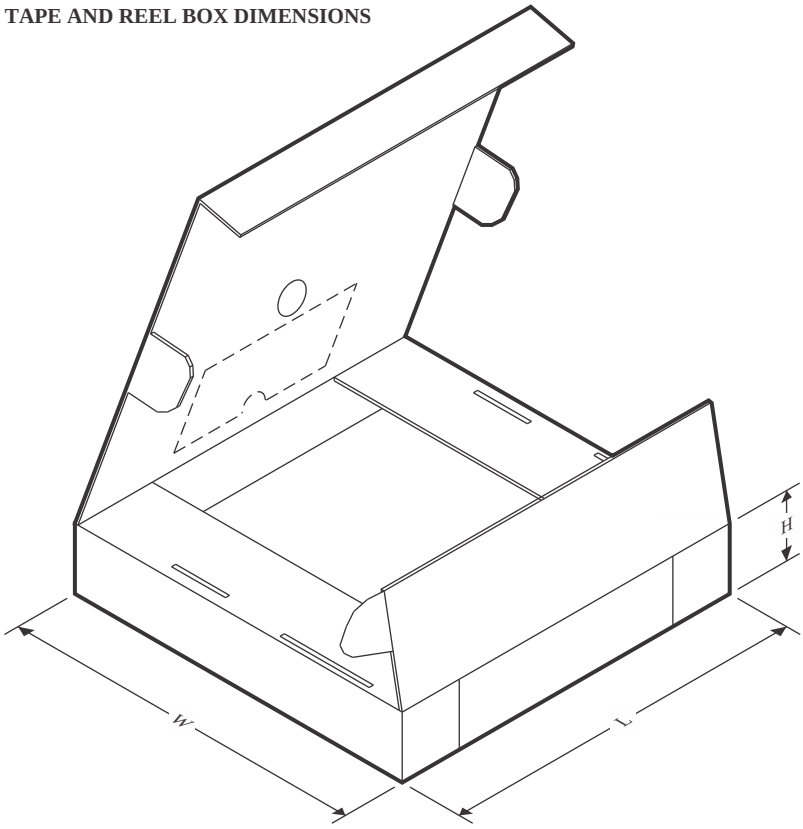
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCS503TPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

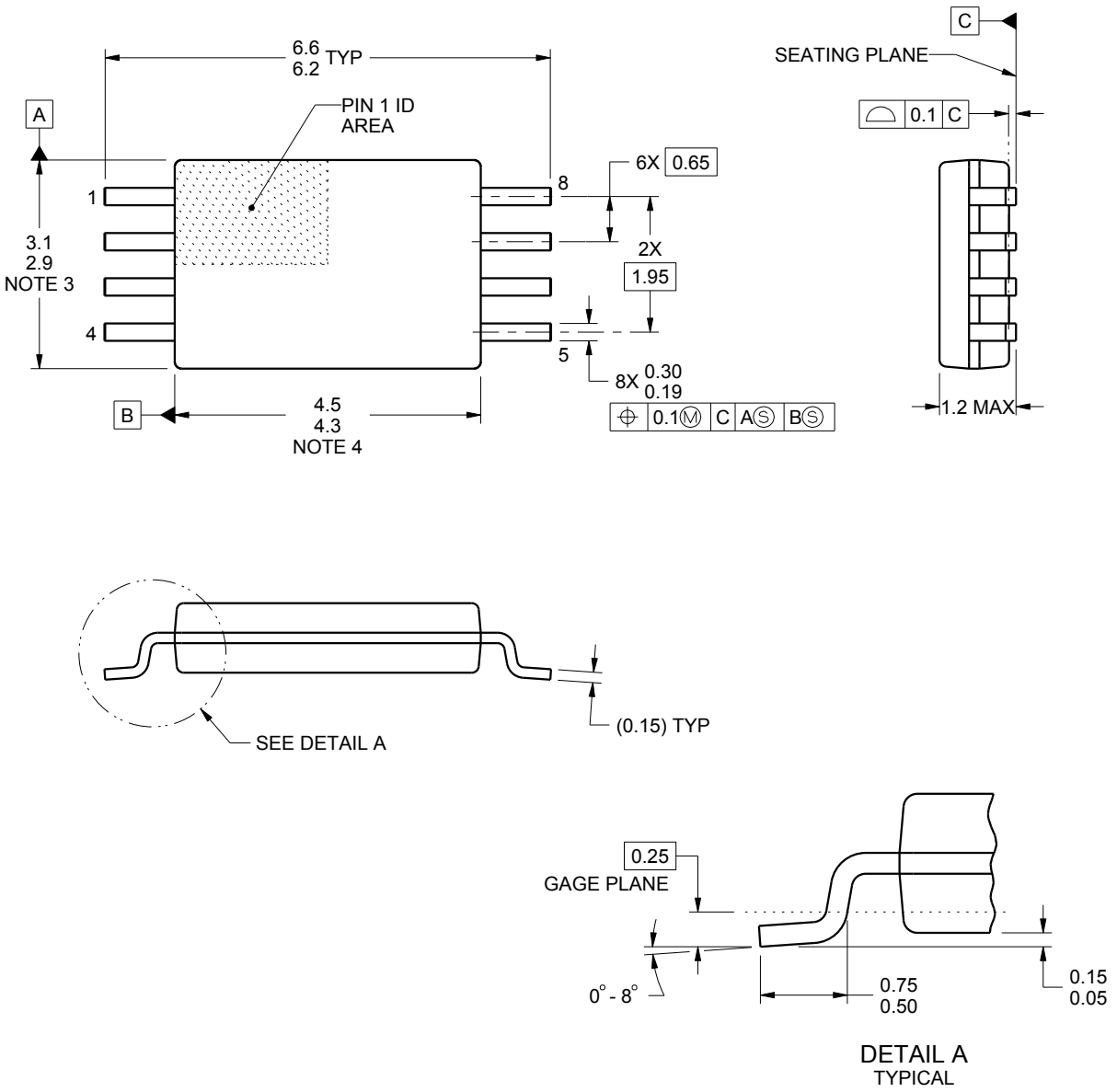
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCS503TPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0008A

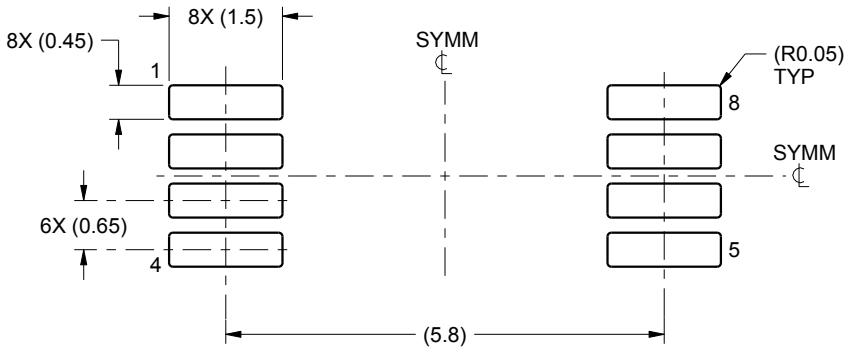
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

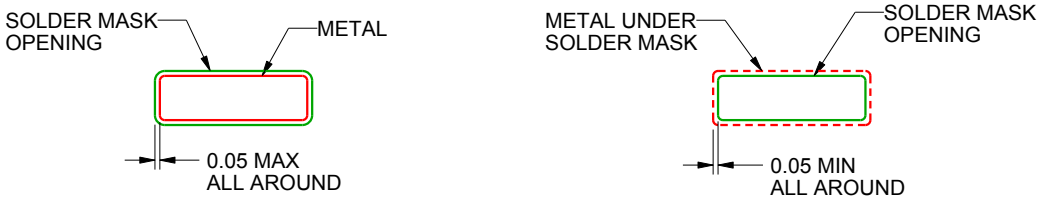


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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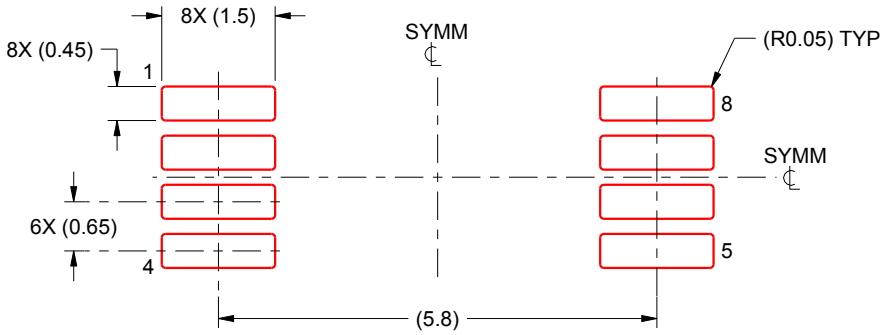
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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