CSD16556Q5B 25V N 沟道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低电阻
- 超低 Q_g和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 5mm x 6mm 塑料封装

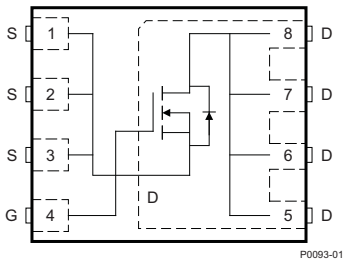
2 应用范围

- 网络互联、电信和计算系统中的负载点同步降压
- 已针对同步场效应晶体管 (FET) 应用进行优化

3 说明

这款 25V、0.9mΩ、5mm × 6mm SON NexFET™ 功率 MOSFET 设计用于大大降低同步整流和其它功率转换应用中的损耗。

顶视图



产品概要

T_A = 25°C		典型值	单位
V_{DS}	漏源电压	25	V

产品概要 (接下页)

T_A = 25°C		典型值		单位
Q_g	栅极电荷总量 (4.5V)	36		nC
Q_{gd}	栅极电荷（栅极到漏极）	12		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5 V	1.2	mΩ
		V_{GS} = 10V	0.9	mΩ
$V_{GS(th)}$	阈值电压	1.4		V

订购信息(1)

器件	介质	数量	封装	出货
CSD16556Q5B	13 英寸卷带	2500	SON 5mm x 6mm 塑料封装	卷带封装
CSD16556Q5BT	7 英寸卷带	250		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

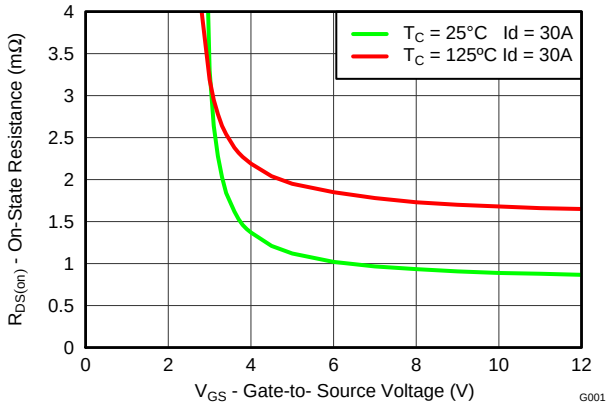
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	25	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	263	
	持续漏极电流(1)	40	A
I_{DM}	脉冲漏极电流(2)	400	A
P_D	功率耗散(1)	3.2	W
	功率耗散，T_C = 25°C	191	
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 103A，L = 0.1mH，R_G = 25Ω	530	mJ

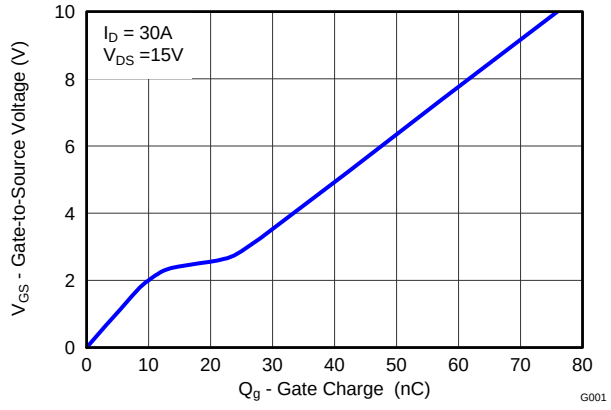
(1) $R_{\theta JA}$=40°C/W，这是在一块厚度为 0.06 英寸 (1.52mm) 的 FR4 印刷电路板 (PCB) 上的一英寸^2(6.45cm^2)，2 盎司（厚度 0.071mm）的铜过渡垫片上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 1.3°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2013) to Revision C **Page**

- 已将器件编号添加至标题 ... 1
- 已在订购信息中添加“7 英寸卷带” ... 1
- 已将最大脉冲电流增加至 400A ... 1
- 已添加外壳温度保持在 25ºC 时的最大功耗一行 ... 1
- 已更新脉冲电流条件 ... 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve ... 4
- Updated the SOA in Figure 10 ... 6
- 已更新机械制图和尺寸表 ... 8

Changes from Revision A (December 2012) to Revision B **Page**

- Changed g_{fs}, Transconductance TYP value From: 2 S To: 191 S ... 3

Changes from Original (November 2012) to Revision A **Page**

- 已将器件状态从“产品预览”更改为“量产数据” ... 1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = 250 µA	25			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.2	1.4	1.7	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_{DS} = 30 A		1.2	1.5	mΩ
		V_{GS} = 10 V, I_{DS} = 30 A		0.9	1.07	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 30 A		191		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1MHz		4750	6180	pF
C_{oss}	Output Capacitance			2270	2950	pF
C_{rss}	Reverse Transfer Capacitance			220	280	pF
R_G	Series Gate Resistance			0.7	1.4	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_{DS} = 30 A		36	47	nC
Q_{gd}	Gate Charge Gate-to-Drain			12		nC
Q_{gs}	Gate Charge Gate-to-Source			11		nC
$Q_{g(th)}$	Gate Charge at Vth			7		nC
Q_{oss}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		45		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 30 A,R_G = 2 Ω		17		ns
t_r	Rise Time			34		ns
$t_{d(off)}$	Turn Off Delay Time			25		ns
t_f	Fall Time			13		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 30 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD}= 15 V, I_F = 30 A, di/dt = 300 A/µs		84		nC
t_{rr}	Reverse Recovery Time			41		ns

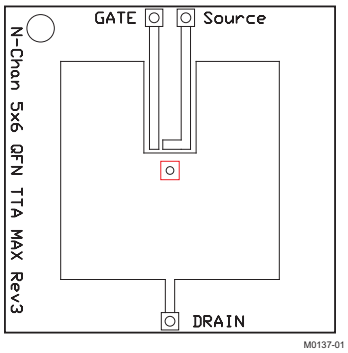
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

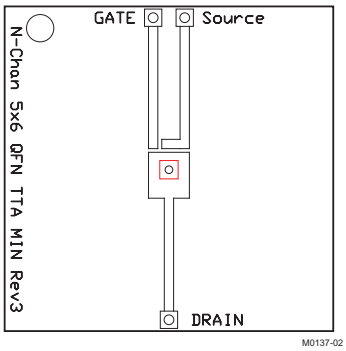
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			1.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

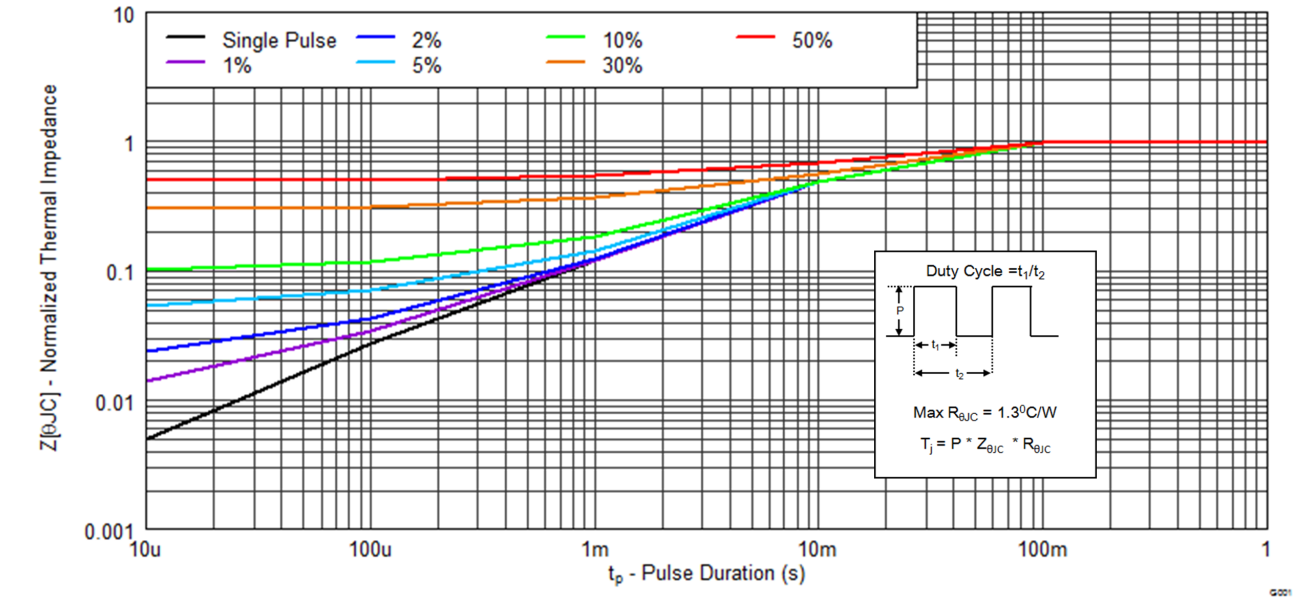


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

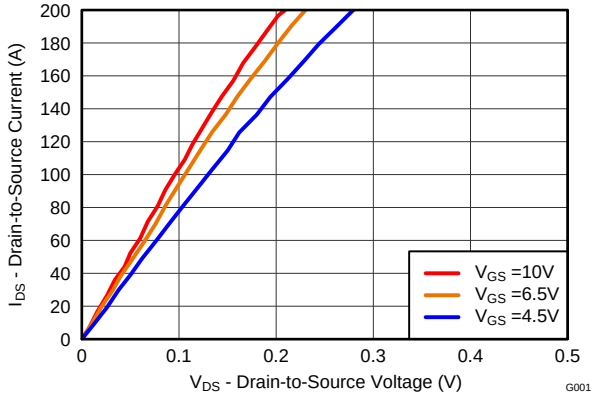


Figure 2. Saturation Characteristics

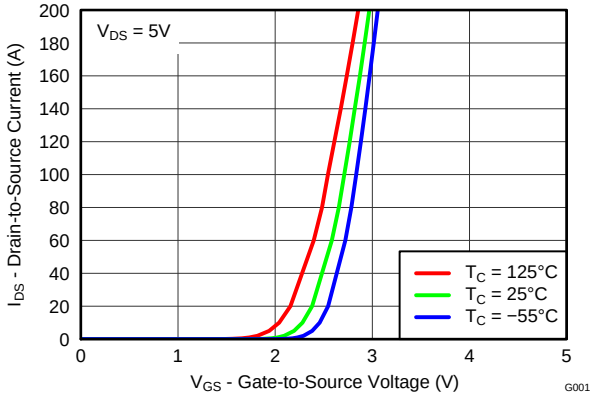


Figure 3. Transfer Characteristics

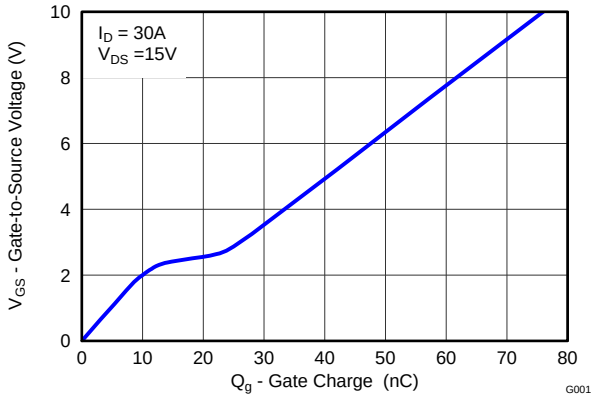


Figure 4. Gate Charge

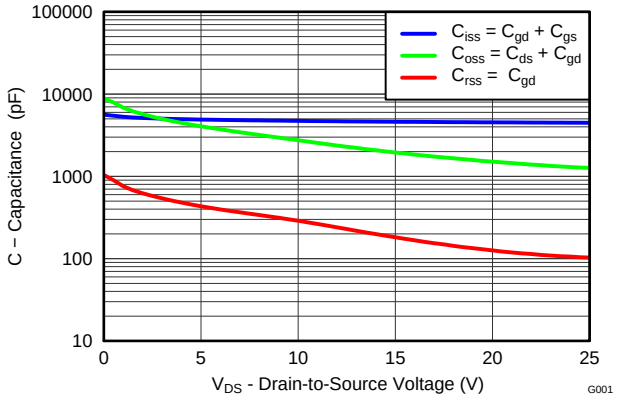


Figure 5. Capacitance

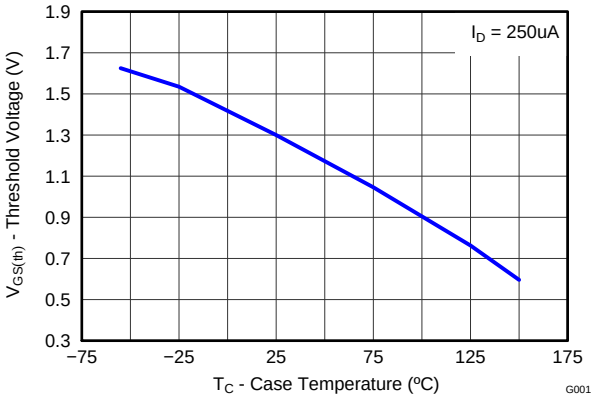


Figure 6. Threshold Voltage vs Temperature

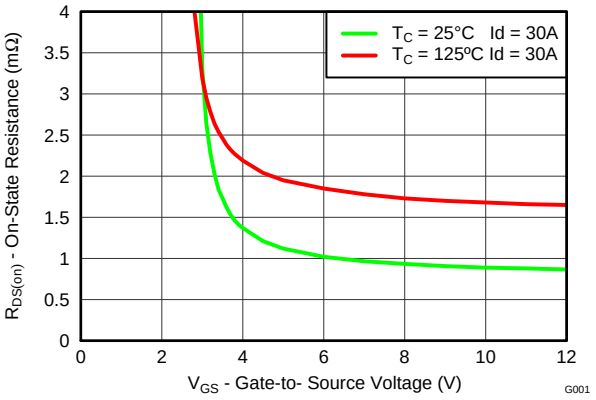


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

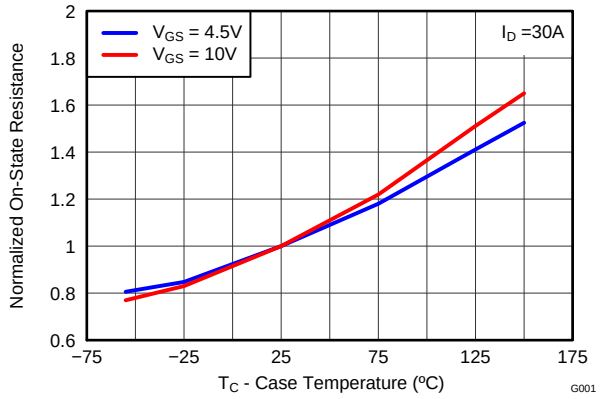


Figure 8. Normalized On-State Resistance vs Temperature

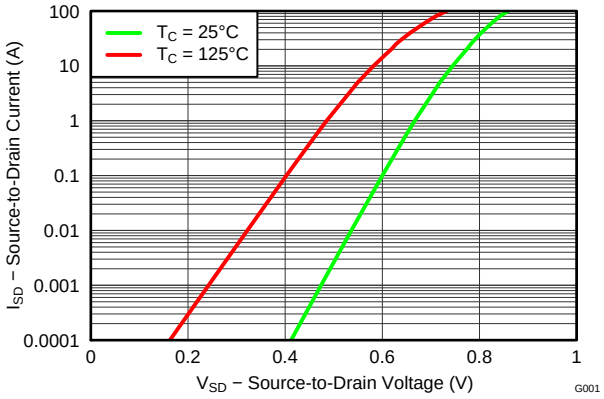


Figure 9. Typical Diode Forward Voltage

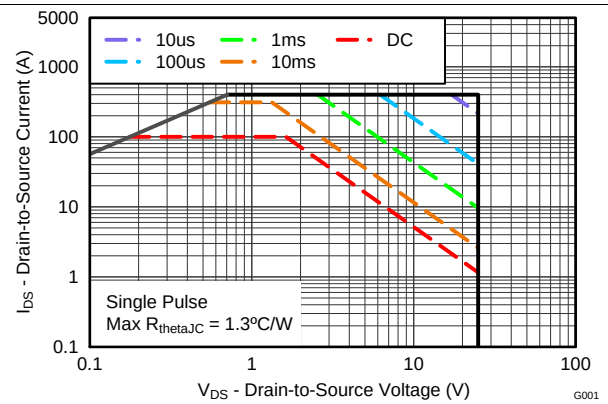


Figure 10. Maximum Safe Operating Area (SOA)

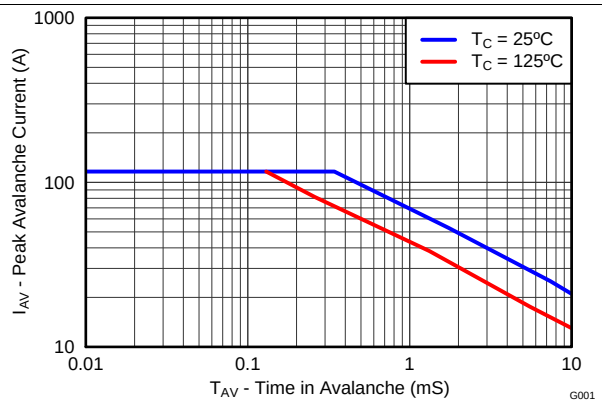


Figure 11. Single Pulse Unclamped Inductive Switching

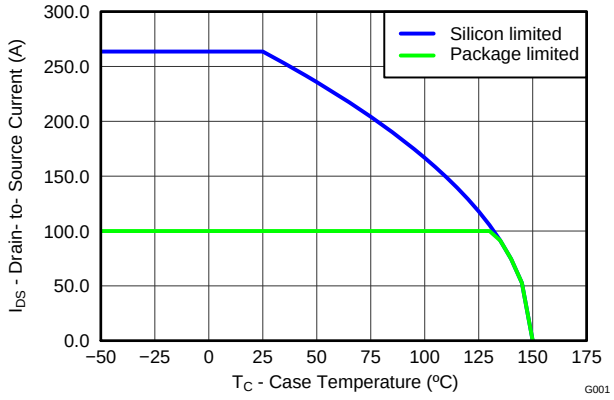


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

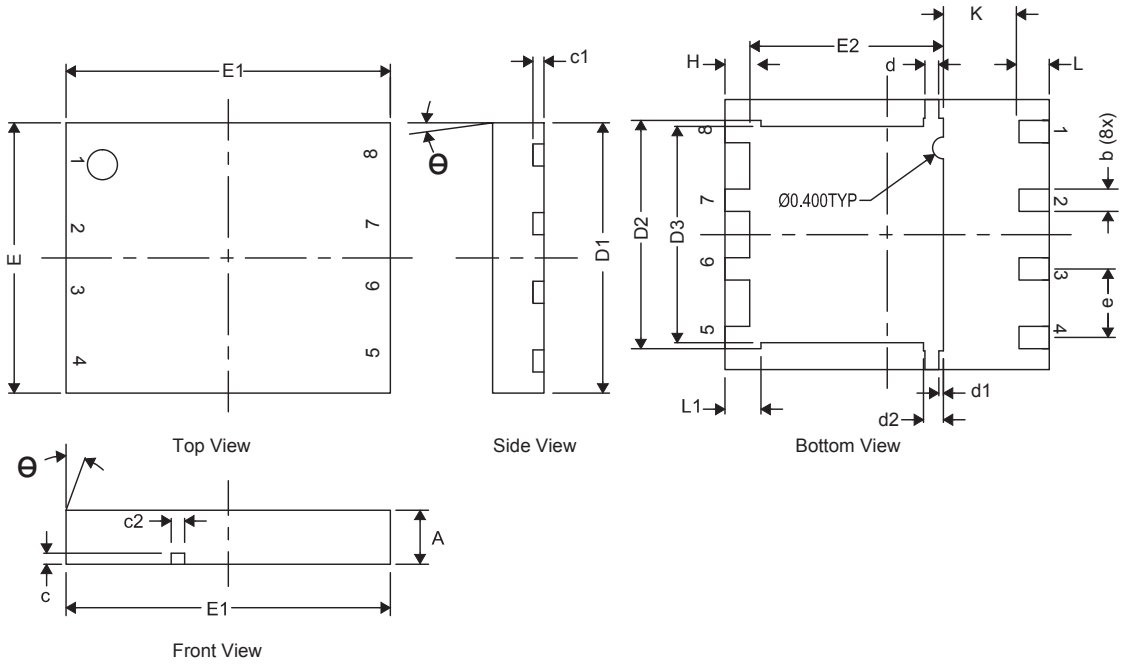
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械、封装和可订购信息

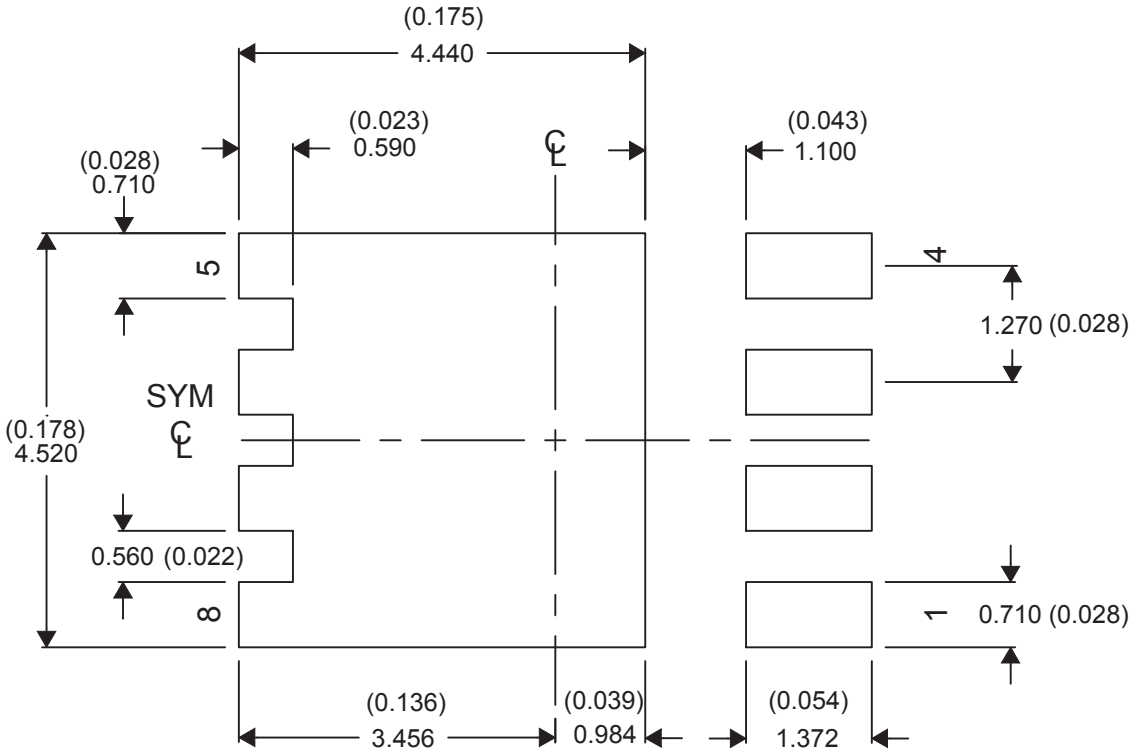
以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q5B 封装尺寸



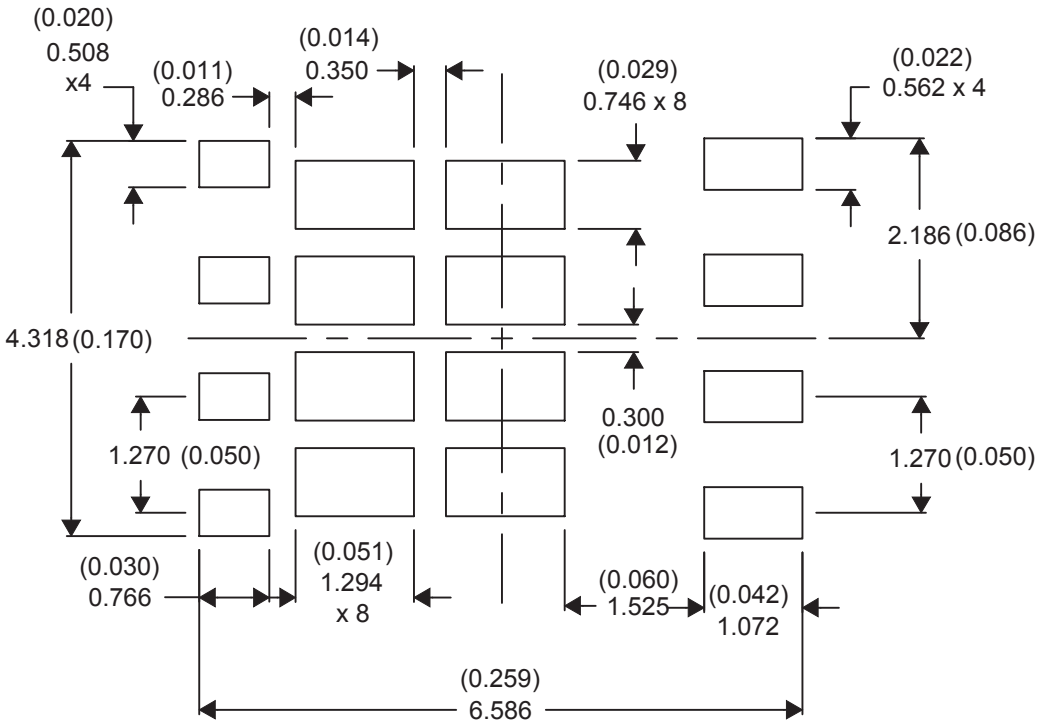
DIM	毫米		
	最小值	标称值	最大值
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 典型值		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 典型值		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 典型值		

7.2 建议 PCB 布局

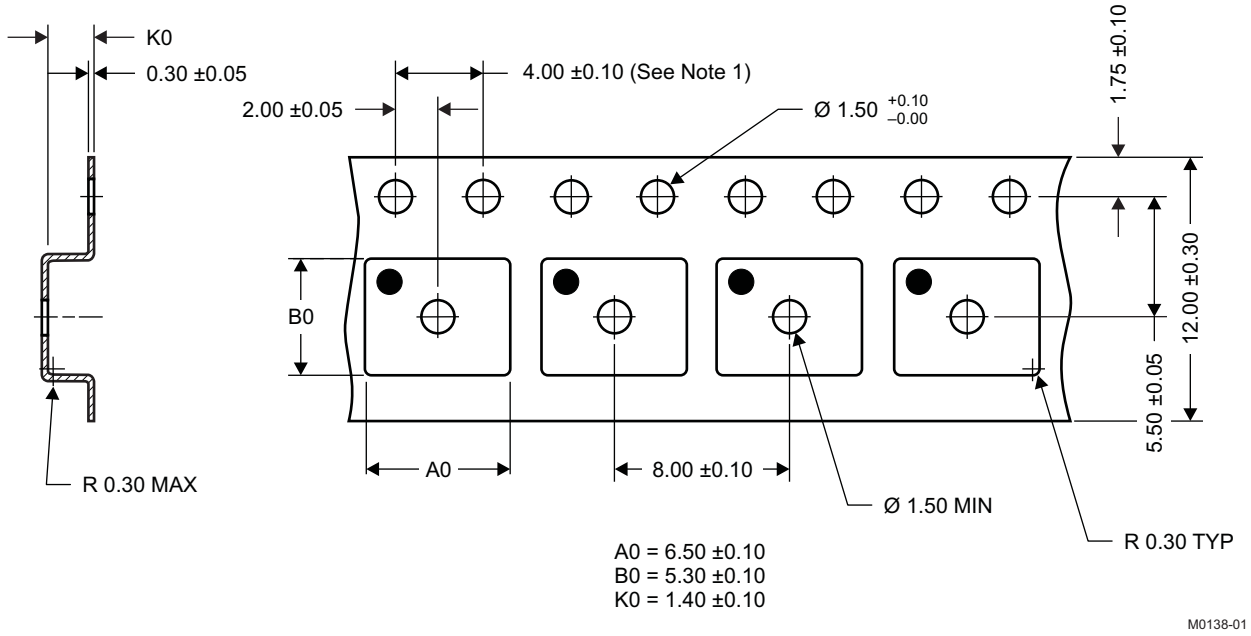


要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模板布局



7.4 Q5B 卷带信息



注释：

1. 10 个链齿孔的累积容差为 ±0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16556Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16556	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要声明和免责声明

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