CSD25310Q2 20V P 沟道 NexFET™ 功率 MOSFET

1 特性

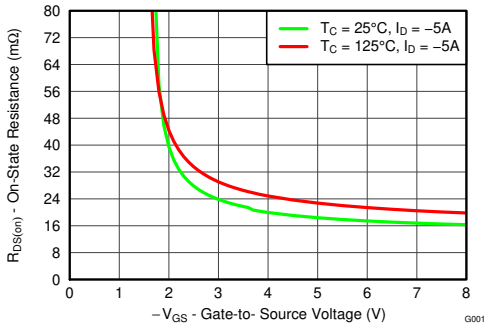
- 超低 Q_g 和 Q_{gd}
- 低导通电阻
- 低热阻
- 无铅
- 符合 RoHS
- 无卤素
- SON 2mm × 2mm 塑料封装

2 应用

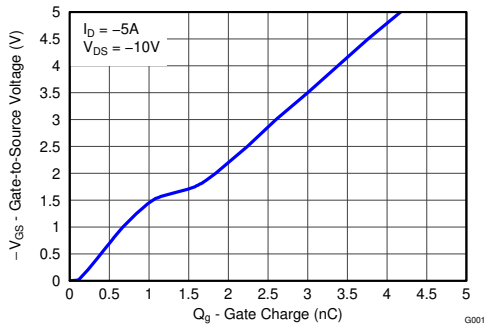
- 电池管理
- 负载管理
- 电池保护

3 说明

这款 19.9mΩ、–20V P 沟道器件旨在以超薄且具有出色散热特性的极小封装提供更低的导通电阻和栅极电荷。该器件将低导通电阻与 SON 2mm × 2mm 塑料封装的极小封装尺寸融为一体，堪称电池供电型空间受限应用的理想之选。



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	栅极电荷总量（– 4.5V）	3.6		nC
Q_{gd}	栅漏栅极电荷	0.5		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -1.8V	59.0	mΩ
		V_{GS} = -2.5V	27.0	mΩ
		V_{GS} = -4.5V	19.9	mΩ
$V_{GS(th)}$	阈值电压	-0.85		V

订购信息

器件	介质	数量	封装	配送
CSD25310Q2	7 英寸卷带	3000	SON 2 x 2mm 塑料封装	卷带包装
CSD25310Q2T	7 英寸卷带	250		

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	±8	V
I_D	持续漏极电流（受封装限制）	-20	A
	持续漏极电流(1)	-9.6	A
I_{DM}	脉冲漏极电流(2)	48	A
P_D	功率耗散 1. $R_{\theta JA}$ = 43°C/W，这是在一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 平方英寸（2 盎司）覆铜上测得的典型值。	2.9	W
T_J，T_{stg}	运行结温和储存温度范围	-55 至 150	°C

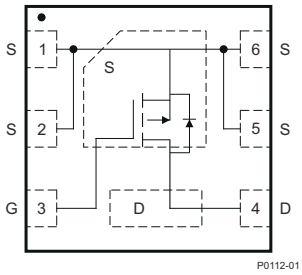


图 3-1. 顶视图

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4 Revision History

Changes from Revision A (June 2014) to Revision B (March 2022) **Page**

- Updated drain and source connection images.....4

Changes from Revision * (January 2014) to Revision A (June 2014) **Page**

- 已将“无铅端子镀层”修改为唯一状态“无铅”.....1
- 在订购信息表中添加了小卷带选项.....1

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 μA	–20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –8 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.55	–0.85	–1.10	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V, I_{DS} = –5 A		59.0	89.0	mΩ
		V_{GS} = –2.5 V, I_{DS} = –5 A		27.0	32.5	mΩ
		V_{GS} = –4.5 V, I_{DS} = –5 A		19.9	23.9	mΩ
g_{fs}	Transconductance	V_{DS} = –16 V, I_{DS} = –5 A		34		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		504	655	pF
C_{OSS}	Output Capacitance			281	365	pF
C_{RSS}	Reverse Transfer Capacitance			16.7	21.7	pF
R_g	Series Gate Resistance			1.9		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –5 A		3.6	4.7	nC
Q_{gd}	Gate Charge Gate to Drain			0.5		nC
Q_{gs}	Gate Charge Gate to Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		5.0		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –5 A R_G = 2 Ω		8		ns
t_r	Rise Time			15		ns
$t_{d(off)}$	Turn Off Delay Time			15		ns
t_f	Fall Time			5		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = –5 A, V_{GS} = 0 V		–0.8	–1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = –10 V, I_F = –5 A, di/dt = 200 A/μs		9.2		nC
t_{rr}	Reverse Recovery Time			13		ns

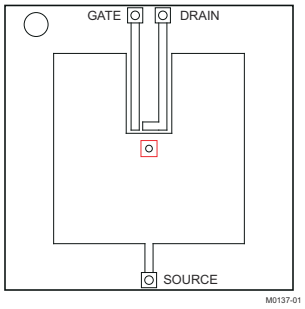
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

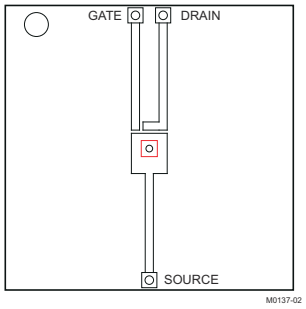
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			4.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			55	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 55 when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 215 when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

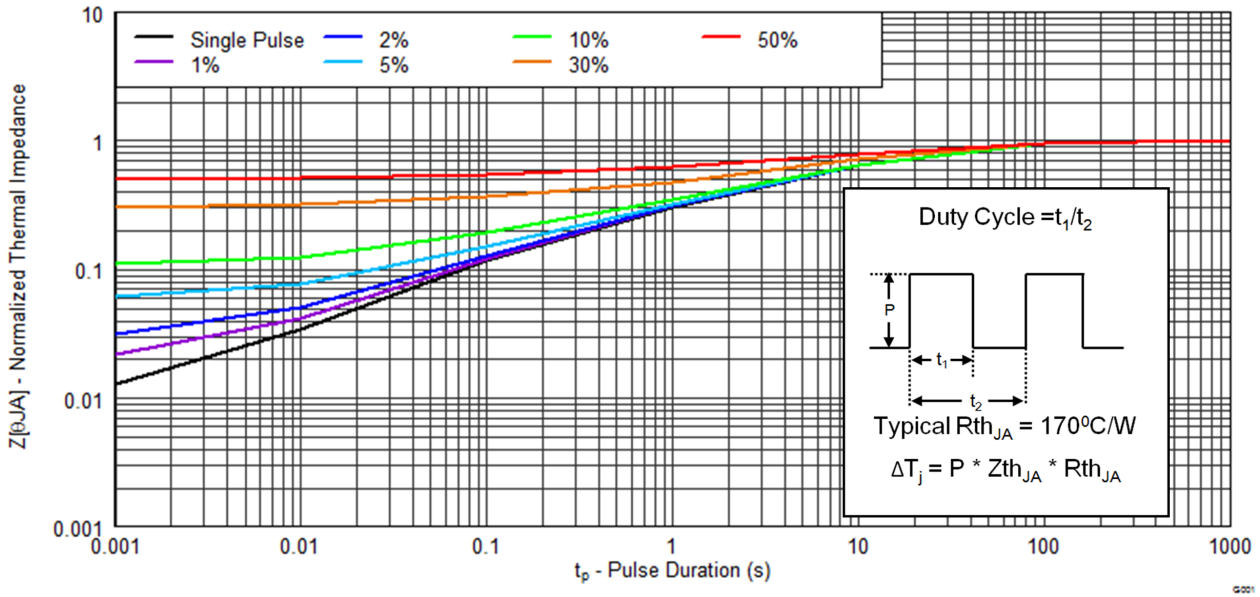


图 5-1. Transient Thermal Impedance

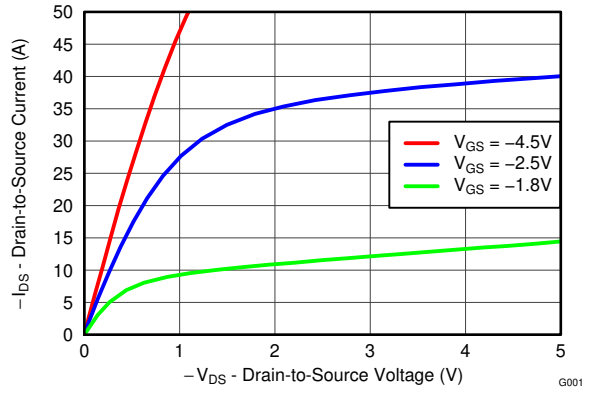


图 5-2. Saturation Characteristics

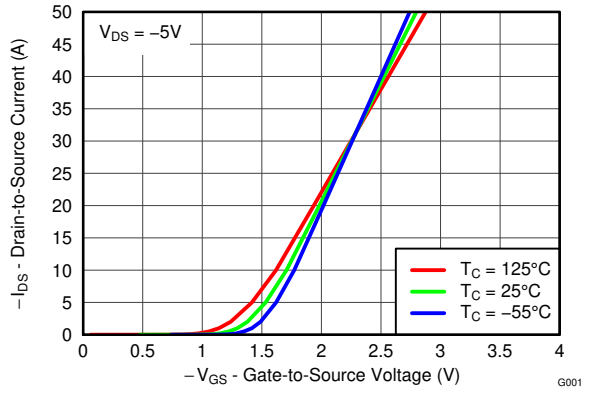


图 5-3. Transfer Characteristics

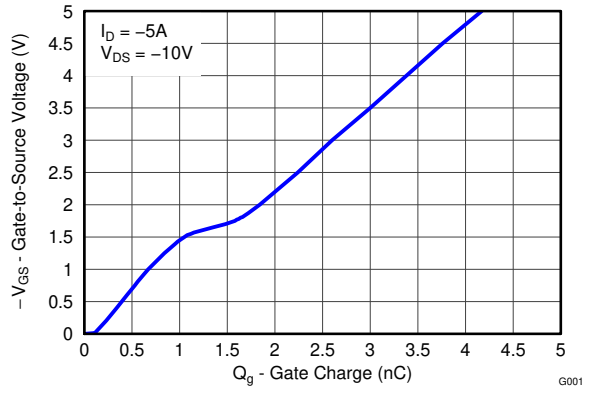


图 5-4. Gate Charge

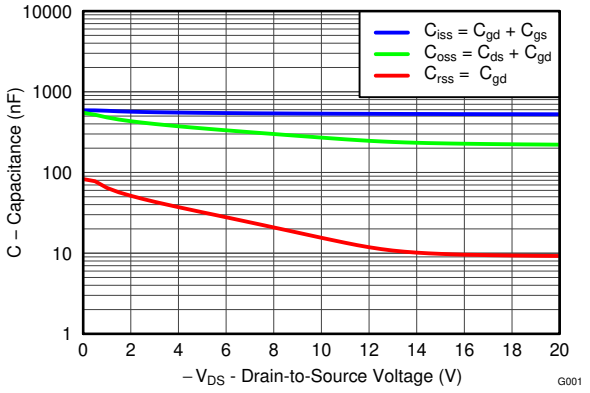


图 5-5. Capacitance

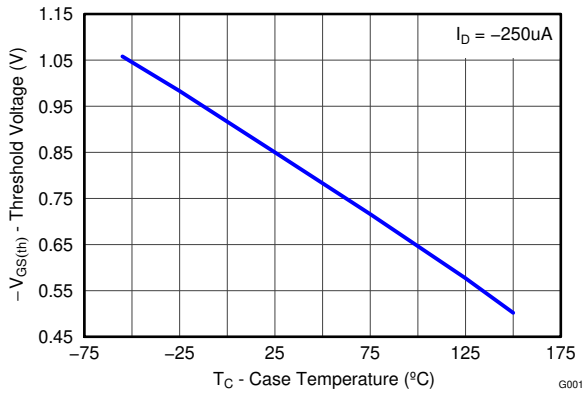


图 5-6. Threshold Voltage vs Temperature

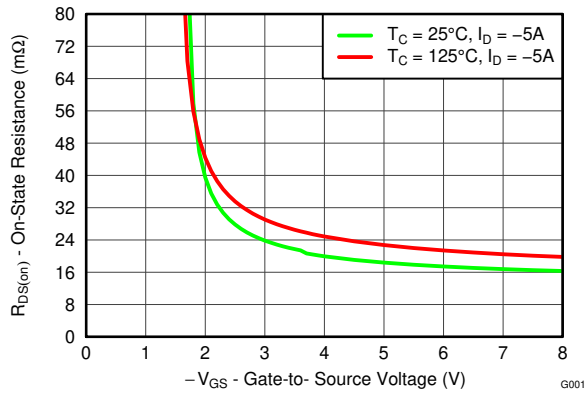


图 5-7. On-State Resistance vs Gate-to-Source Voltage

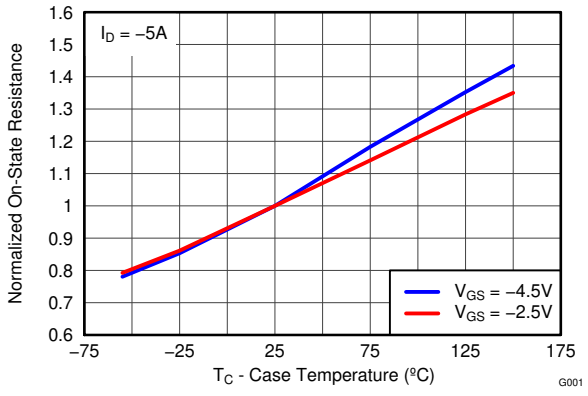


图 5-8. Normalized On-State Resistance vs Temperature

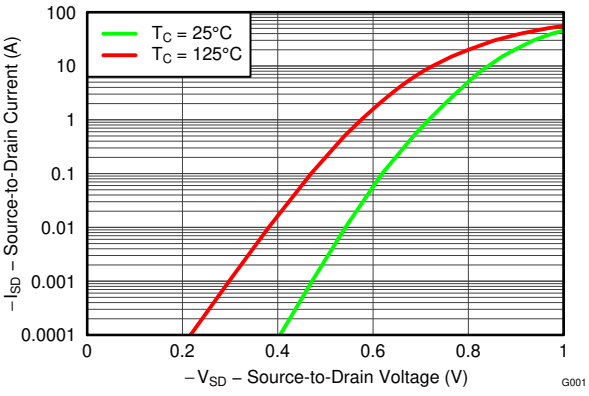


图 5-9. Typical Diode Forward Voltage

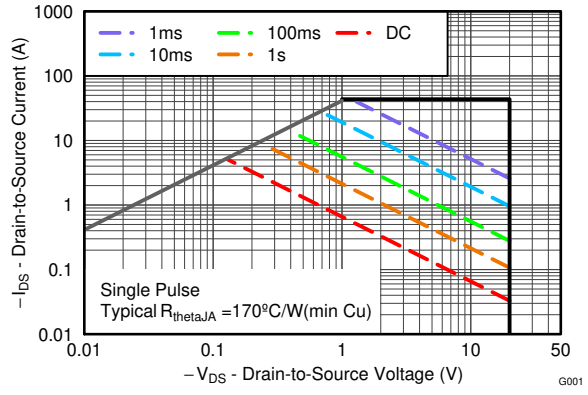


图 5-10. Maximum Safe Operating Area

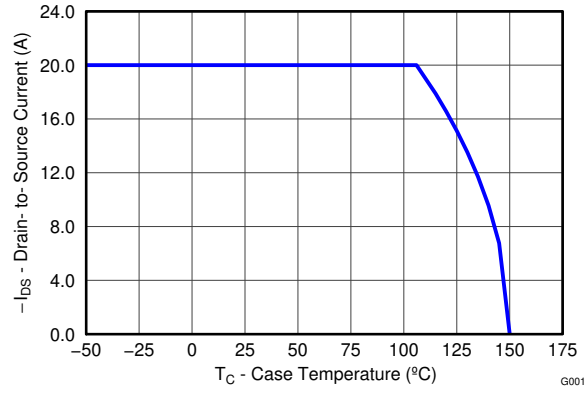


图 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET™ is a trademark of TI.
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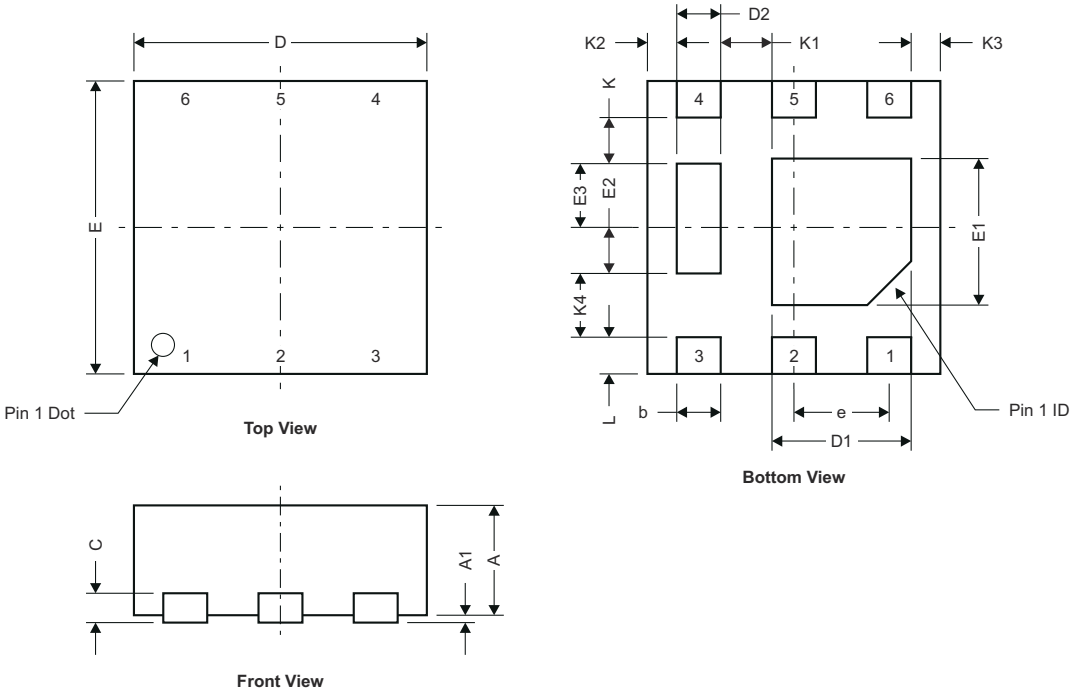
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

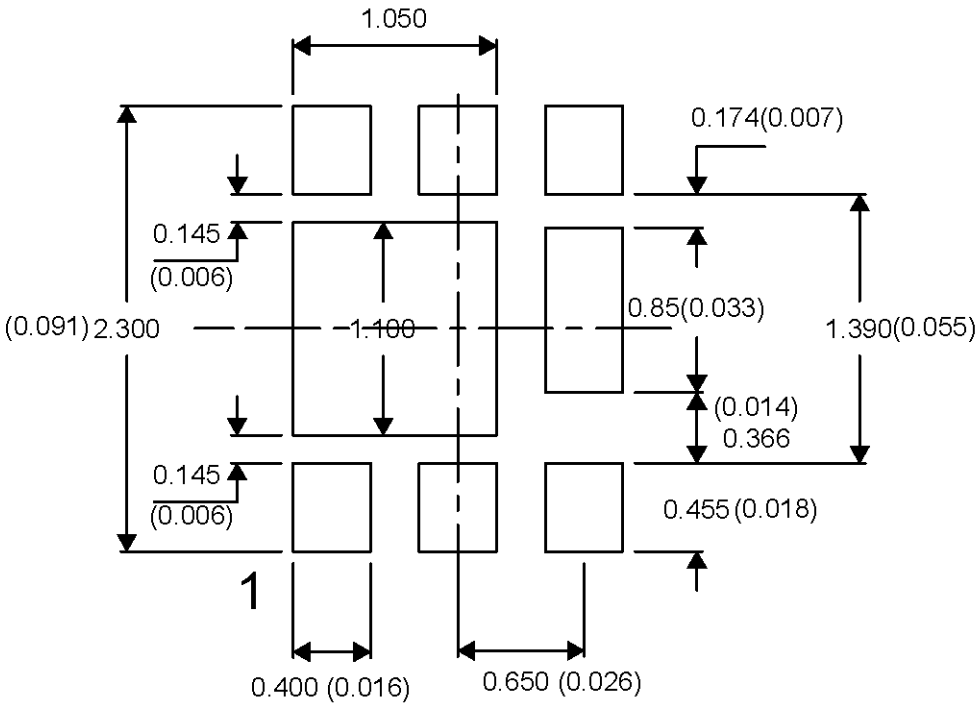
7.1 Q2 Package Dimensions



M0165-01

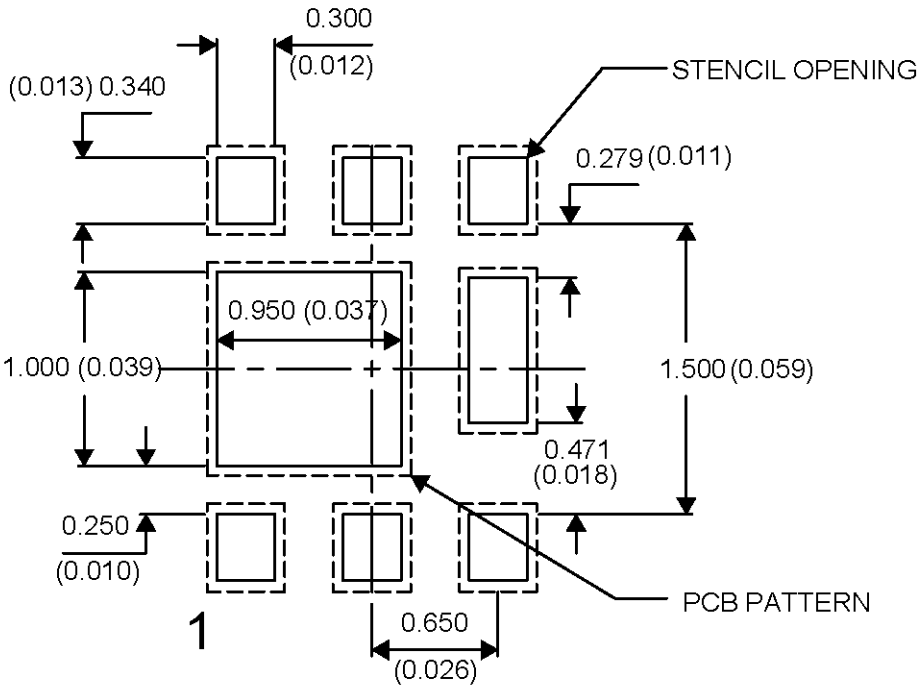
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 TYP			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.012

7.2 Recommended PCB Pattern



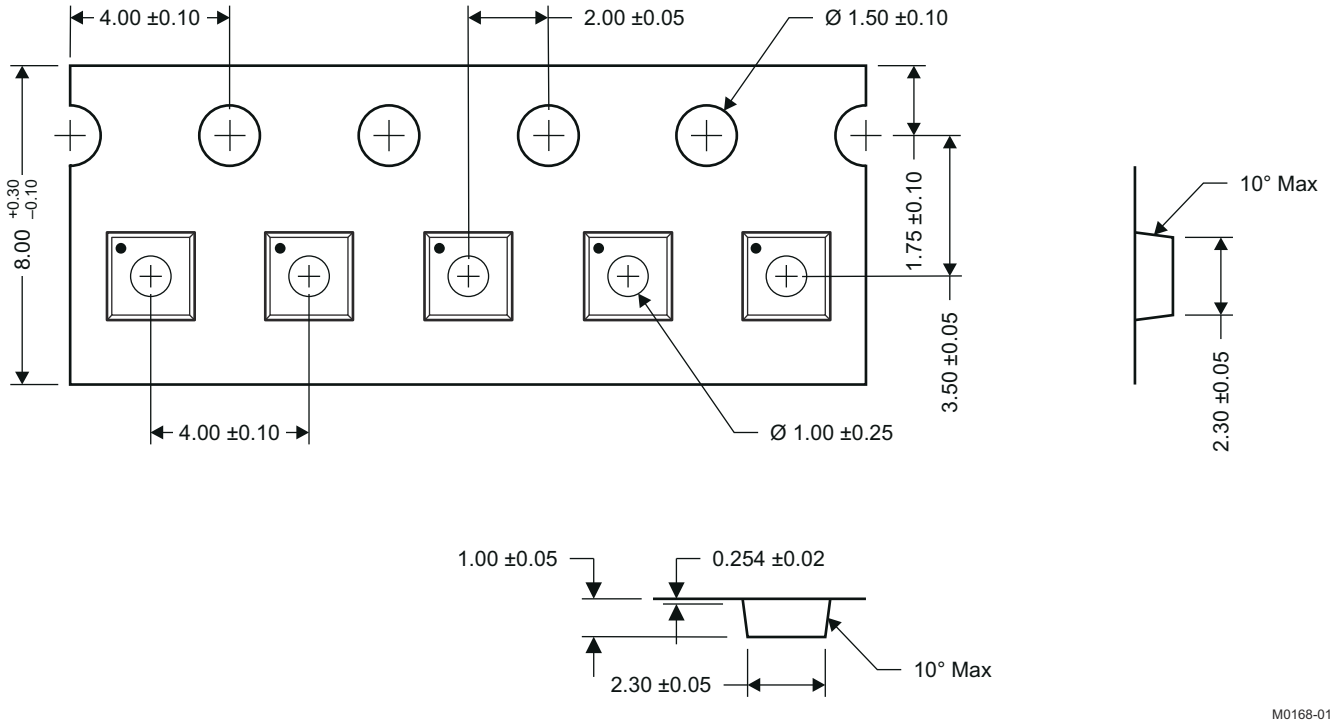
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Pattern



All dimensions are in mm, unless otherwise specified.

7.4 Q2 Tape and Reel Information



1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.20
3. Other material available
4. Typical SR of form tape Max 10^9 OHM/SQ
5. All dimensions are in mm, unless otherwise specified.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25310Q2	ACTIVE	WSON	DQK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	2530	Samples
CSD25310Q2T	ACTIVE	WSON	DQK	6	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	2530	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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