CSD75208W1015 双路 20V 共源 P 通道 NexFET™功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 双路 P 通道 MOSFET
- 共源配置
- 1.5mm x 1mm 小尺寸封装
- 栅极 - 源电压钳位
- 栅极静电放电 (ESD) 保护 - 3kV
- 无铅
- 符合 RoHS 环保标准
- 无卤素

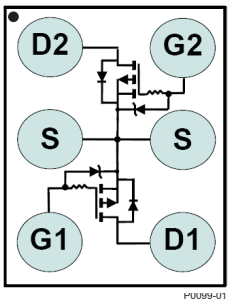
2 应用

- 电池管理
- 负载开关
- 电池保护

3 说明

此器件设计用于在超薄且具有出色散热特性的超小外形尺寸封装内提供最低的导通电阻和栅极电荷。低导通电阻与小型低厚度封装结合在一起，使得此器件成为电池供电运行空间受限应用的 理想选择。

顶视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	1.9		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.23		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = –1.8V	100	mΩ
		V_{GS} = -2.5V	70	mΩ
		V_{GS} = -4.5V	56	mΩ
R_{D1D2}（导通）	漏极到漏极导通电阻	V_{GS} = -1.8V	190	mΩ
		V_{GS} = -2.5V	120	mΩ
		V_{GS} = -4.5V	90	mΩ
$V_{GS(th)}$	阈值电压	-0.8		V

订购信息(1)

器件	数量	介质	封装	出货
CSD75208W1015	3000	7 英寸卷带	1.0mm × 1.5mm 晶圆级封装	卷带封装
CSD75208W1015T	250	7 英寸卷带		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

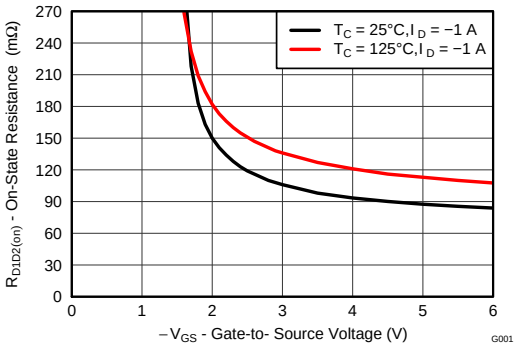
T_A = 25°C		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-6	V
I_{D1D2}	持续漏极到漏极电流，T_C = 25°C 时测得	-1.6	A
	脉冲漏极到漏极电流，T_C = 25°C(1) 时测得	–22	A
I_S	持续源引脚电流	–3	A
	(1)脉冲源引脚电流 (2)	–39	A
I_G	持续栅极钳位电流	-0.5	A
	脉冲栅极钳位电流(1)	-7	A
P_D	功率耗散	0.75	W
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C

(1) 最大 $R_{\theta JA}$ = 165ºC/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%

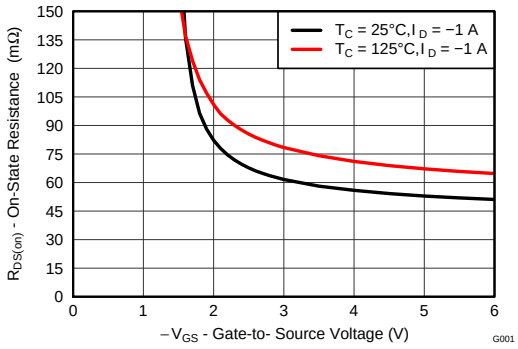
(2) 两器件并行

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

R_{D1D2}（导通）与 V_{GS} 间的关系



$R_{DS(on)}$ 与 V_{GS} 间的关系



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4 修订历史记录

Changes from Original (July 2014) to Revision A **Page**

- Changed Figure 1. ... 5
- 已添加 *社区资源* 和*接收文档更新通知* 部分添加到了*器件和文档支持*。 ... 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–20			V
BV_{GSS}	Gate-to-Source Voltage	V_{DS} = 0 V, I_G = –250 μA	–6.1		–7.2	V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.5	–0.8	–1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V, I_D = –1 A		100	150	mΩ
		V_{GS} = –2.5 V, I_D = –1 A		70	88	mΩ
		V_{GS} = –4.5 V, I_D = –1 A		56	68	mΩ
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	V_{GS} = –1.8 V, I_{D1D2} = –1 A		190	285	mΩ
		V_{GS} = –2.5 V, I_{D1D2} = –1 A		120	150	mΩ
		V_{GS} = –4.5 V, I_{D1D2} = –1 A		90	108	mΩ
g_{fs}	Transconductance	V_{DS} = –2 V, I_D = –1 A		7.5		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		315	410	pF
C_{OSS}	Output Capacitance			132	172	pF
C_{RSS}	Reverse Transfer Capacitance			7.7	10	pF
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –1 A		1.9	2.5	nC
Q_{gd}	Gate Charge, Gate-to-Drain			0.23		nC
Q_{gs}	Gate Charge, Gate-to-Source			0.48		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.31		nC
Q_{OSS}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		2.1		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –1 A, R_G = 0 Ω		9		ns
t_r	Rise Time			5		ns
$t_{d(off)}$	Turn Off Delay Time			29		ns
t_f	Fall Time			11		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = –1 A, V_{GS} = 0 V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = –10 V, I_F = –1 A, di/dt = 200 A/μs		4.3		nC
t_{rr}	Reverse Recovery Time			9		ns

5.2 Thermal Information

T_A = 25°C unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (1) (2)		165		°C/W
	Junction-to-Ambient Thermal Resistance (2) (3)		95		

(1) Device mounted on FR4 material with minimum Cu mounting area
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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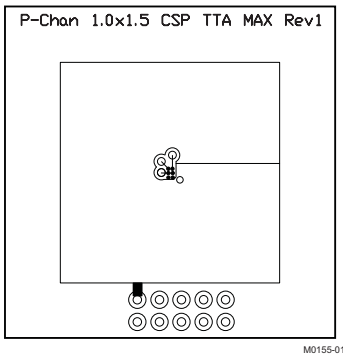
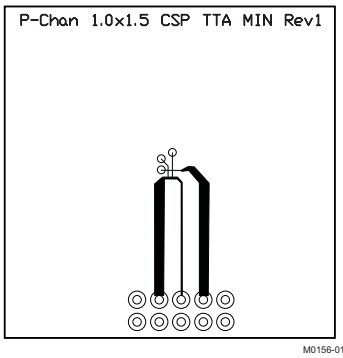


Typ $R_{\theta JA}$ = 95°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Typ $R_{\theta JA}$ = 165°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

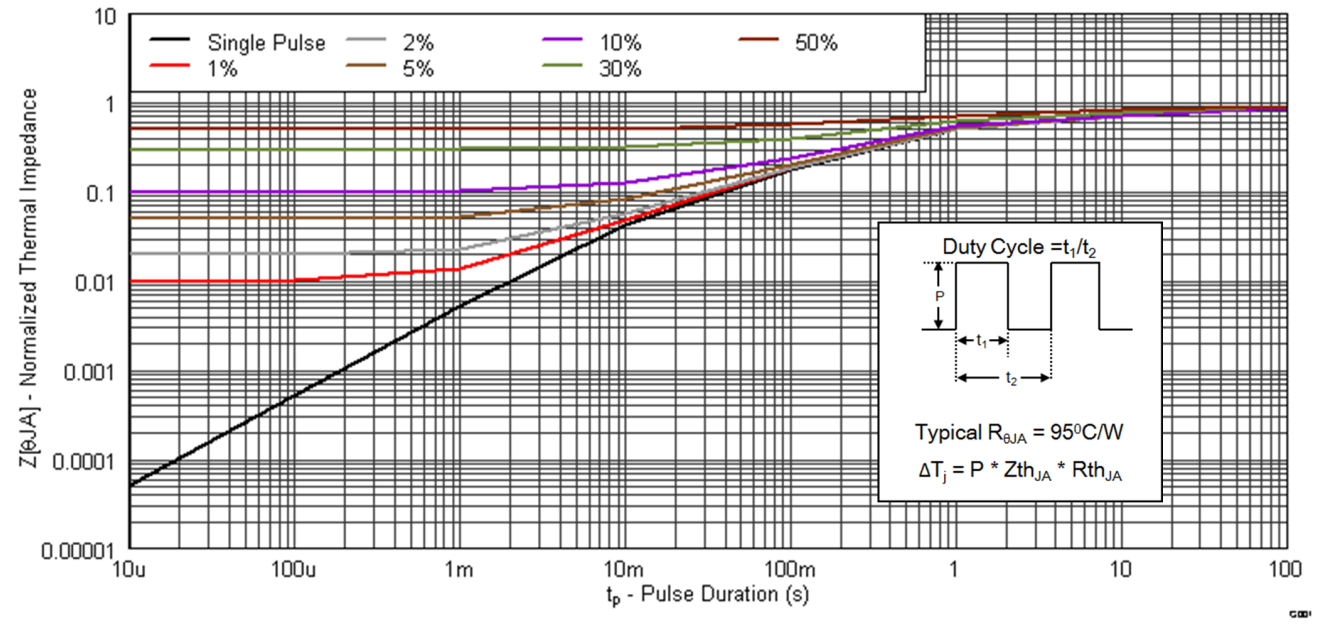


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

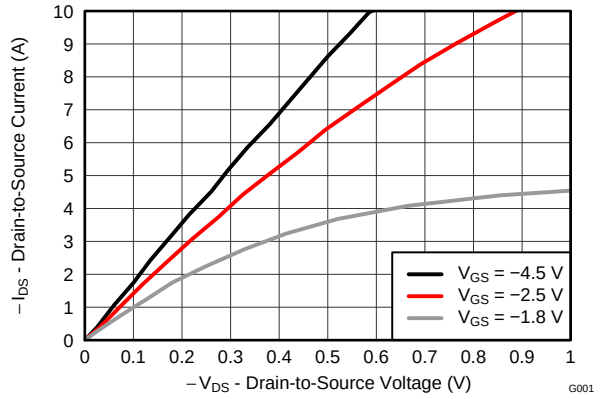


Figure 2. Saturation Characteristics

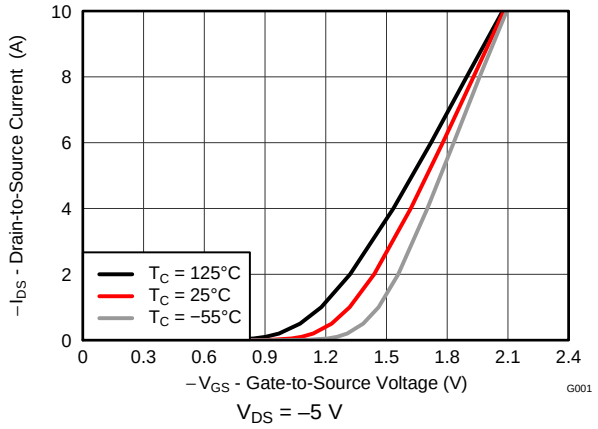


Figure 3. Transfer Characteristics

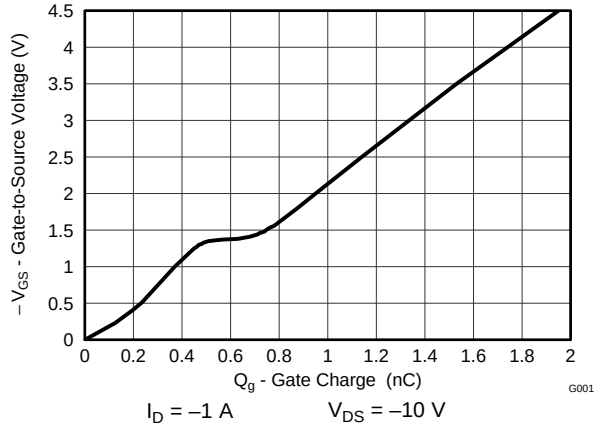


Figure 4. Gate Charge

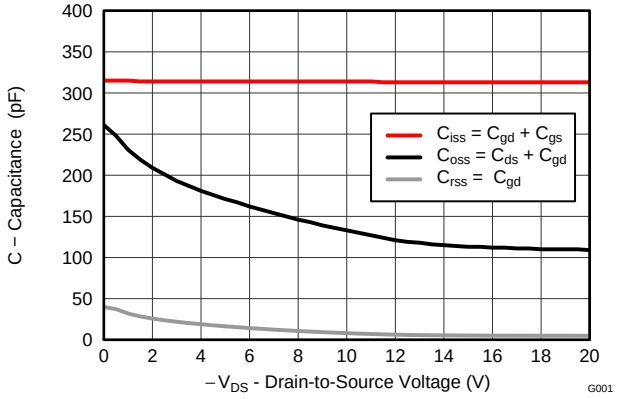


Figure 5. Capacitance

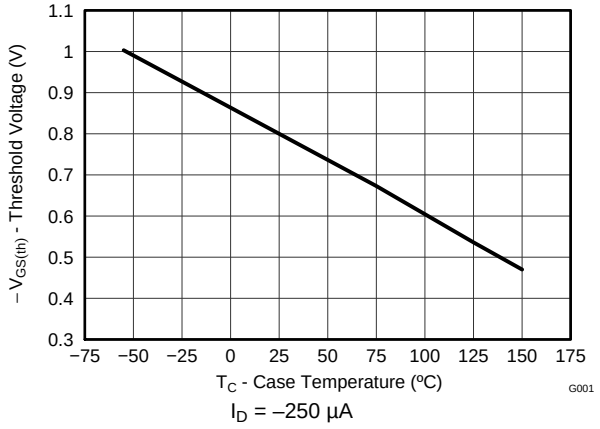


Figure 6. Threshold Voltage vs Temperature

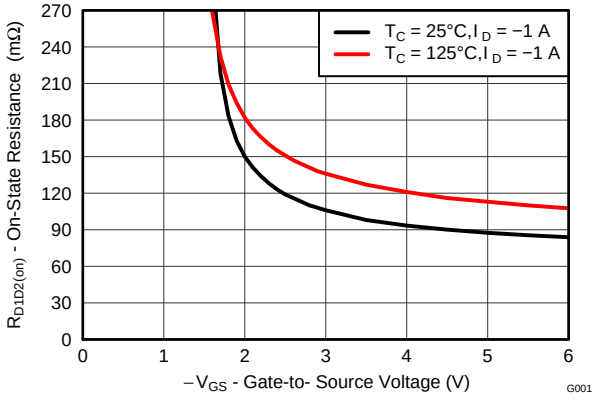


Figure 7. On-State Drain-to-Drain Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

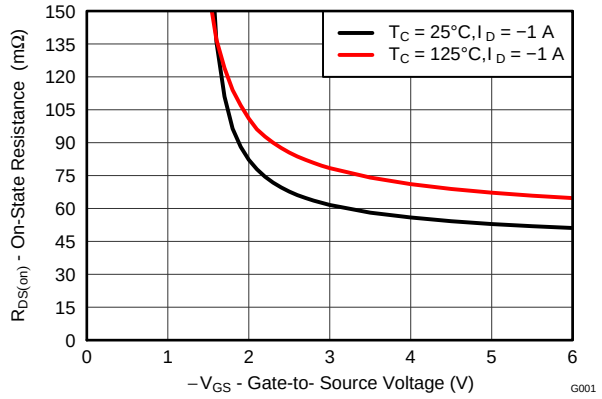

Figure 8. On-State Drain-to-Source Resistance vs Gate-to-Source Voltage

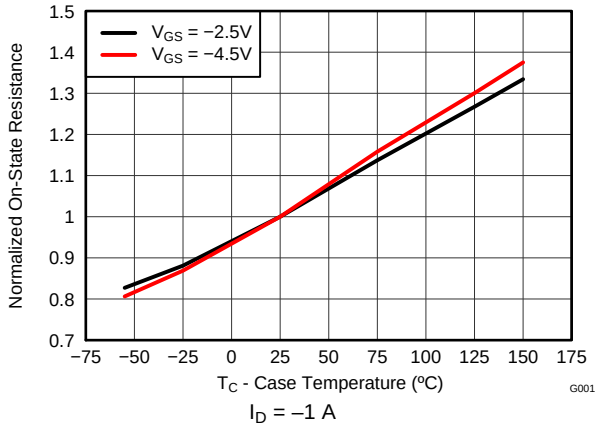

Figure 9. Normalized On-State Resistance vs Temperature

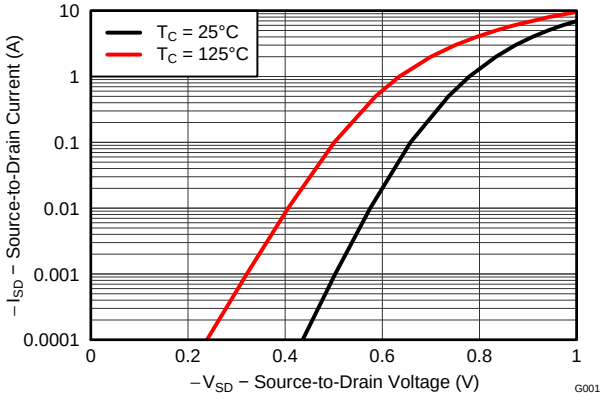

Figure 10. Typical Diode Forward Voltage

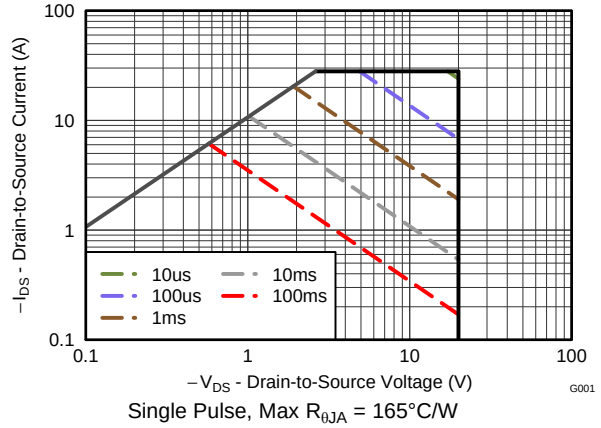

Figure 11. Maximum Safe Operating Area

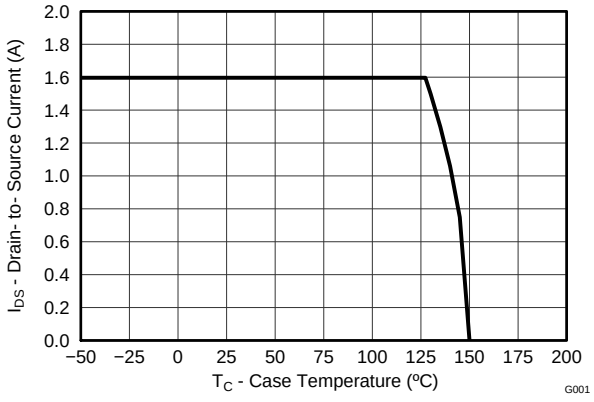

Figure 12. Maximum Drain Current vs Temperature

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6 器件和文档支持

将

6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我*进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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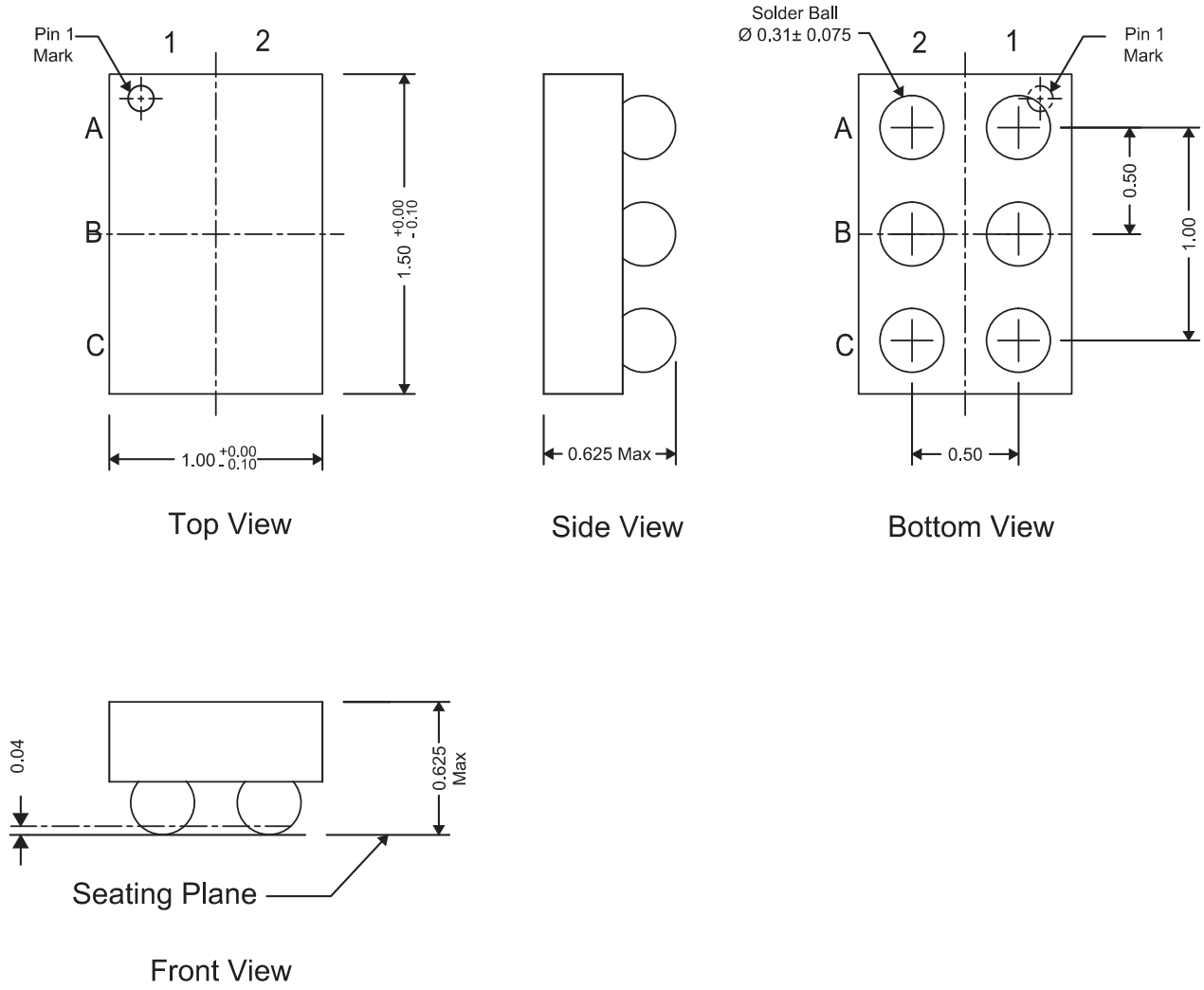
7 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

7.1 CSD75208W1015 封装尺寸

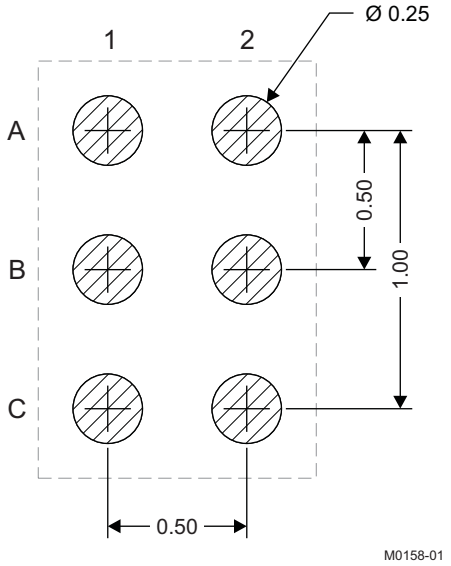


NOTE: 全部尺寸单位为 mm（除非另外注明）。

表 **1.** 引脚分配

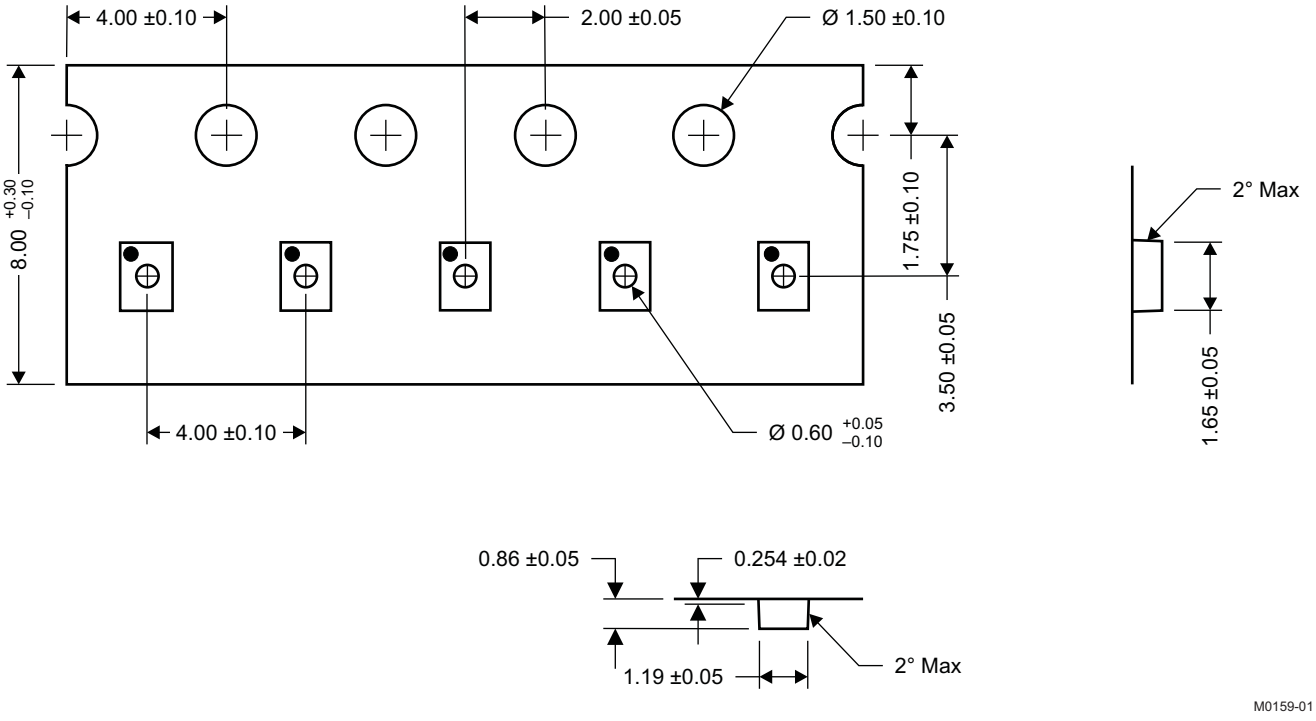
位置	名称
B1，B2	源极
C1	栅极 1
C2	漏极 1
A2	栅极 2
A1	漏极 2

7.2 建议印刷电路板 (PCB) 焊盘图案



NOTE: 全部尺寸单位为 mm（除非另外注明）。

7.3 卷带封装信息



NOTE: 全部尺寸单位为 mm（除非另外注明）。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD75208W1015	ACTIVE	DSBGA	YZC	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75208	Samples
CSD75208W1015T	ACTIVE	DSBGA	YZC	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75208	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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