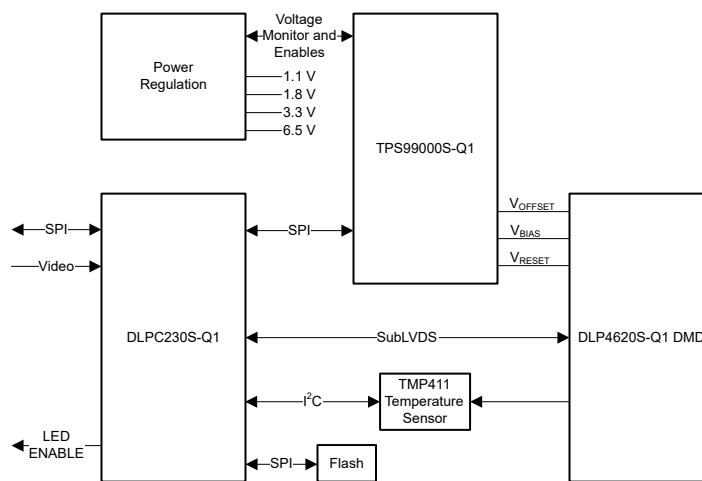**TEXAS INSTRUMENTS**

DLP4620S-Q1 适用于汽车显示应用的 DLP 数字微镜器件 (DMD)

1 特性

- 符合汽车应用要求
  - DMD 阵列工作温度范围 -40°C 至 105°C
- 功能安全质量管理型
  - 有助于使 ISO 2626 功能安全系统设计满足 ASIL-B 要求的文档
- DLP4620S-Q1 汽车芯片组包括：
  - DLP4620S-Q1 DMD
  - DLPC230S-Q1 DMD 控制器
  - TPS99000S-Q1 系统管理和照明控制器
- 0.46 英寸对角线微镜阵列
  - 7.6 μm 微镜间距
  - ±12° 微镜倾斜角（相对于平面）
  - Bottom 照明可实现高效率和更小的发动机尺寸
  - 高达 1920 × 960 分辨率，外部基于 GPU 的梅花形预处理
  - 1358 × 566 或 1220 × 610 分辨率模式
  - 与 LED 或激光照明兼容
- 600MHz subLVDS DMD 接口，可实现低功耗和低排放
- 温度极值下 DMD 刷新率为 10 kHz
- DMD 存储器单元的内置自检 (BIST)

2 应用

- 宽视场和增强现实抬头显示 (HUD)
- 数字仪表组、导航和信息娱乐系统挡风玻璃显示

3 说明

DLP® DLP4620S-Q1 汽车数字微镜器件 (DMD) 与 DLPC230S-Q1 DMD 控制器和 TPS99000S-Q1 系统管理和照明控制器结合使用，能够实现具有高性能、高分辨率的增强现实抬头显示 (HUD)。采用 2:1 宽高比，支持超宽宽高比设计；具有 90 万像素分辨率，可在 HUD 应用实现视网膜级受限显示。DLP4620S-Q1 在光通量和分辨率之间实现了良好的平衡，能够获得宽视野和较大的驾驶员眼动范围，增强用户体验。该芯片组耦合了 LED 或激光和光学系统，能够获得更饱满的 125% NTSC 色彩、超过 15,000cd/m2 的超高亮度、超过 5000:1 的高动态调光比以及太阳能高负载容差。DLP4620S-Q1 汽车 DMD 微镜阵列针对底部照明而配置，可实现高效及更紧凑的光学引擎设计，以支持左舵和右舵驾驶员配置。DLP4620S-Q1 器件采用面板封装，可优化系统成本。该封装针对 DMD 阵列而言具有低热阻的特点，可实现高效的散热解决方案。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
DLP4620S-Q1	FQX	25.2 mm × 11.0 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

DLP4620S-Q1 DLP® 芯片组系统方框图

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English Data Sheet: DLPS230

ADVANCE INFORMATION

Table of Contents

4 Revision History

Changes from Revision * (December 2022) to Revision A (February 2023)   **Page**

![Texas Instruments logo]

5 Pin Configuration and Functions
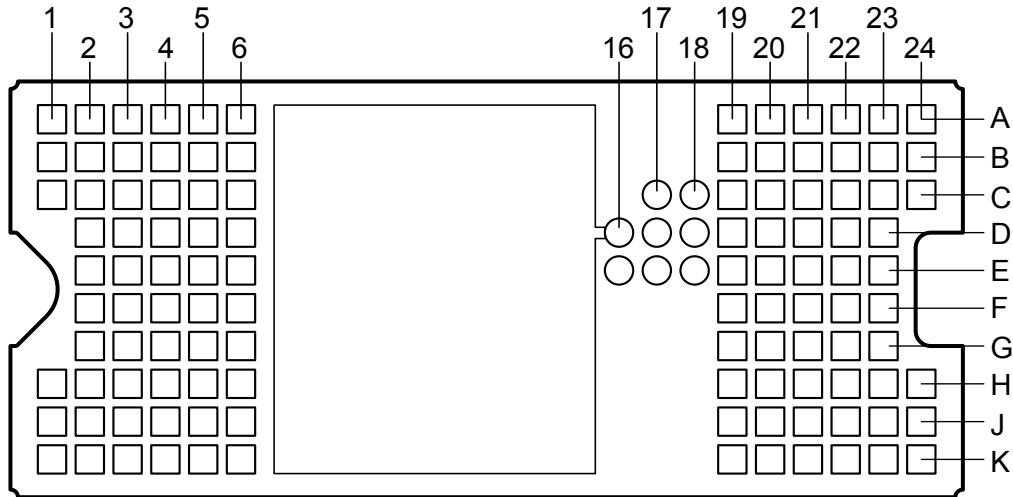
图 5-1. FQX Package 120-Pin LGA Bottom View

表 5-1. Pin Functions—Connector Pins

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(0)	A3	I	SubLVDS	Double	Data, Negative
D_AN(1)	B1	I	SubLVDS	Double	Data, Negative
D_AN(2)	C2	I	SubLVDS	Double	Data, Negative
D_AN(3)	F2	I	SubLVDS	Double	Data, Negative
D_AN(4)	H2	I	SubLVDS	Double	Data, Negative
D_AN(5)	K1	I	SubLVDS	Double	Data, Negative
D_AN(6)	K4	I	SubLVDS	Double	Data, Negative
D_AN(7)	K6	I	SubLVDS	Double	Data, Negative
D_AP(0)	A2	I	SubLVDS	Double	Data, Positive
D_AP(1)	C1	I	SubLVDS	Double	Data, Positive
D_AP(2)	D2	I	SubLVDS	Double	Data, Positive
D_AP(3)	E2	I	SubLVDS	Double	Data, Positive
D_AP(4)	G2	I	SubLVDS	Double	Data, Positive
D_AP(5)	K2	I	SubLVDS	Double	Data, Positive
D_AP(6)	K3	I	SubLVDS	Double	Data, Positive
D_AP(7)	K5	I	SubLVDS	Double	Data, Positive
D_BN(0)	A22	I	SubLVDS	Double	Data, Negative
D_BN(1)	B24	I	SubLVDS	Double	Data, Negative
D_BN(2)	D23	I	SubLVDS	Double	Data, Negative
D_BN(3)	F23	I	SubLVDS	Double	Data, Negative
D_BN(4)	H23	I	SubLVDS	Double	Data, Negative

Product Folder Links: *DLP4620S-Q1*

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表 5-1. Pin Functions—Connector Pins (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_BN(5)	K24	I	SubLVDS	Double	Data, Negative
D_BN(6)	K21	I	SubLVDS	Double	Data, Negative
D_BN(7)	K19	I	SubLVDS	Double	Data, Negative
D_BP(0)	A23	I	SubLVDS	Double	Data, Positive
D_BP(1)	C24	I	SubLVDS	Double	Data, Positive
D_BP(2)	C23	I	SubLVDS	Double	Data, Positive
D_BP(3)	E23	I	SubLVDS	Double	Data, Positive
D_BP(4)	G23	I	SubLVDS	Double	Data, Positive
D_BP(5)	K23	I	SubLVDS	Double	Data, Positive
D_BP(6)	K22	I	SubLVDS	Double	Data, Positive
D_BP(7)	K20	I	SubLVDS	Double	Data, Positive
DCLK_AN	J1	I	SubLVDS	Double	Clock, Negative
DCLK_AP	H1	I	SubLVDS	Double	Clock, Positive
DCLK_BN	J24	I	SubLVDS	Double	Clock, Negative
DCLK_BP	H24	I	SubLVDS	Double	Clock, Positive
LS_CLKN	C3	I	SubLVDS	Single	Clock for Low Speed Interface, Negative
LS_CLKP	C4	I	SubLVDS	Single	Clock for Low Speed Interface, Positive
LS_WDATAN	C5	I	SubLVDS	Single	Write Data for Low Speed Interface, Negative
LS_WDATAP	C6	I	SubLVDS	Single	Write Data for Low Speed Interface, Positive
CONTROL INPUTS					
DMD_DEN_ARSTZ	E6	I	LPSDR		Asynchronous Reset Active Low. Logic High Enables DMD
LS_RDATA_A	E19	O	LPSDR	Single	Read Data for Low Speed Interface
LS_RDATA_B	F19	O	LPSDR	Single	Read Data for Low Speed Interface
TEMPERATURE SENSE DIODE					
TEMP_N	F6	O			Calibrated temperature diode used to assist accurate temperature measurements of DMD die
TEMP_P	G6	I			

Product Folder Links: *DLP4620S-Q1*

表 5-1. Pin Functions—Connector Pins (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
POWER					
VBIAS	A4	Power			Supply voltage for positive bias level at micromirrors
VBIAS	A21	Power			
VOFFSET	B3	Power			Supply voltage for high-voltage CMOS core logic. Supply voltage for offset level at micromirrors
VOFFSET	B4	Power			
VOFFSET	B21	Power			
VOFFSET	B22	Power			
VOFFSET	J4	Power			
VOFFSET	J21	Power			
VRESET	B6	Power			Supply voltage for negative reset level at micromirrors
VRESET	B19	Power			
VDD	A5	Power			Supply voltage for Low Voltage CMOS core logic; for LPSDR inputs; for normal high level at micromirror address electrodes
VDD	A20	Power			
VDD	C20	Power			
VDD	D4	Power			
VDD	D19	Power			
VDD	D21	Power			
VDD	E3	Power			
VDD	E22	Power			
VDD	F4	Power			
VDD	G3	Power			
VDD	G21	Power			
VDD	H22	Power			
VDD	J3	Power			
VDD	J6	Power			
VDD	J19	Power			
VDDI	E5	Power			Supply voltage for SubLVDS receivers
VDDI	E20	Power			
VDDI	F5	Power			
VDDI	F20	Power			
VDDI	G5	Power			
VDDI	G20	Power			
VDDI	H5	Power			
VDDI	H20	Power			

ADVANCE INFORMATION

Product Folder Links: DLP4620S-Q1

表 5-1. Pin Functions—Connector Pins (continued)

| PIN | | TYPE | SIGNAL | DATA RATE | DESCRIPTION |
NAME	NO.				
VSS	A1	Ground			
VSS	A6	Ground			
VSS	A19	Ground			
VSS	A24	Ground			
VSS	B2	Ground			
VSS	B5	Ground			
VSS	B20	Ground			
VSS	B23	Ground			
VSS	C19	Ground			
VSS	C21	Ground			
VSS	C22	Ground			
VSS	D3	Ground			
VSS	D5	Ground			
VSS	D6	Ground			
VSS	D20	Ground			
VSS	D22	Ground			
VSS	E4	Ground			
VSS	E21	Ground			Common return. Ground for all power
VSS	F3	Ground			
VSS	F21	Ground			
VSS	F22	Ground			
VSS	G4	Ground			
VSS	G19	Ground			
VSS	G22	Ground			
VSS	H3	Ground			
VSS	H4	Ground			
VSS	H6	Ground			
VSS	H19	Ground			
VSS	H21	Ground			
VSS	J2	Ground			
VSS	J5	Ground			
VSS	J20	Ground			
VSS	J22	Ground			
VSS	J23	Ground			

ADVANCE INFORMATION

表 5-2. Pin Functions—Test Pads

NUMBER	SYSTEM BOARD
TP0	Do not connect.
TP1	Do not connect.
TP2	Do not connect.
MBRST(0)	Do not connect.
MBRST(1)	Do not connect.
MBRST(6)	Do not connect.
MBRST(7)	Do not connect.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic[1] Supply voltage for LPSDR low speed interface	− 0.5	2.3	V
V_{DDI}	Supply voltage for subLVDS receivers[1]	− 0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode[1] [2]	− 0.5	8.75	V
V_{BIAS}	Supply voltage for micromirror electrode[1]	− 0.5	17	V
V_{RESET}	Supply voltage for micromirror electrode[1]	− 11	0.5	V
$|V_{DDI} - V_{DD}|$	Supply voltage delta (absolute value)[3]		0.3	V
$|V_{BIAS} - V_{OFFSET}|$	Supply voltage delta (absolute value)[4]		8.75	V
$|V_{BIAS} - V_{RESET}|$	Supply voltage delta (absolute value)[5]		28	V
INPUT VOLTAGE				
Input voltage for LVCMOS inputs[1]		− 0.5	V_{DD} + 0.5	V
Input voltage for other inputs subLVDS[1] [6]		− 0.5	V_{DDI} + 0.5	V
INPUT PINS				
$|V_{ID}|$	SubLVDS input differential voltage (absolute value)[6]		810	mV
$|I_{ID}|$	SubLVDS input differential current		10	mA
CLOCK FREQUENCY				
F_{max_LS}	Clock frequency for low speed interface LS_CLK	100	130	MHz
TEMPERATURE DIODE				
I_{TEMP_DIODE}	Max current source into temperature diode		120	μA
ENVIRONMENTAL				
T_{ARRAY}	Operating DMD array temperature	− 40	105	°C

(1) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(2) VOFFSET supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw and permanent damage to the device.
(4) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw and permanent damage to the device.
(5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw and permanent damage to the device.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. SubLVDS differential inputs must not exceed the specified limit or damage to the internal termination resistors may result.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	− 40	125	°C

6.3 ESD Ratings

			VALUE	UNIT
V(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1)   AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode[3]	8.25	8.5	8.75	V
V_{BIAS}	Supply voltage for mirror electrode	15.5	16	16.5	V
V_{RESET}	Supply voltage for micromirror electrode	− 9.5	− 10	− 10.5	V
$|V_{DDI} - V_{DD}|$	Supply voltage delta (absolute value)[4]			0.3	V
$|V_{BIAS}-V_{OFFSET}|$	Supply voltage delta (absolute value)[5]			8.75	V
$|V_{BIAS} - V_{RESET}|$	Supply voltage delta (absolute value)[6]			28	V
LOW-SPEED LPDSR INTERFACE					
f_{clock_LS}	Clock frequency for low speed interface LS_CLK	108		120	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK)	44		56	%
SUBLVDS INTERFACE					
f_{clock_HS}	Clock frequency for high-speed interface DCLK	300		540	MHz
DCD_{IN}	LVDS duty cycle distortion (DCLK)	44		56	%
$|V_{ID}|$	LVDS differential input voltage magnitude[7]	150	250	350	mV
V_{CM}	Common mode voltage[7]	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage[7]	525		1275	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance[8]	80	100	120	Ω
	100-Ω differential PCD trace	6.35		152.4	mm
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature[9] [11]	-40		105	°C
Illumination					
ILL_{UV}	Illumination, wavelength < 395 nm[10]			2	mW/cm²
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in area shown in Figure 6-1			90	mW/mm²

(1)   Recommended Operating Conditions are applicable after the DMD is installed in the final product.
(2)   The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(3)   VOFFSET supply transients must fall within specified min/max voltages.
(4)   To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than the specified limit.
(5)   To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than the specified limit.
(6)   To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than the specified limit.
(7)   See Figure 6-6 and Figure 6-7.
(8)   See Figure 6-8.
(9)   DMD Active Array temperature can be calculated as shown in the *Micromirror Array Temperature Calculation*.
(10)   The maximum operation conditions for operating temperature and UV illumination must not be implemented simultaneously.
(11)   The operating profile information for the device micromirror landed duty-cycle and temperature is provided upon request.
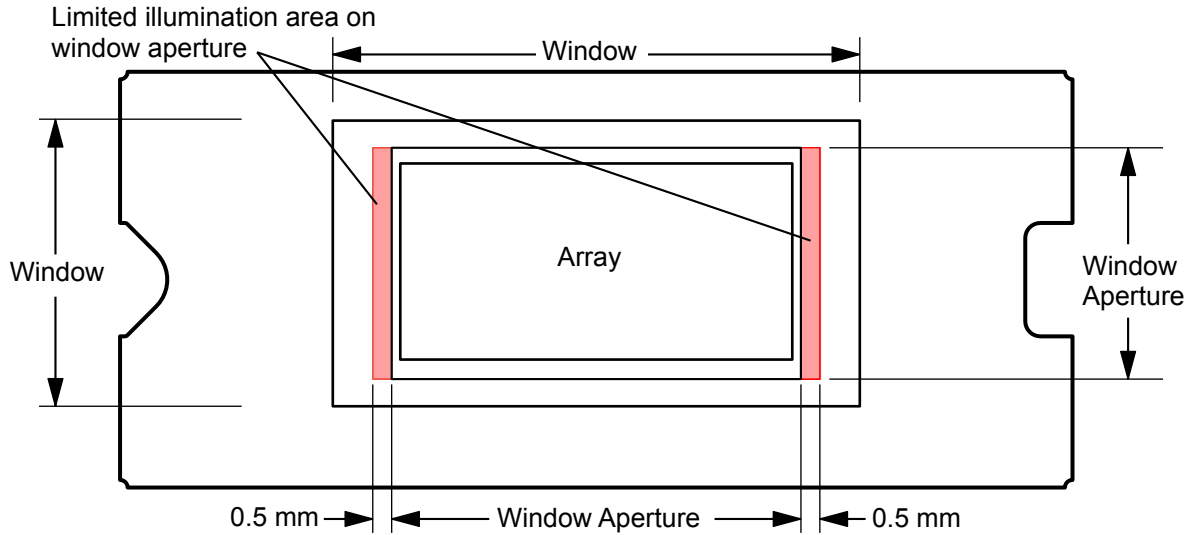
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Product Folder Links: *DLP4620S-Q1*

6.4.1 Illumination Overfill Diagram

图 6-1. Illumination Overfill Diagram

6.5 Thermal Information

THERMAL METRIC		DLP4620S-Q1 FQX	UNIT
Thermal resistance	Active area-to-test point 1 (TP1) [1]	1.3	°C/W
Thermal resistance	Active area-to-temperature sense diode [1]	0.1	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions* . The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD[2]	VDD = 1.95 V			220	mA
I_{DDI}	Supply current: VDDI[2]	VDDI = 1.95 V			55	mA
I_{OFFSET}	Supply current: VOFFSET	VOFFSET = 8.75 V			35	mA
I_{BIAS}	Supply current: VBIAS	VBIAS = 16.5 V			1.5	mA
I_{RESET}	Supply current: VRESET	VRESET = – 10.5 V			16	mA
POWER						
P_{DD}	Supply power dissipation: VDD[2]	VDD = 1.95 V			430	mW
P_{DDI}	Supply power dissipation: VDDI[2]	VDDI = 1.95 V			108	mW
P_{OFFSET}	Supply power dissipation: VOFFSET	VOFFSET = 8.75 V			307	mW
P_{BIAS}	Supply power dissipation: VBIAS	VBIAS = 16.5 V			25	mW
P_{RESET}	Supply power dissipation: VRESET	VRESET = – 10.5 V			168	mW
P_{TOTAL}	Supply power dissipation: total				1038	mW
LVCMOS INPUT						

Product Folder Links: **DLP4620S-Q1**

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage[3]		$0.7 \times V_{DD}$		$V_{DD} + 0.3$	V
V_{IL}	Low-level input voltage[3]		-0.3		$0.3 \times V_{DD}$	V
$V_{IH(AC)}$	AC input high voltage[3]		$0.8 \times V_{DD}$		$V_{DD} + 0.3$	V
$V_{IL(AC)}$	AC input low voltage[3]		-0.3		$0.2 \times V_{DD}$	V
V_{Hyst}	Input hysteresis[3]	See Figure 6-9	$0.1 \times V_{DD}$		$0.4 \times V_{DD}$	V
I_{IL}	Low-level input current[3]	VDD = 1.95 V; V_I = 0 V	-100			nA
I_{IH}	High-level input current[3]	VDD = 1.95 V; V_I = 1.95 V			135	µ A
LVCMOS OUTPUT						
V_{OH}	DC output high voltage[4]	$I_{OH} = -2$ mA	$0.8 \times V_{DD}$			V
V_{OL}	DC output low voltage[4]	$I_{OL} = 2$ mA			$0.2 \times V_{DD}$	V
I_{OZ}	High impedance output current	VDD = 1.95 V			10	µA
CAPACITANCE						
C_{IN}	Input capacitance LVCMOS	F = 1 MHz			10	pF
	Input capacitance subLVDS	F = 1 MHz			20	pF
C_{OUT}	Output capacitance	F = 1 MHz			10	pF
C_{TEMP}	Input capacitance subLVDS	F = 1 MHz			20	pF

(1)   Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2)   Supply power dissipation based on non-compressed commands and data.
(3)   LPSDR input specifications are for pin DMD_DEN_ARSTZ.
(4)   LPSDR output specification is for pins LS_RDATA_A and LS_RDATA_B.

6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted

			MIN	NOM	MAX	UNIT
Low-Speed Interface						
t_r	Rise slew rate [1] [2]	(20% to 80%) × VDD	0.25			V/ns
t_f	Fall slew rate [1] [2]	(80% to 20%) × VDD	0.25			V/ns
t_c	Cycle time LS_CLK			7.7	8.3	ns
$t_{W(H)}$	Pulse duration LS_CLK high[3]	50% to 50% reference points	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low[3]	50% to 50% reference points	3.1			ns
t_{su}	Setup time[3]	LS_WDATA valid before LS_CLK ↑ or LS_CLK ↓	1.5			ns
t_h	Hold time[3]	LS_WDATA valid after LS_CLK ↑ or LS_CLK ↓	1.5			ns
t_{WINDOW}	Window time	Setup time + hold time	3			ns
$t_{DERATING}$	Window time derating	For each 0.25 V/ns reduction in slew rate below 1 V/ns		0.35		ns
High-Speed Interface						
t_r	Rise slew rate[2]	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate[2]	80% to 20% reference points	0.7	1		V/ns
t_c	Cycle time DCLK [3]			1.79	1.85	ns
$t_{W(H)}$	Pulse duration DCLK high[3]	50% to 50% reference points	0.79			ns

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6.7 Timing Requirements (continued)

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted

			MIN	NOM	MAX	UNIT
$t_{W(L)}$	Pulse duration DCLK low[3]	50% to 50% reference points	0.79			ns
t_{WINDOW}	Window time[3] [4]	Setup time + Hold time	0.3			ns
$t_{LVDS-EN+REFGEN}$	Power-up receiver [5]				2000	ns

(1)   Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 6-2.
(2)   See Figure 6-3.
(3)   See Figure 6-4.
(4)   See Figure 6-5.
(5)   Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.

Electrical and Timing Diagrams
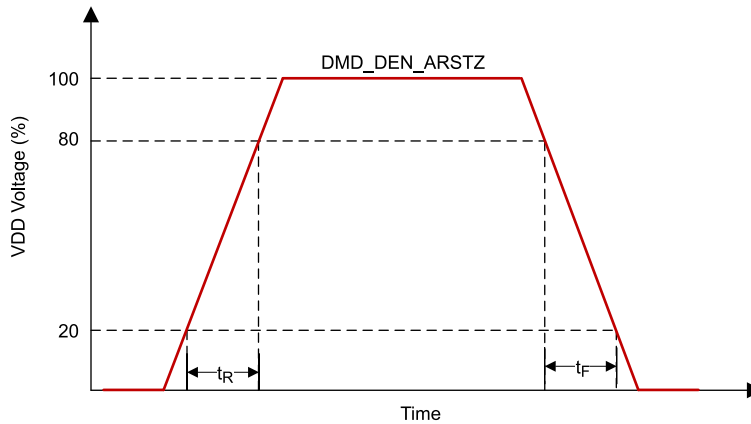
图 **6-2. LPSDR Input Rise and Fall Slew Rate**
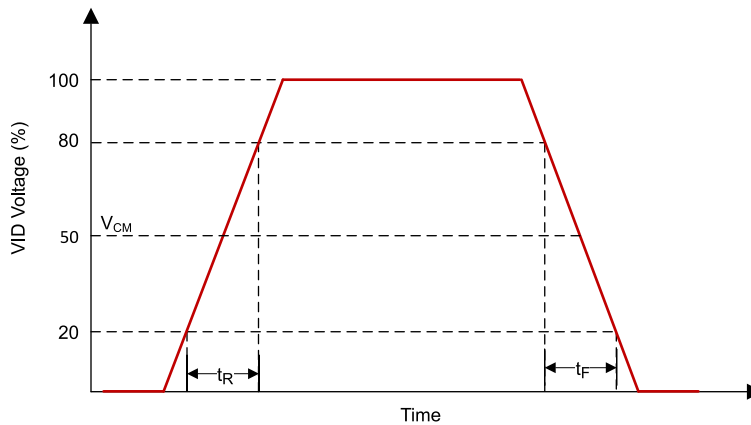
图 **6-3. SubLVDS Input Rise and Fall Slew Rate**

Product Folder Links: *DLP4620S-Q1*

ADVANCE INFORMATION
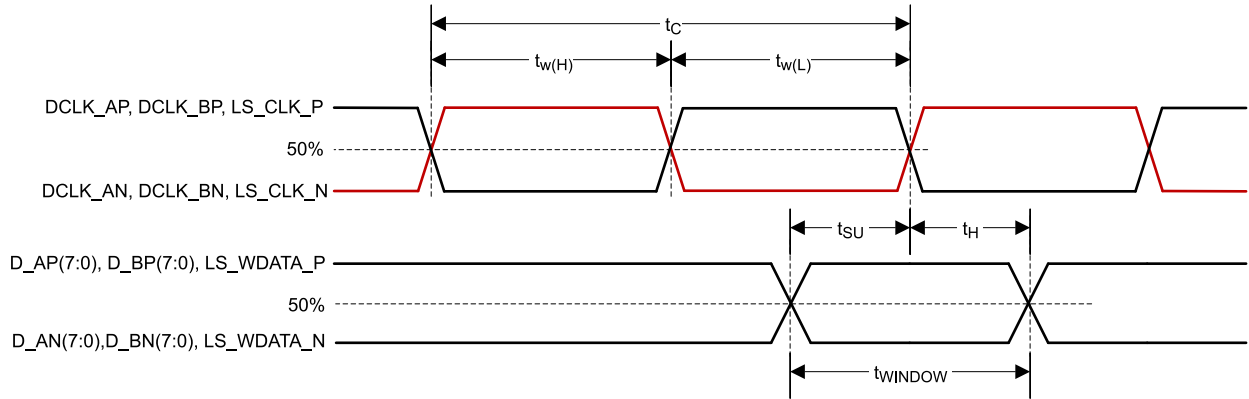
图 6-4. SubLVDS Switching Parameters
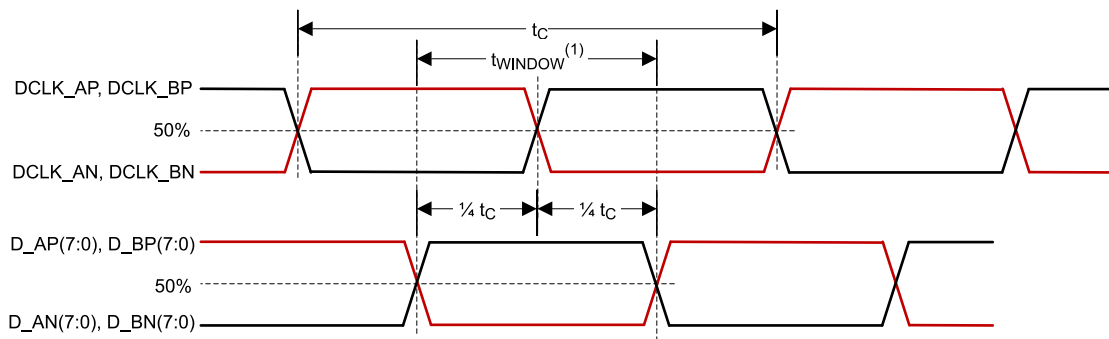
(1) High-speed training scan window

图 6-5. High-Speed Training Scan Window
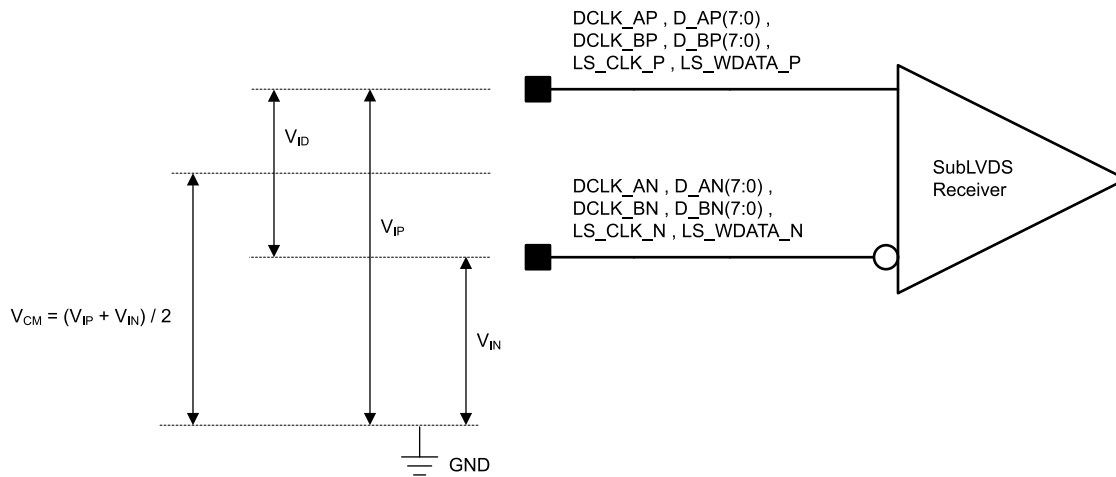
图 6-6. SubLVDS Voltage Parameters
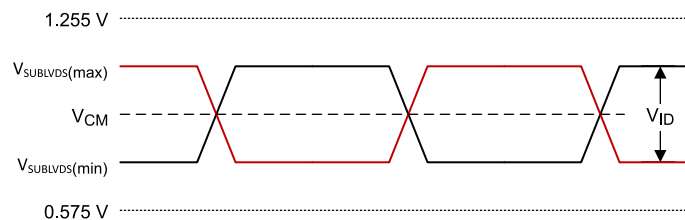
图 6-7. SubLVDS Waveform Parameters

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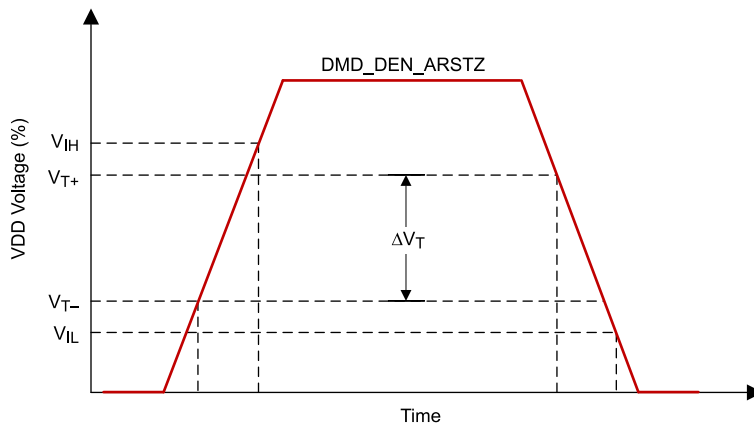**ADVANCE INFORMATION**
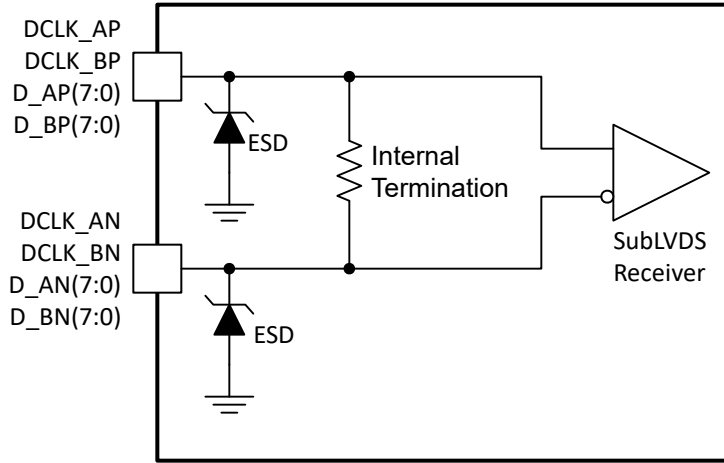
图 **6-8. SubLVDS Equivalent Input Circuit**

图 **6-9. LPSDR Input Hysteresis**

6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output[2]	$C_L = 45$ pF			15	ns
	Slew rate, LS_RDATA			0.5		V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B		40%		60%	

(1)   Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

(2)   See 图 6-10 and 图 6-11.

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6.8.1 LPSDR and Test Load Circuit Diagrams
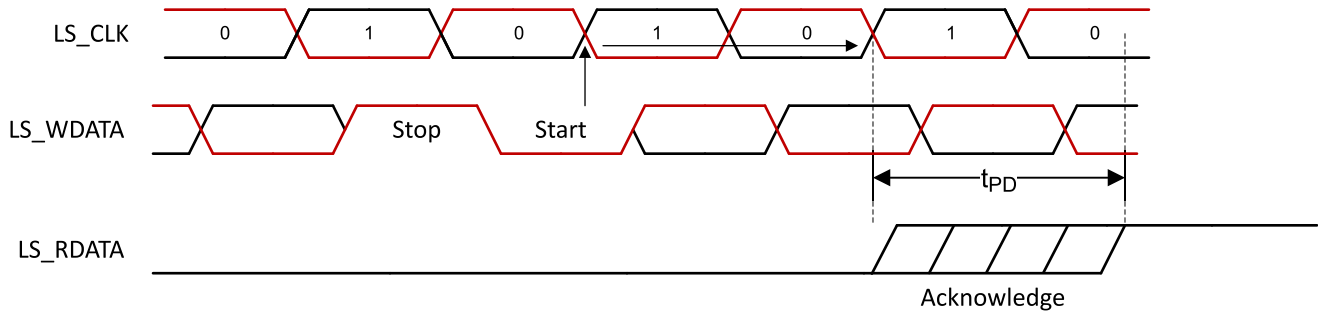
图 **6-10. LPSDR Read Out**
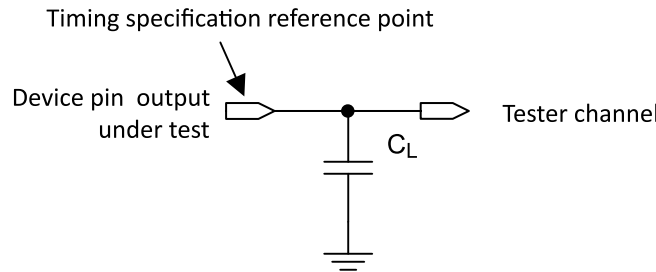
图 **6-11. Test Load Circuit for Output Propagation Measurement**

6.9 System Mounting Interface Loads

PARAMETER	Condition	MIN	NOM	MAX	UNIT
Thermal interface area	Maximum load uniformly distributed within each area[1]			90	N
Electrical interface area	Maximum load uniformly distributed within each area[1]			135	

(1)   See Figure 6-12.

System Interface Loads Diagram
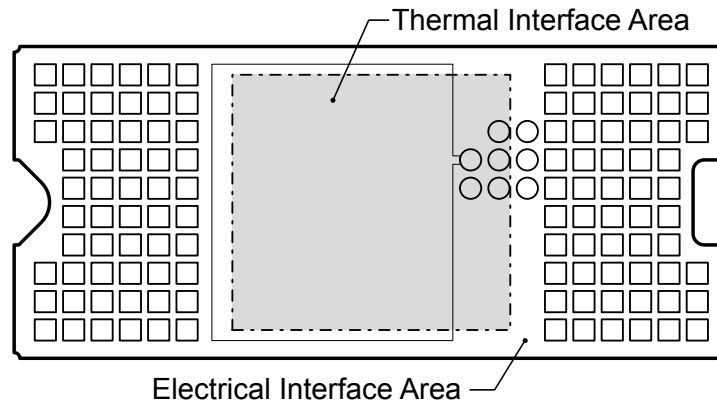
图 **6-12. System Interface Loads**

6.10 Physical Characteristics of the Micromirror Array

	PARAMETER		VALUE	UNIT
M	Number of active columns[1]		960	micromirrors
N	Number of active rows[1]		960	micromirrors
ε	Micromirror (pixel) pitch—diagonal[1]		7.6	μm
P	Micromirror (pixel) pitch—horizontal and vertical[1]		10.8	μm

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6.10 Physical Characteristics of the Micromirror Array (continued)

PARAMETER		VALUE	UNIT
Micromirror active array width	(P × M) + (P / 2)	10.373	mm
Micromirror active array height	(P x N) / 2 + (P / 2)	5.189	mm
Micromirror active border	Pond of micromirrors (POM) [2]	10	micromirrors/side

(1) See 图 6-13.

(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

6.10.1 Array Physical Characteristics Diagram
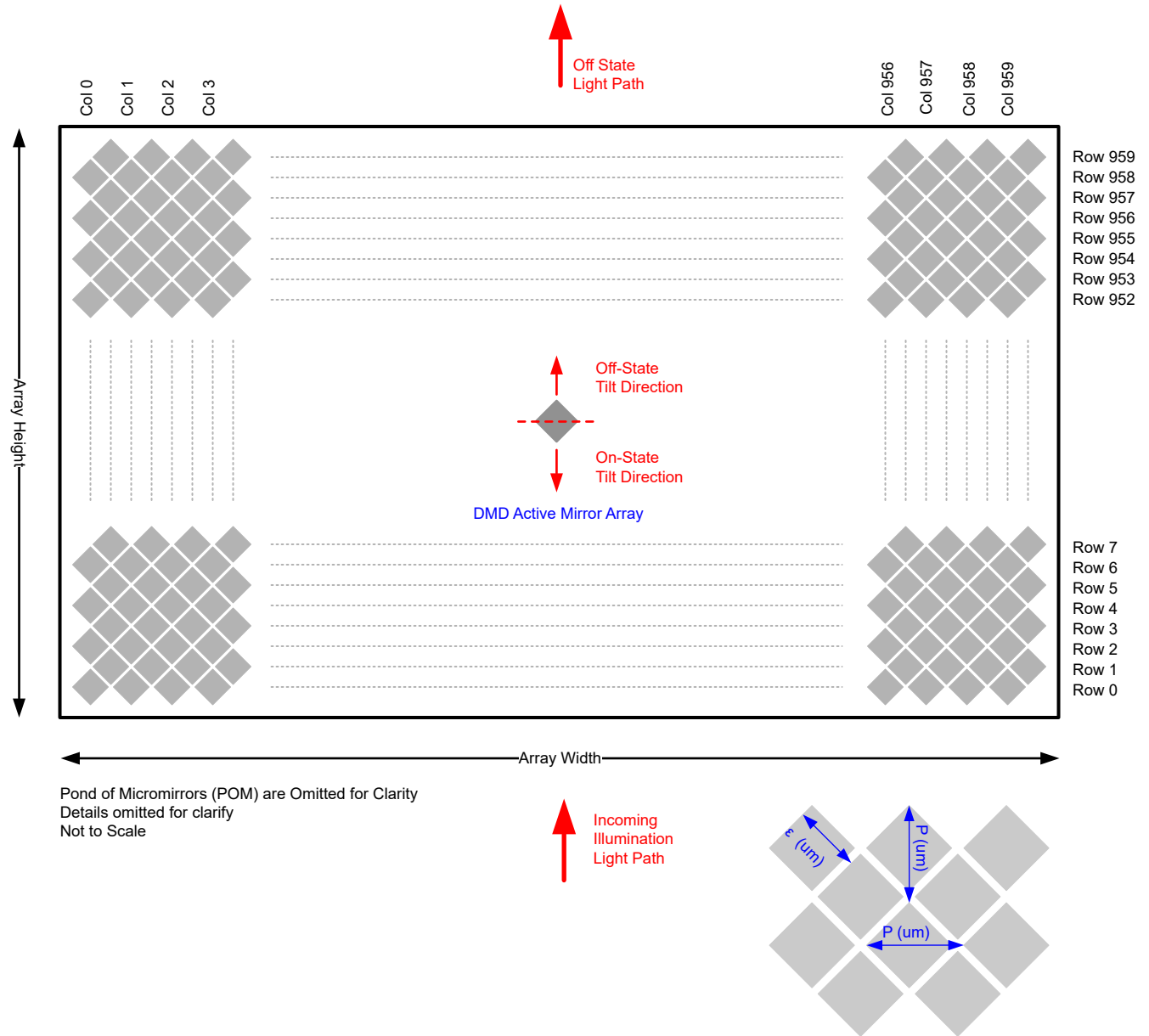
图 6-13. Micromirror Array Physical Characteristics

Product Folder Links: DLP4620S-Q1

6.11 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state[1]		12		degree
Micromirror tilt angle tolerance[2]		– 1		1	degree
DMD efficiency[3]	420 nm – 700 nm		66%		

(1) Measured relative to the plane formed by the overall micromirror array at 25°C.

(2) For some applications, it is critical to account for the micromirror tilt angle variation in the overall optical system design. With some optical system designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some optical system designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.

(3) DMD efficiency is measured photopically under the following conditions: 24° illumination angle, F/2.4 illumination and collection apertures, uniform source spectrum (halogen), uniform pupil illumination, the optical system is telecentric at the DMD, and the efficiency numbers are measured with 100% electronic micromirror landed duty-cycle and do not include system optical efficiency or overfill loss. This number is measured under conditions described above and deviations from these specified conditions could result in a different efficiency value in a different optical system. The factors that can influence the DMD efficiency related to system application include: light source spectral distribution and diffraction efficiency at those wavelengths (especially with discrete light sources such as LEDs or lasers), and illumination and collection apertures (F/#) and diffraction efficiency. The interaction of these system factors as well as the DMD efficiency factors that are not system dependent are described in detail in *DMD Optical Efficiency for Visible Wavelengths Application Note*.

6.12 Window Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	At wavelength 546.1 nm		1.5119		
Window aperture[1]				See [1].	
Illumination overfill				See [1].	

(1) See the mechanical package ICD for details regarding the size and location of the window aperture.

6.13 Chipset Component Usage Specification

The DLP4620S-Q1 is a component of a chipset. Reliable function and operation of the DLP4620S-Q1 requires that it be used in conjunction with the TPS99000S-Q1 and DLPC230S-Q1, and includes components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

备注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

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7 Detailed Description

7.1 Overview

The DLP4620S-Q1 automotive DMD consists of 921600 highly reflective, digitally switchable, micrometer-sized mirrors organized in a two-dimensional array. As shown in Figure 6-13, the micromirror array consists of 960 micromirror columns × 960 micromirror rows in a diamond pixel configuration with a 2:1 aspect ratio.

Around the perimeter of the 960 × 960 array of micromirrors is a uniform band of border micromirrors called the Pond of Micromirrors (POM). The border micromirrors are not user-addressable. The border micromirrors land in the – 12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 960 × 960 active array.

Due to the diamond pixel configuration, the columns of each odd row are offset by half a pixel from the columns of the even row. Each mirror is switchable between two discrete angular positions: – 12° and +12°. The mirrors are illuminated from the bottom which allows for compact and efficient system optical design.

Although the native resolution of the DLP4620S-Q1 is 960 × 960 with an aspect ratio of 2:1, when paired with the DLPC230S-Q1 controller, the DLP4620S-Q1 can be driven with different resolutions. For example, a Head-Up Display system can use a resolution of 960 × 480 or 1920 × 960 with external quincunx processing before the DLPC230S-Q1. The DLPC230S-Q1 can also support resolutions of 1220x610 and 1358 × 566 which are displayed as 864 × 864 and 960 × 800 sub-images on the 960 × 960 DLP4620S-Q1, respectively. The table below summarizes the resolution options.

表 **7-1. DLP4620S-Q1 Resolution Options**

INPUT MANHATTAN RESOLUTION	EXTERNAL VIDEO PROCESSING REQUIRED	DMD DIAMOND MIRRORS USED
960 × 480	No	960 × 960
1220 × 610	No	864 × 864 (sub-image)
1358 × 566	No	960 × 800 (sub-image)
1920 × 960	Yes: Quincunx	960 × 960

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7.2 Functional Block Diagram

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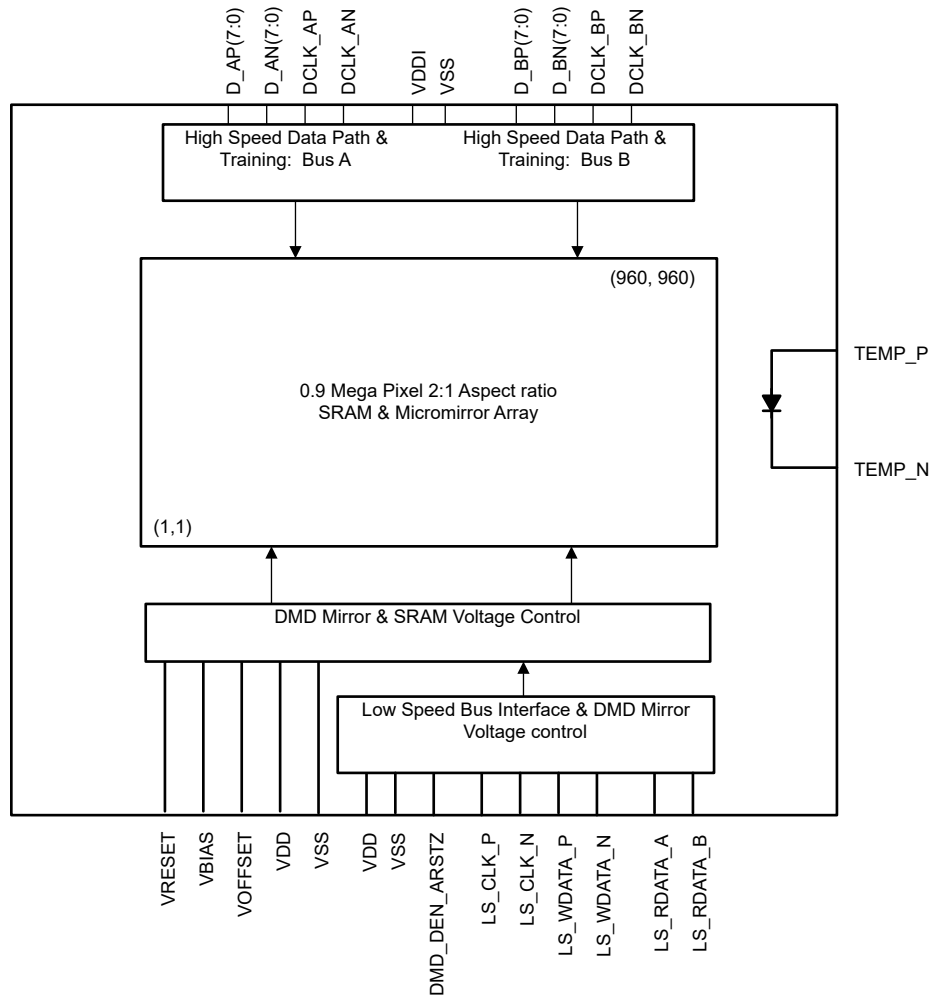
7.3 Feature Description

The DLP4620S-Q1 consists of a two-dimensional array of 1-bit CMOS memory cells driven by a subLVDS bus from the DLPC230S-Q1 and powered by the TPS99000S-Q1. The temperature sensing diode is used to continuously monitor the DMD array temperature.

To ensure reliable operation, the DLP4620S-Q1 must be used with the DLPC230S-Q1 DMD display controller and the TPS99000S-Q1 system management and illumination controller.

7.3.1 SubLVDS Data Interface

The subLVDS signaling protocol was designed to enable very fast DMD data refresh rates while simultaneously maintaining low power and low emission.

Data is loaded into the SRAM under each micromirror using the subLVDS interface from the DLPC230S-Q1. This interface consists of 16 pairs of differential data signals plus two clock pairs into two separate buses A and B loading the left and right half of the SRAM array. The data is latched on both transitions creating a double data rate (DDR) interface. The subLVDS interface also implements a continuous training algorithm to optimize the data and clock timing to allow for a more robust interface.

The entire DMD array of 0.9 million pixels can be updated at a rate of less than 100 μs as a result of the high speed subLVDS interface.

7.3.2 Low Speed Interface for Control

The purpose of the low speed interface is to configure the DMD at power up and power down and to control the micromirror reset voltage levels that are synchronized with the data loading. The micromirror reset voltage controls the time when the mirrors are mechanically switched. The low speed differential interface includes two pairs of signals for write data and clock, and two single-ended signals for output (A and B).

7.3.3 DMD Voltage Supplies

The micromirrors require unique voltage levels to control the mechanical switching from –12° to +12°. These voltage levels are nominally 16 V, 8.5 V, and –10 V (VBIAS, VOFFSET, and VRESET), and are generated by the TPS99000S-Q1.

7.3.4 Asynchronous Reset

Reset of the DMD is required and controlled by the DLPC230S-Q1 via the signal DMD_DEN_ARSTZ.

7.3.5 Temperature Sensing Diode

The DMD includes a temperature sensing diode designed to be used with the TMP411 temperature monitoring device. The DLPC230S-Q1 monitors the temperature sense diode via the TMP411. The DLPC230S-Q1 operation of the DMD timing can be adjusted based on the DMD array temperature, therefore this connection is essential to ensure reliable operation of the DMD.

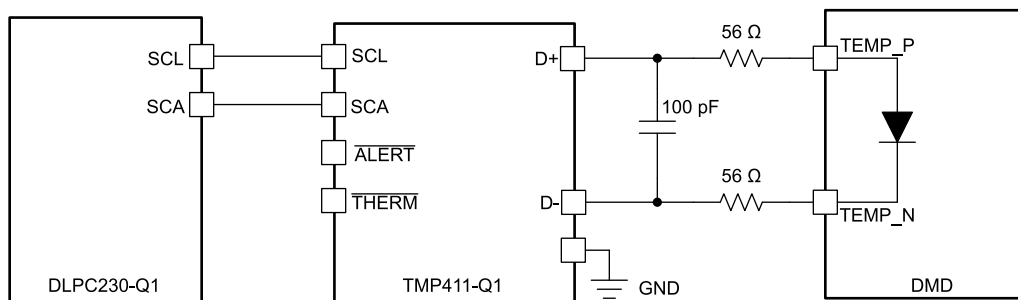图 7-1 shows the typical connection between the DLPC230S-Q1, TMP411, and the DMD.

图 7-1. Temperature Sense Diode Typical Circuit Configuration

7.3.5.1 Temperature Sense Diode Theory

A temperature sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Three different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in their base‑emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the TMP411-Q1 data sheet for detailed information about temperature diode theory and measurement. 图 7-2 and 图 7-3 illustrate the relationships between the current and voltage through the diode.
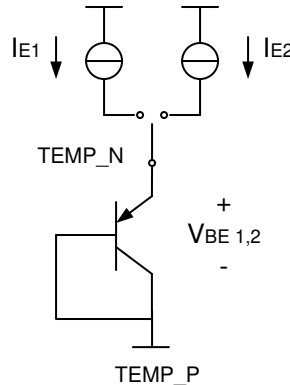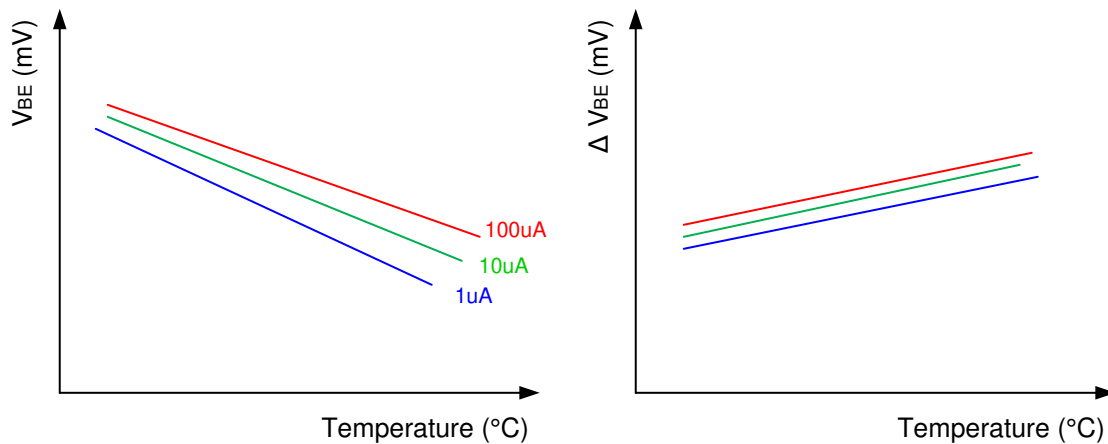
图 7-2. Temperature Measurement Theory

图 7-3. Example of Delta VBE Versus Temperature

7.4 System Optical Considerations

Optimizing system optical performance and image performance strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.4.1 Numerical Aperture and Stray Light Control

The numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This cone angle defined by the numerical aperture should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines the DMD's capability to separate the "On" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces.

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7.4.2 Pupil Match

TI＇s optical and image performance specifications assume that the exit pupil of the illumination optics is nominally centered and located at the entrance pupil position of the projection optics. Misalignment of pupils between the illumination and projection optics can degrade screen image uniformity and cause objectionable artifacts in the display＇s border and/or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.4.3 Illumination Overfill

Overfill light illuminating the area outside the active array can create artifacts from the mechanical features and other surfaces that surround the active array. These artifacts may be visible in the projected image. The illumination optical system should be designed to minimize light flux incident outside the active array and on the window aperture. Depending on the particular system＇s optical architecture and assembly tolerances, this amount of overfill light on the area outside of the active array may still cause artifacts to be visible.

Illumination light and overfill can also induce undesirable thermal conditions on the DMD, especially if illumination light impinges directly on the DMD window aperture or near the edge of the DMD window. Heat load on the aperture in the areas shown in 图 6-1 should not exceed the values listed in *Recommended Operating Conditions*. This area is a 0.5-mm wide area and length of the aperture opening. The values listed in *Recommended Operating Conditions* assume a uniform distribution. For a non-uniform distribution please contact TI for additional information.

备注

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED PREVIOUSLY.

7.5 DMD Image Performance Specification

表 7-2. DMD Image Performance

PARAMETER[1] [2]	MIN	NOM	MAX	UNIT
Dark Blemishes—Viewed on a linear blue 60 screen[3]			4	
Light Blemishes—Viewed on a linear gray 10 screen.			4	
Bright Pixels—Viewed on a linear gray 10 screen.			0	micromirrors
Dark Pixels—Viewed on a white screen			4	micromirrors

(1) See the *System Optical Considerations* section.
(2) Blemish counts do not include reflections or shadows of the same artifact. Any artifact that is not specifically called out in this table is acceptable. Viewing distance must be > 60 in. Screen size should be similar to application image size. All values referenced are in linear gamma. Non-linear gamma curves may be running by default, and it should be ensured with a TI applications engineer that the equivalent linear gamma value as specified is used to judge artifacts.
(3) Linear gray 5 may be substituted in monochrome applications.

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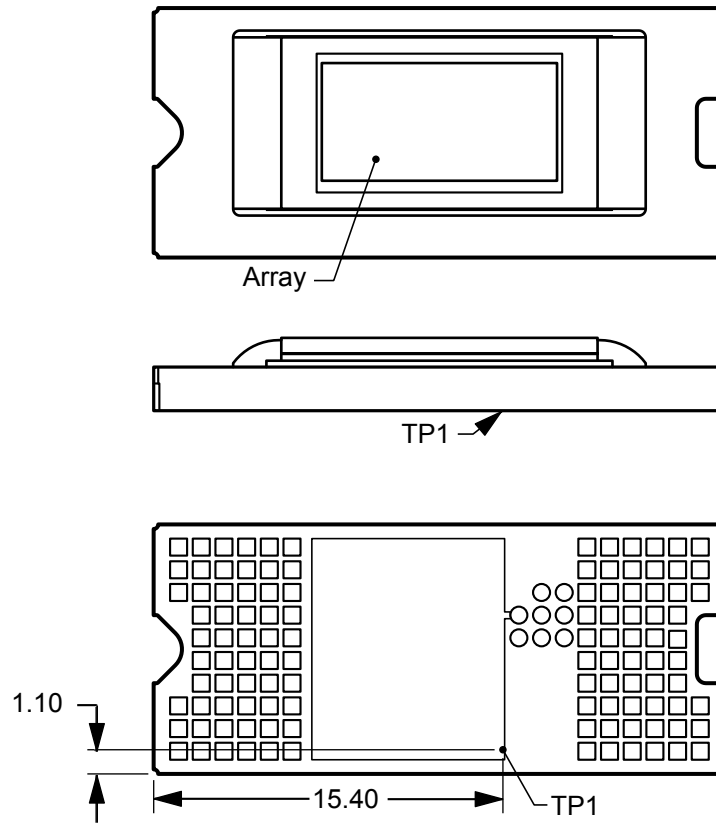## 7.6 Micromirror Array Temperature Calculation

图 7-4. DMD Thermal Test Points

The active array temperature can be computed analytically from the thermal measurement point on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (TP1) in Figure 7-4 is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \tag{1}$$

$$Q_{ILLUMINATION} = (Q_{INCIDENT} \times DMD\ Absorption\ Constant) \tag{2}$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \tag{3}$$

where

- T_{ARRAY} = computed array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature at the TP1 location in DMD Thermal Test Points (°C)
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to thermal test point TP1 (°C/W),
- Q_{ARRAY} = total power (electrical plus absorbed) on the DMD array (W)
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (W)
- $Q_{ILLUMINATION}$ = absorbed illumination heat load (W)
- $Q_{INCIDENT}$ = incident power on the DMD (W)

The DMD absorption constant is a function of illumination distribution on the active array and the array border, angle of incidence (AOI), f number of the system, and operating state of the mirrors. The absorption constant is higher in the OFF state than in the ON state. Equations to calculate the absorption constant are provided for

both ON and OFF mirror states. They assume an AOI of 34 degrees, an f/1.7 system, and they account for the distribution of light on the active array, POM, and array border.

DMD Absorption Constant (OFF state) = 0.895 – 0.004783 × (% of light on ActiveArray + POM)   (4)

DMD Absorption Constant (ON state) = 0.895 – 0.007208 × (% of light on ActiveArray + POM)   (5)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies.

The following sample calculations assume 10% of the total incident light falls outside of the active array and POM, and the mirrors are in the OFF state.

1. $T_{CERAMIC}$ = 50°C (measured)
2. $Q_{INCIDENT}$ = 10 W (measured)
3. DMD Absorption Constant = 0.895 – 0.004783 × 90 = 0.46
4. $Q_{ELECTRICAL}$ = 0.4 W
5. $R_{ARRAY-TO-CERAMIC}$ = 1.3°C/W
6. Q_{ARRAY} = 0.4 W + (0.46 x 10 W) = 5 W
7. T_{ARRAY} = 50°C x (5 W x 1.3°C/W) = 56.5°C

When designing the DMD heatsink solution, the package thermal resistance from array to reference ceramic temperature (thermocouple location TP1 can be used to determine the temperature rise through the package as given by the following equations:

$$T_{ARRAY\text{-}TO\text{-}CERAMIC} = Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}$$ (6)

7.6.1 Monitoring Array Temperature Using the Temperature Sense Diode

The active array temperature can be computed analytically from the temperature sense diode measurement, the thermal resistance from array to diode, the electrical power, and the illumination heat load. The relationship between array temperature and the temperature sense diode is provided by the following equations:

$$T_{ARRAY} = T_{DIODE} + (Q_{ARRAY} \times R_{ARRAY-TO-DIODE})$$ (7)

$$Q_{ILLUMINATION} = (Q_{INCIDENT} \times DMD\ Absorption\ Constant)$$ (8)

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$ (9)

where

- T_{ARRAY} = computed array temperature (°C)
- T_{DIODE} = measured temperature sense diode temperature (°C)
- $R_{ARRAY-TO-DIODE}$ = package thermal resistance from array to diode (°C/W)
- Q_{ARRAY} = total power, electrical plus absorbed, on the DMD array (W)
  Refer to Section 7.6 for details.
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (W)
- $Q_{ILLUMINATION}$ = absorbed illumination heat load (W)
- $Q_{INCIDENT}$ = incident power on the DMD (W)

The temperature sense diode to array thermal resistance ($R_{ARRAY-TO-DIODE}$) assumes a uniform illumination distribution on the DMD.

The following sample calculations assume 10% of the total incident light falls outside of the active array and POM, and the mirrors are in the OFF state.

1. T_{DIODE} = 55°C/W
2. $Q_{INCIDENT}$ = 10 W (measured)
3. DMD Absorption Constant = 0.895 – 0.004783 × 90 = 0.46
4. $Q_{ELECTRICAL}$ = 0.4 W

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5. $R_{ARRAY-TO-DIODE}$ = 0.1°C/W
6. Q_{ARRAY} = 0.4 W + (0.46 × 10 W) = 5 W
7. T_{ARRAY} = 55°C + (5 W × 0.1°C/W) = 55.5°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time), whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

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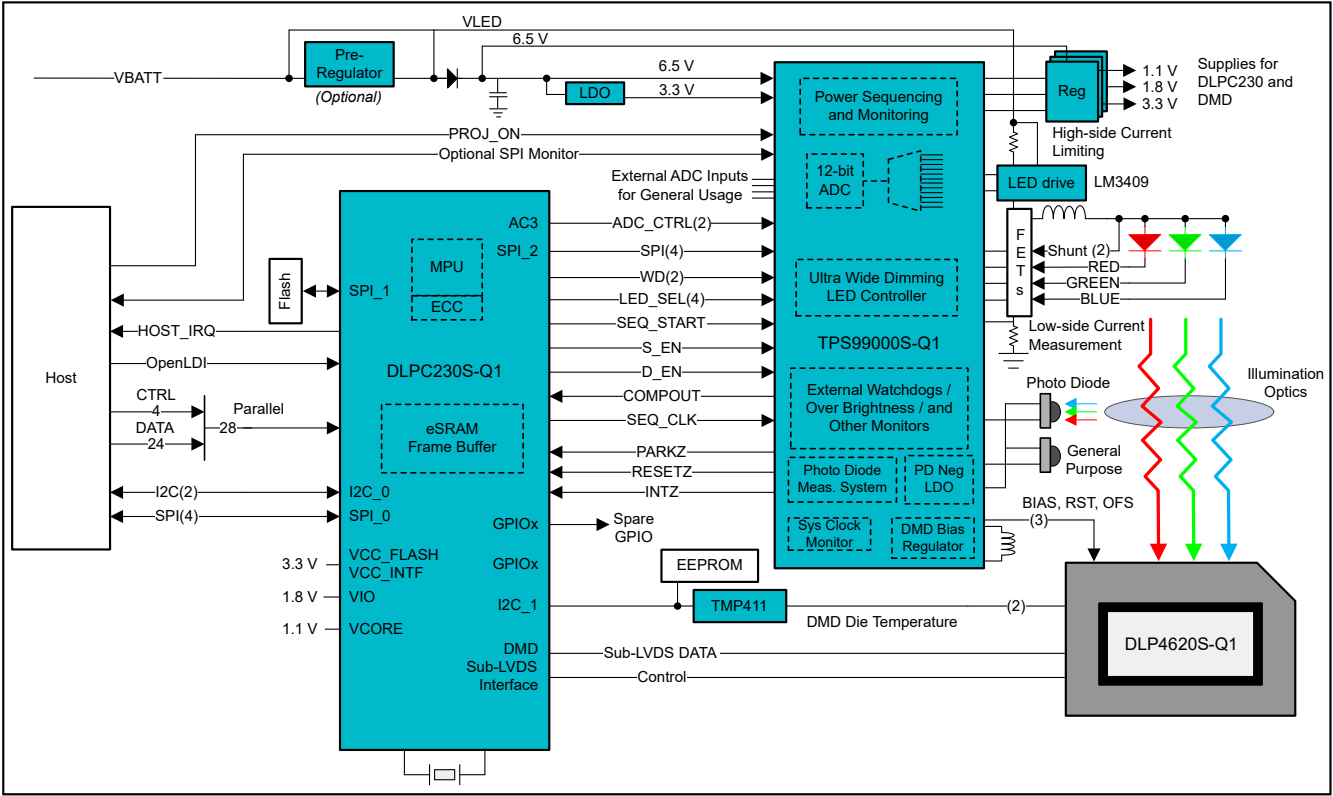
8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DLP4620S-Q1 chipset is designed to support projection-based automotive applications such as s head-up display systems.

8.2 Typical Application

The chipset consists of three components—the DLP4620S-Q1 automotive DMD, the DLPC230S-Q1, and the TPS99000S-Q1. The DMD is a light modulator consisting of tiny mirrors that are used to form and project images. The DLPC230S-Q1 is a controller for the DMD; it formats incoming video and controls the timing of the DMD illumination sources and the DMD in order to display the incoming video. The TPS99000S-Q1 is a high performance voltage regulator for the DMD, a controller for the illumination sources (e.g. LEDs or lasers) and a management IC for the entire chipset. In conjunction, the DLPC230S-Q1 and the TPS99000S-Q1 can be used for system-level monitoring, diagnostics, and failure detection features. 图 8-1 is a system level block diagram with these devices in the DLP head-up display configuration and displays the primary features and functions of each device.
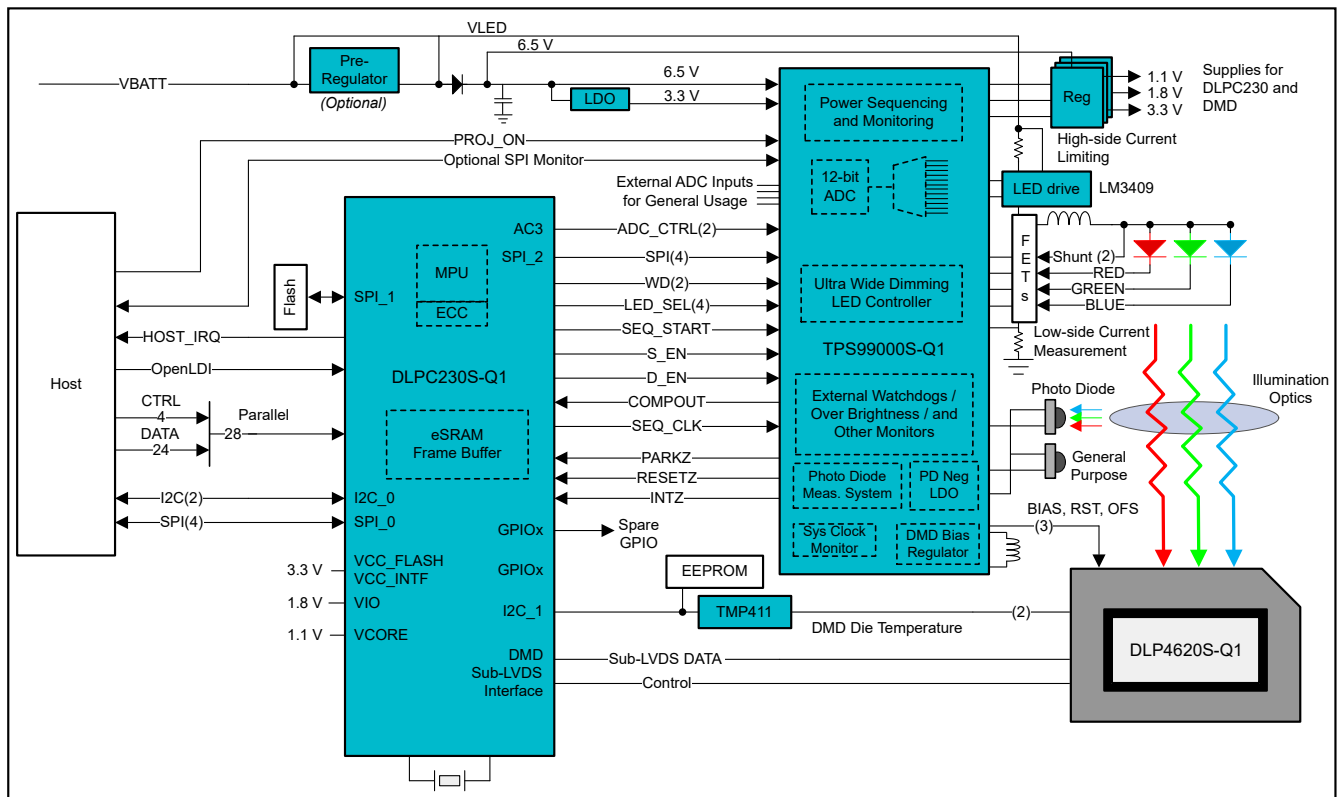

图 8-1. HUD System Block Diagram

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8.2.1 Application Overview

图 8-1 shows the system block diagram for a DLP HUD module. The system uses the DLPC230S-Q1, TPS99000S-Q1, and the DLP4620S-Q1 automotive DMD to enable a head-up display with high brightness, high efficiency, and a large virtual image distance. The combination of the DLPC230S-Q1 and TPS99000S-Q1 removes the need for external SDRAM and a dedicated microprocessor. The chipset manages the illumination control of LED sources, power sequencing functions, and system management functions. Additionally, the chipset supports numerous system diagnostic and built-in self test (BIST) features. The following paragraphs describe the functionality of the chipset used for a HUD system in more detail.

The DLPC230S-Q1 is a controller for the DMD and the light sources in the DLP Headlight, HUD or Projector module. It receives input video from the host and synchronizes DMD and light source timing in order to achieve the desired video. The DLPC230S-Q1 formats input video data that is displayed on the DMD. It synchronizes these video segments with light source timing in order to create a video with grayscale shading and multiple colors, if applicable.

The DLPC230S-Q1 receives inputs from a host processor in the vehicle. The host provides commands and input video data. Host commands can be sent using either the I^{2}C bus or SPI bus. The bus that is not being used for host commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The 24-bit bus can be limited to only 8-bits or 16-bits of data for single light source or dual light source systems depending on the system design. The SPI flash memory provides the embedded software for the DLPC230S-Q1's ARM core, any calibration data, and default settings. The TPS99000S-Q1 provides diagnostic and monitoring information to the DLPC230S-Q1 using an SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The TMP411 uses an I^{2}C interface to provide the DMD array temperature to the DLPC230S-Q1.

The outputs of the DLPC230S-Q1 are configuration and monitoring commands to the TPS99000S-Q1, timing controls to the LED or laser driver, control and data signals to the DMD, and monitoring and diagnostics information to the host processor. The DLPC230S-Q1 communicates with the TPS99000S-Q1 over an SPI bus. It uses this to configure the TPS99000S-Q1 and to read monitoring and diagnostics information from the TPS99000S-Q1. The DLPC230S-Q1 sends drive enable signals to the LED or laser driver, and synchronizes this with the DMD mirror timing. The control signals to the DMD are sent using a subLVDS interface.

The TPS99000S-Q1 is a highly integrated mixed-signal IC that controls DMD power and provides monitoring and diagnostics information for the DLP HUD system. The power sequencing and monitoring blocks of the TPS99000S-Q1 properly power up the DMD and provide accurate DMD voltage rails (–16 V, 8.5 V, and 10 V), and then monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The TPS99000S-Q1 also has several output signals that can be used to control a variety of LED or laser driver topologies. The TPS99000S-Q1 has several general-purpose ADCs that designers can use for system level monitoring, such as over-brightness detection.

The TPS99000S-Q1 receives inputs from the DLPC230S-Q1, the power rails it monitors, the host processor, and potentially several other ADC ports. The DLPC230S-Q1 sends configuration and control commands to the TPS99000S-Q1 over an SPI bus and several other control signals. The DLPC230S-Q1's clocks are also monitored by the watchdogs in the TPS99000S-Q1 to detect any errors. The power rails are monitored by the TPS99000S-Q1 in order to detect power failures or glitches and request a proper power down of the DMD in case of an error. The host processor can read diagnostics information from the TPS99000S-Q1 using a dedicated SPI bus, which enables independent monitoring. Additionally, the host can request the image to be turned on or off using a PROJ_ON signal. Lastly, the TPS99000S-Q1 has several general-purpose ADCs that can be used to implement system level monitoring functions.

The outputs of the TPS99000S-Q1 are diagnostic information and error alerts to the DLPC230S-Q1, and control signals to the LED or laser driver. The TPS99000S-Q1 can output diagnostic information to the host and the DLPC230S-Q1 over two SPI buses. In case of critical system errors, such as power loss, it outputs signals to the DLPC230S-Q1 that trigger power down or reset sequences. It also has output signals that can be used to implement various LED or laser driver topologies.

ADVANCE INFORMATION

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data), and produces a mechanical output (mirror position). The electrical interface to the DMD is a subLVDS interface with the DLPC230S-Q1. The mechanical output is the state of more than 0.9 million mirrors in the DMD array that can be tilted ±12°. In a projection system the mirrors are used as pixels in order to display an image.

8.2.2 Reference Design

For information about connecting together the DLP4620S-Q1 DMD, DLPC230S-Q1 controller, and TPS99000S-Q1, please contact the TI Application Team for additional information about the DLP4620S-Q1 evaluation module (EVM). TI has optical-mechanical reference designs available, see the TI Application team for more information.

8.2.3 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles, or number of operating hours at different temperatures. To assist in evaluation an Application Report may be provided in the future. See the TI Application team for more information.

ADVANCE INFORMATION

Product Folder Links: *DLP4620S-Q1*

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required. DMD power-up and power-down sequencing is strictly controlled by the TPS99000S-Q1 device.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. VSS must also be connected.

## 9.1 Power Supply Power-Up Procedure

- During power-up, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in the *Recommended Operating Conditions*.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after VDD and VDDI have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in 图 9-1.

9.2 Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in the *Recommended Operating Conditions* (refer to Note 2 in 节 9.3).
- During power-down, the DMD's LPSDR input pins must be less than VDDI, the specified limit shown in the *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in 节 9.3.

ADVANCE INFORMATION

9.3 Power Supply Sequencing Requirements

图 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)
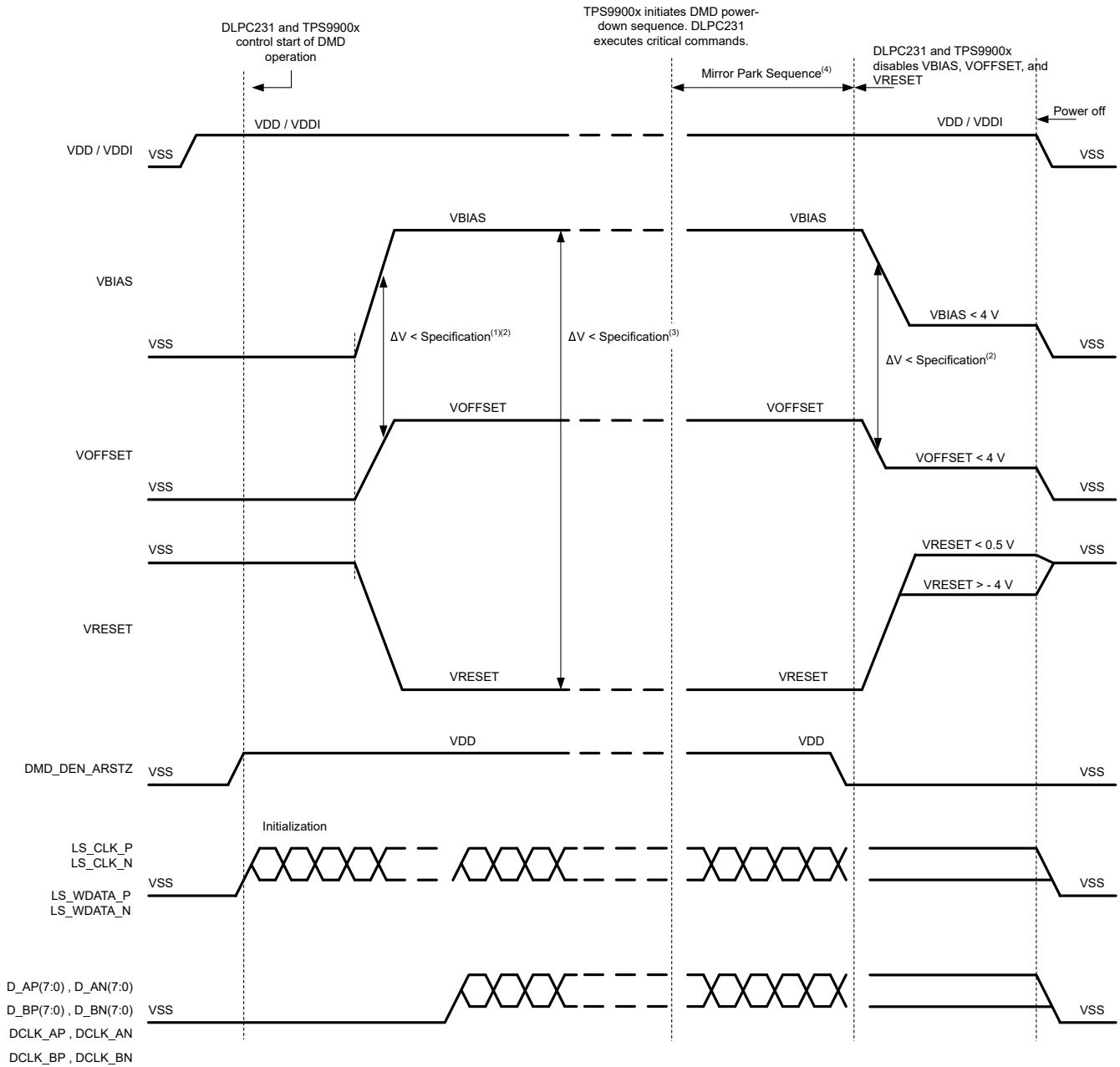
A. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in the Recommended Operating Conditions. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down. Also, the TPS99000S-Q1 is capable of managing the timing between VBIAS and VOFFSET.

B. To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified than the limit shown in the Recommended Operating Conditions.

C. When system power is interrupted, the TPS99000S-Q1 initiates hardware power-down that disables VBIAS, VRESET, and VOFFSET after the Micromirror Park Sequence.

D. The drawing is not to scale and details are omitted for clarity.

10 Layout

10.1 Layout Guidelines

Please refer to the DLPC230S-Q1 and TPS99000S-Q1 data sheets for specific PCB layout and routing guidelines. For specific DMD PCB guidelines, use the following:

- Match lengths for the LS_WDATA and LS_CLK signals
- Minimize vias, layer changes, and turns for the HS bus signals
- Minimum of two 220-nF decoupling capacitors close to VBIAS
- Minimum of two 220-nF decoupling capacitors close to VRESET
- Minimum of two 220-nF decoupling capacitors close to VOFFSET
- Minimum of four 100-nF decoupling capacitors close to VDDI and VDD
- Temperature diode pins

  The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411 temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411 are sensitive to noise. See the *TMP411 ±1°C Remote and Local Temperature Sensor with N-Factor and Series Resistance Correction Data Sheet* for specific routing recommendations.

ADVANCE INFORMATION

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11 Device and Documentation Support

11.1 第三方产品免责声明

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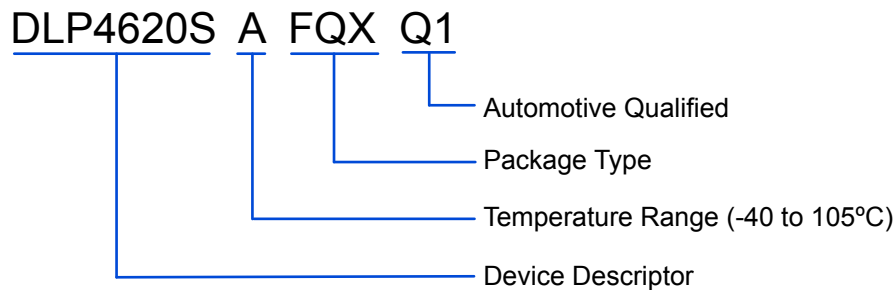### 11.2 Device Support

11.2.1 Device Nomenclature

图 11-1. Part Number Description

11.2.2 Device Markings

The device marking includes the legible character string GHJJJJK DLP4620SAFQXQ1. GHJJJJK is the lot trace code. DLP4620SAFQXQ1 is the part number.
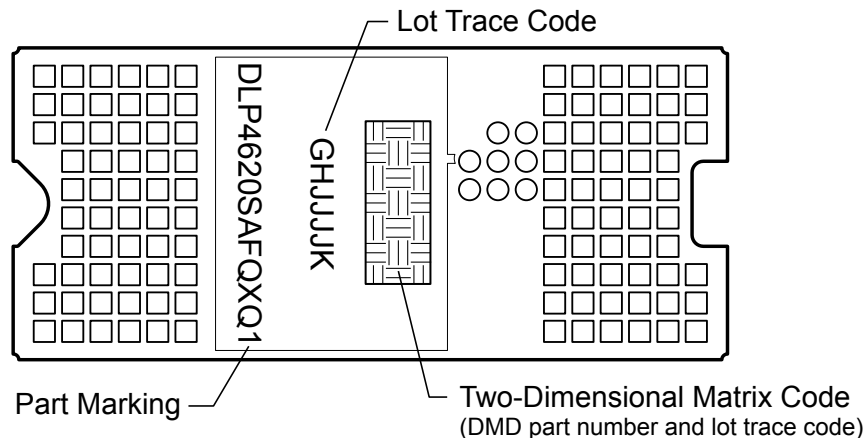

图 11-2. DMD Marking

11.3 Trademarks

DLP® is a registered trademark of Texas Instruments.

is a registered trademark of Texas Instruments.

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11.4 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

Product Folder Links: *DLP4620S-Q1*

11.5 DMD Handling

The DMD is an optical device so precautions should be taken to avoid damaging the glass window. Please see the application note DLPA019 DMD Handling for instructions on how to properly handle the DMD.

11.6 术语表

TI 术语表　　　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XDLP462SAFQXQ1	ACTIVE	CLGA	FQX	120	72	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 105		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TRAY

L - Outer tray length without tabs

KO - Outer tray height

W - Outer tray width

P1 - Tray unit pocket pitch

CW - Measurement for tray edge (Y direction) to corner pocket center

CL - Measurement for tray edge (X direction) to corner pocket center

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
XDLP462SAFQXQ1	FQX	CLGA	120	72	8 x 7	150	315	135.9	12190	21.9	15.15	16.95

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