DLP801XE 0.8 4K+ DMD

1 特性

- 0.8 英寸对角线微镜阵列
  - 4K+ (3840 × 2400) 显示分辨率
  - 9.0µm 微镜间距
  - ±14.5° 微镜倾斜度（相对于平坦表面）
  - 角落照明
- 支持高光功率密度，适用于高亮度大型场馆显示器
  - 高达 40W/cm^2 总光功率密度
- 2xLVDS 输入数据总线
- 支持高达 60 Hz 的 4K+ 分辨率
- DLPC4420 display controller、DLPA100 电源管理和电机驱动器 IC 为激光荧光体和 RGB 激光提供支持

2 应用

- 大型场馆投影仪
- 智能投影仪
- 企业投影仪
- 数字标牌

3 说明

DLP801XE 数字微镜器件 (DMD) 是一款数控微机电系统 (MEMS) 空间光调制器 (SLM)，可用于实现高亮度 4K+ 固态照明显示系统。TI DLP® 0.8-inch 4K+ 芯片组由 DMD、two DLPC4420 display controllers、DLPA300 微镜驱动器以及 DLPA100 电源和电机驱动器组成。芯片组外形紧凑，可为体型小巧并采用固态照明的 4K+ 显示提供完整的系统解决方案。

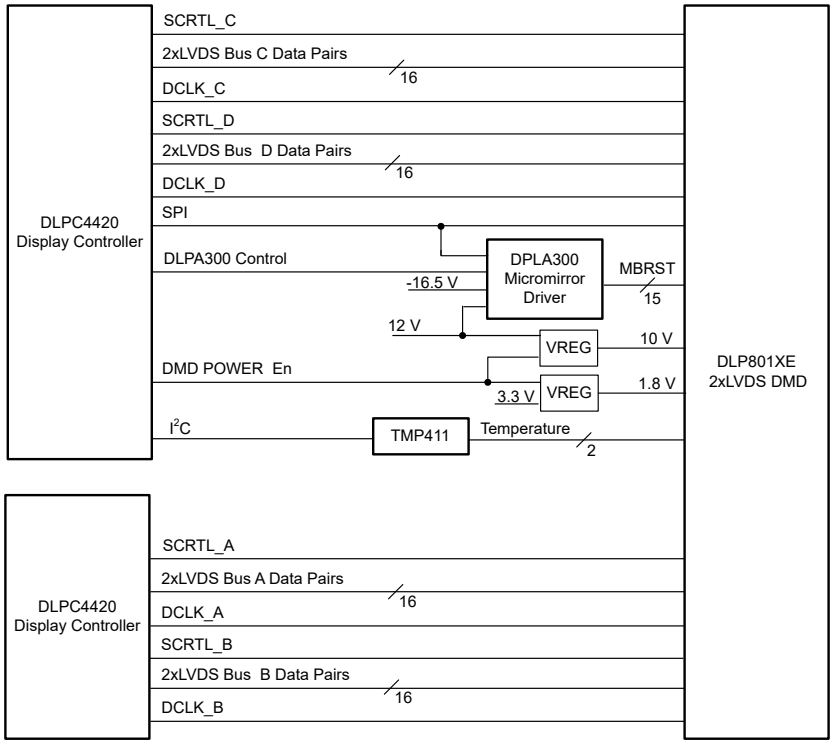
为了帮助缩短设计周期，DMD 生态系统包含现成的资源，其中包括量产就绪型光学模块、光学模块制造商和设计公司。

要了解有关如何使用 DMD 开始进行设计的更多信息，请访问 *TI DLP 显示技术入门* 页面。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
DLP801XE	FYV (350)	35.0 mm × 32.2 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用

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Changes from Revision * (October 2022) to Revision A (March 2023)	Page
• Added t_{SKEW_A2B}	14
• Updated 图 6-8	15

5 Pin Configuration and Functions

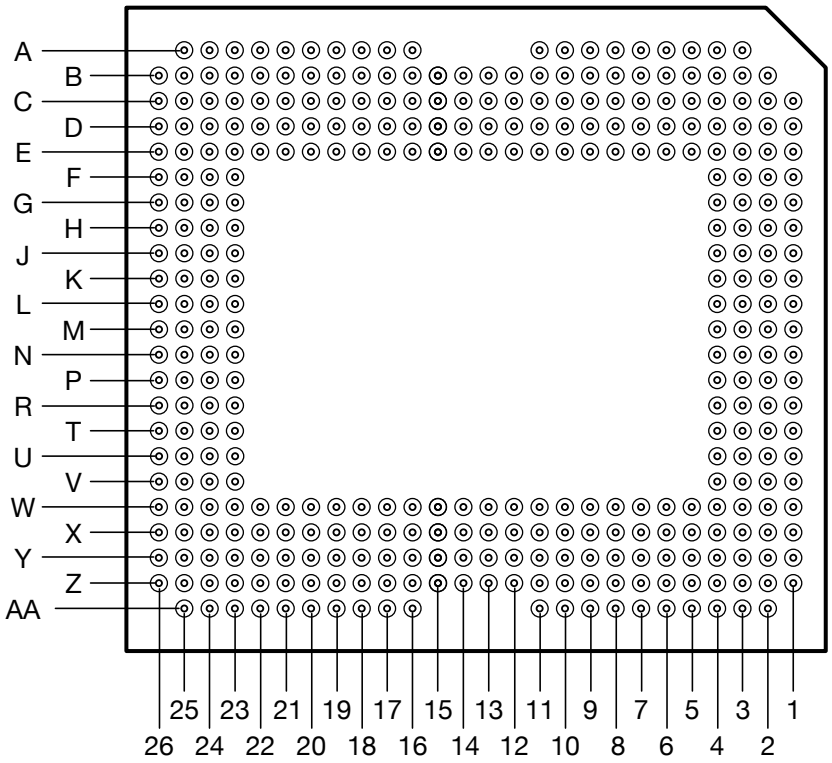


图 5-1. FYV Package (350-Pin) Bottom View

表 5-1. Pin Functions

PIN		TYPE[1]	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
LVDS BUS A					
D_AN(0)	E10	I	High-speed differential pair	LVDS	Differential 100 Ω
D_AP(0)	E11	I			
D_AN(1)	D6	I	High-speed differential pair		Differential 100 Ω
D_AP(1)	C6	I			
D_AN(2)	E3	I	High-speed differential pair		Differential 100 Ω
D_AP(2)	D3	I			
D_AN(3)	C7	I	High-speed differential pair		Differential 100 Ω
D_AP(3)	C8	I			
D_AN(4)	D8	I	High-speed differential pair		Differential 100 Ω
D_AP(4)	D7	I			
D_AN(5)	E6	I	High-speed differential pair		Differential 100 Ω
D_AP(5)	E5	I			
D_AN(6)	C5	I	High-speed differential pair		Differential 100 Ω
D_AP(6)	C4	I			
D_AN(7)	B8	I	High-speed differential pair		Differential 100 Ω
D_AP(7)	B9	I			
D_AN(8)	B6	I	High-speed differential pair		Differential 100 Ω
D_AP(8)	B5	I			
D_AN(9)	C10	I	High-speed differential pair		Differential 100 Ω
D_AP(9)	B10	I			
D_AN(10)	A9	I	High-speed differential pair		Differential 100 Ω
D_AP(10)	A10	I			
D_AN(11)	C13	I	High-speed differential pair		Differential 100 Ω
D_AP(11)	C14	I			
D_AN(12)	B12	I	High-speed differential pair		Differential 100 Ω
D_AP(12)	B13	I			
D_AN(13)	C17	I	High-speed differential pair		Differential 100 Ω
D_AP(13)	C16	I			
D_AN(14)	B15	I	High-speed differential pair		Differential 100 Ω
D_AP(14)	B16	I			
D_AN(15)	D15	I	High-speed differential pair		Differential 100 Ω
D_AP(15)	E15	I			
DCLK_AN	B3	I	High-speed differential pair		Differential 100 Ω
DCLK_AP	C3	I			
SCTRL_AN	E4	I	High-speed differential pair		Differential 100 Ω
SCTRL_AP	D4	I			
LVDS BUS B					

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
D_BN(0)	W10	I	High-speed differential pair	LVDS	Differential 100 Ω
D_BP(0)	W11	I			
D_BN(1)	Z3	I	High-speed differential pair		Differential 100 Ω
D_BP(1)	Y3	I			
D_BN(2)	W4	I	High-speed differential pair		Differential 100 Ω
D_BP(2)	X4	I			
D_BN(3)	Y7	I	High-speed differential pair		Differential 100 Ω
D_BP(3)	Y8	I			
D_BN(4)	X8	I	High-speed differential pair		Differential 100 Ω
D_BP(4)	X7	I			
D_BN(5)	Y6	I	High-speed differential pair		Differential 100 Ω
D_BP(5)	X6	I			
D_BN(6)	X3	I	High-speed differential pair		Differential 100 Ω
D_BP(6)	W3	I			
D_BN(7)	Z8	I	High-speed differential pair		Differential 100 Ω
D_BP(7)	Z9	I			
D_BN(8)	Z6	I	High-speed differential pair		Differential 100 Ω
D_BP(8)	Z5	I			
D_BN(9)	Y10	I	High-speed differential pair		Differential 100 Ω
D_BP(9)	Z10	I			
D_BN(10)	AA9	I	High-speed differential pair		Differential 100 Ω
D_BP(10)	AA10	I			
D_BN(11)	Y13	I	High-speed differential pair		Differential 100 Ω
D_BP(11)	Y14	I			
D_BN(12)	Z12	I	High-speed differential pair		Differential 100 Ω
D_BP(12)	Z13	I			
D_BN(13)	Y17	I	High-speed differential pair		Differential 100 Ω
D_BP(13)	Y16	I			
D_BN(14)	Z15	I	High-speed differential pair		Differential 100 Ω
D_BP(14)	Z16	I			
D_BN(15)	X15	I	High-speed differential pair		Differential 100 Ω
D_BP(15)	W15	I			
DCLK_BN	Y4	I	High-speed differential pair		Differential 100 Ω
DCLK_BP	Y5	I			
SCTRL_BN	W5	I	High-speed differential pair		Differential 100 Ω
SCTRL_BP	W6	I			
LVDS BUS C					

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
D_CN(0)	B18	I	High-speed differential pair	LVDS	Differential 100 Ω
D_CP(0)	B19	I			
D_CN(1)	H24	I	High-speed differential pair		Differential 100 Ω
D_CP(1)	G24	I			
D_CN(2)	L23	I	High-speed differential pair		Differential 100 Ω
D_CP(2)	K23	I			
D_CN(3)	C18	I	High-speed differential pair		Differential 100 Ω
D_CP(3)	C19	I			
D_CN(4)	A19	I	High-speed differential pair		Differential 100 Ω
D_CP(4)	A20	I			
D_CN(5)	E24	I	High-speed differential pair		Differential 100 Ω
D_CP(5)	D24	I			
D_CN(6)	K25	I	High-speed differential pair		Differential 100 Ω
D_CP(6)	J25	I			
D_CN(7)	C26	I	High-speed differential pair		Differential 100 Ω
D_CP(7)	D26	I			
D_CN(8)	C21	I	High-speed differential pair		Differential 100 Ω
D_CP(8)	B21	I			
D_CN(9)	G25	I	High-speed differential pair		Differential 100 Ω
D_CP(9)	F25	I			
D_CN(10)	A24	I	High-speed differential pair		Differential 100 Ω
D_CP(10)	B24	I			
D_CN(11)	J26	I	High-speed differential pair		Differential 100 Ω
D_CP(11)	K26	I			
D_CN(12)	D25	I	High-speed differential pair		Differential 100 Ω
D_CP(12)	C25	I			
D_CN(13)	E23	I	High-speed differential pair		Differential 100 Ω
D_CP(13)	D23	I			
D_CN(14)	B23	I	High-speed differential pair		Differential 100 Ω
D_CP(14)	C23	I			
D_CN(15)	K24	I	High-speed differential pair		Differential 100 Ω
D_CP(15)	L24	I			
DCLK_CN	H23	I	High-speed differential pair		Differential 100 Ω
DCLK_CP	G23	I			
SCTRL_CN	F26	I	High-speed differential pair		Differential 100 Ω
SCTRL_CP	G26	I			
LVDS BUS D					

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
D_DN(0)	Z18	I	High-speed differential pair	LVDS	Differential 100 Ω
D_DP(0)	Z19	I			
D_DN(1)	T24	I	High-speed differential pair		Differential 100 Ω
D_DP(1)	U24	I			
D_DN(2)	N23	I	High-speed differential pair		Differential 100 Ω
D_DP(2)	P23	I			
D_DN(3)	Y18	I	High-speed differential pair		Differential 100 Ω
D_DP(3)	Y19	I			
D_DN(4)	AA19	I	High-speed differential pair		Differential 100 Ω
D_DP(4)	AA20	I			
D_DN(5)	W24	I	High-speed differential pair		Differential 100 Ω
D_DP(5)	X24	I			
D_DN(6)	P25	I	High-speed differential pair		Differential 100 Ω
D_DP(6)	R25	I			
D_DN(7)	Y26	I	High-speed differential pair		Differential 100 Ω
D_DP(7)	X26	I			
D_DN(8)	Y21	I	High-speed differential pair		Differential 100 Ω
D_DP(8)	Z21	I			
D_DN(9)	U25	I	High-speed differential pair		Differential 100 Ω
D_DP(9)	V25	I			
D_DN(10)	AA24	I	High-speed differential pair		Differential 100 Ω
D_DP(10)	Z24	I			
D_DN(11)	R26	I	High-speed differential pair		Differential 100 Ω
D_DP(11)	P26	I			
D_DN(12)	X25	I	High-speed differential pair		Differential 100 Ω
D_DP(12)	Y25	I			
D_DN(13)	W23	I	High-speed differential pair		Differential 100 Ω
D_DP(13)	X23	I			
D_DN(14)	Z23	I	High-speed differential pair		Differential 100 Ω
D_DP(14)	Y23	I			
D_DN(15)	P24	I	High-speed differential pair		Differential 100 Ω
D_DP(15)	N24	I			
DCLK_DN	T23	I	High-speed differential pair		Differential 100 Ω
DCLK_DP	U23	I			
SCTRL_DN	V26	I	High-speed differential pair		Differential 100 Ω
SCTRL_DP	U26	I			
SCP INTERFACE					
SCPCLK	U2	I	Serial Communications Port CLK	LVCMOS	Internal Pull Down
SCPDI	T3	I	Serial Communications Data In	LVCMOS	Internal Pull Down
SCPENZ	U4	I	Serial Communications Port Enable	LVCMOS	Internal Pull Down
SCPDO	U3	O	Serial Communications Port Output	LVCMOS	Internal Pull Down
OTHER SIGNALS					
DMD_PWRDNZ	G4	I	Chip – Level ResetZ	LVCMOS	Internal Pull Down

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
N/C	G1, H1, J1, J3, J4, K3, P3, R1, R3, R4, T1, U1, V3, D17, X17, K4, P4, F3, G2, W18, G3, H3, X16	No Connect			
TEMP_N	W16	I/O			
TEMP_P	W17	I/O			
MICROMIRROR BIAS RESET INPUTS					
MBRST(0)	E14	I	Mirror actuation signal		
MBRST(1)	D13	I	Mirror actuation signal		
MBRST(2)	E13	I	Mirror actuation signal		
MBRST(3)	C12	I	Mirror actuation signal		
MBRST(4)	E12	I	Mirror actuation signal		
MBRST(5)	C11	I	Mirror actuation signal		
MBRST(6)	D16	I	Mirror actuation signal		
MBRST(7)	C15	I	Mirror actuation signal		
MBRST(8)	W14	I	Mirror actuation signal		
MBRST(9)	X13	I	Mirror actuation signal		
MBRST(10)	W13	I	Mirror actuation signal		
MBRST(11)	Y12	I	Mirror actuation signal		
MBRST(12)	W12	I	Mirror actuation signal		
MBRST(13)	Y11	I	Mirror actuation signal		
MBRST(14)	Y15	I	Mirror actuation signal		
POWERS AND GROUNDS					
VDD	A5, A6, B2, C1, D10, D12, D19, D22, E8, E19, E20, E21, E22, F1, F2, J2, K1, L1, L25, M3, M4, M25, N1, N25, P1, R2, V1, V2, W8, W19, W20, W21, W22, X10, X12, X19, X22, Y1, Z1, Z2, AA2, AA5, AA6	P	Low-voltage CMOS core supply		

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
VDDI	A7, A8, A11, A16, A17, A18, A21, A22, A23, AA7, AA8, AA11, AA16, AA17, AA18, AA21, AA22, AA23	P	I/O supply		
VCC2	A3, A4, A25, B26, L26, M26, N26, Z26, AA3, AA4, AA25	P	Memory array stepped-up voltage		
VSS	B4, B7, B11, B14, B17, B20, B22, B25, C2, C9, C20, C22, C24, D1, D2, D5, D9, D11, D14, D18, D20, D21, E1, E2, E7, E9, E16, E17, E18, E25, E26, F4, F23, F24, H2, H4, H25, H26, J23, J24, K2, L2, L3, L4, M1, M2, M23, M24, N2, N3, N4, P2, R23, R24, T2, T4, T25, T26, V4, V23, V24, W1, W2, W7, W9, W25, W26, X1, X2, X5, X9, X11, X14, X18, X20, X21, Y2, Y9, Y20, Y22, Y24, Z4, Z7, Z11, Z14, Z17, Z20, Z22, Z25	G	Global ground		

(1) I = Input, O = Output, P = Power, G = Ground, NC = No Connect

6 Specifications

6.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{DD}	Supply voltage for LVCMOS core logic(1)	– 0.5	2.3	V
V_{DDI}	Supply voltage for LVDS Interface(1)	– 0.5	2.3	V
V_{CC2}	Micromirror Electrode and HVCMOS voltage(1) (2)	– 0.5	11	V
V_{MBRST}	Input voltage for MBRST pins(1)	– 17.5	22.5	V
$\lvert V_{DDI} - V_{DD} \rvert$	Supply voltage delta (absolute value)(3)		0.3	V
INPUT VOLTAGES				
$\lvert V_{ID} \rvert$	Input differential voltage for LVDS pins (absolute value)		500	mV
V_LVCMOS	Input voltage for all other input pins(1)	– 0.3	V_{DDI} + 0.3	V
ENVIRONMENTAL				
T_{ARRAY}	Temperature, operating(4)	0	90	°C
	Temperature, non – operating(4)	– 40	90	°C
T_{DP}	Dew point temperature, operating and non – operating (noncondensing)		81	°C

(1) All voltages are referenced to common ground V_{SS}. V_{DD}, V_{DDI}, and V_{CC2} power supplies are all required for all DMD operating modes.
(2) V_{CC2} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable voltage difference between V_{DD} and V_{DDI} may result in excessive current draw.
(4) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), shown in Figure 7-1 using the 节 7.6.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	– 40	80	°C
T_{DP-AVG}	Average dew point temperature (noncondensing)((1))		28	°C
T_{DP-ELR}	Elevated dew point temperature range (noncondensing)((2))	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	months

(1) This is the average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation must be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

SYMBOL	PARAMETER	DESCRIPTION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001((1))	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002((2))	±500	V
$V_{(ESD)}$	Electrostatic discharge (MBRST PINS)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±150	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{DD}	Supply voltage for LVCMOS core logic(1)	1.65	1.8	1.95	V
V_{DDI}	Supply voltage for LVDS Interface(1)	1.65	1.8	1.95	V
V_{CC2}	Micromirror Electrode and HVCMOS voltage(1) (2)	9.5	10	10.5	V
V_{MBRST}	Micromirror Bias / Reset Voltage(1)	–17		21.5	V
$\lvert V_{DD} - V_{DDI} \rvert$	Supply voltage delta (absolute value)(3)		0	0.3	V
LVCMOS					
$V_{IH(DC)}$	Input High Voltage	0.7 × VDD		V_{DD} + 0.3	V
$V_{IL(DC)}$	Input Low Voltage	–0.3		0.3 × VDD	V
$V_{IH(AC)}$	Input High Voltage	0.8 × VDD		V_{DD} + 0.3	V
$V_{IL(AC)}$	Input Low Voltage	–0.3		0.2 × VDD	V
I_{OH}	High-level Output Current			2	mA
I_{OL}	Low-level Output Current	–2			mA
t_{PWRDNZ}	PWRDNZ pulse width(4)	10			ns
SCP INTERFACE					
F_{SCPCLK}	SCP clock frequency	50		500	kHz
$SCPCLK_{DCDIN}$	SCP Clk Input duty cycle	40%		60%	
LVDS INTERFACE					
F_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(5)			400	MHz
DCD_{IN}	Input CLK Duty Cycle Distortion tolerance	44%		56%	
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(6)	150	300	440	mV
V_{CM}	Common mode voltage(6)	1100	1200	1300	mV
V_{LVDS}	LVDS voltage(6)	880		1520	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ	2			µs
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operational((8)) ((10)) ((11))	10		40 to 70(10)	°C
	Array temperature, short-term operational, 500 hr max((10)) ((13))	0		10	°C
$T_{DP\ -AVG}$	Average dew point average temperature (non – condensing)(12)			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(13)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
Q_{AP-ILL}	Window aperture illumination overfill(14) (15)			17	W/cm^2
SOLID STATE ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 410 nm((8))			10	mW/cm^2
ILL_{BLU1}	Illumination power at wavelengths ⩾ 410 nm and ⩽ 440 nm((22))			2	W/cm^2
ILL_{BLU}	Illumination power at wavelengths ⩾ 410 nm and ⩽ 475 nm((22))			12.8	W/cm^2
ILL_{VIS}	Illumination power at wavelengths ⩾ 410 nm and ⩽ 800 nm((22))			40	W/cm^2
ILL_{IR}	Ilumination power at wavelengths > 800 nm			10	mW/cm^2

(1) All voltages are referenced to common ground V_{SS}. V_{DD}, V_{DDI}, and V_{CC2} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(2) V_{CC2} supply transients must fall within specified max voltages.

(3) To prevent excess current, the supply voltage delta $|V_{DDI} - V_{DD}|$ must be less than the specified limit. See the *DMD Power Supply Requirements*.
(4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. The PWRDNZ input pin overrides the SCPENZ input pin and tristates the SCPDO output pin.
(5) See LVDS clock timing requirements in *Timing Requirements*.
(6) See Figure 6-5 for the LVDS waveform requirements.
(7) Simultaneous exposure of the DMD to the maximum *Recommend Operating Conditions* for temperature and UV illumination reduces device lifetime.
(8) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), shown in Figure 7-1 using the *Micromirror Array Temperature Calculation*.
(9) Long-term is defined as the usable life of the device.
(10) Per Figure 6-1, the maximum operational array temperature is derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See *Micromirror Landed-on/Landed-off Duty Cycle* for a definition of micromirror landed duty cycle.
(11) Short-term is the total cumulative time over the useful life of the device.
(12) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(13) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT_{ELR}.
(14) Applies to region defined in Figure 6-2
(15) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Minimizing the light flux incident outside the active array is a design requirement of the illumination optical system. Depending on the particular optical architecture and assembly tolerances of the optical system, the amount of overfill light on the outside of the active array may cause system performance degradation.
(16) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).

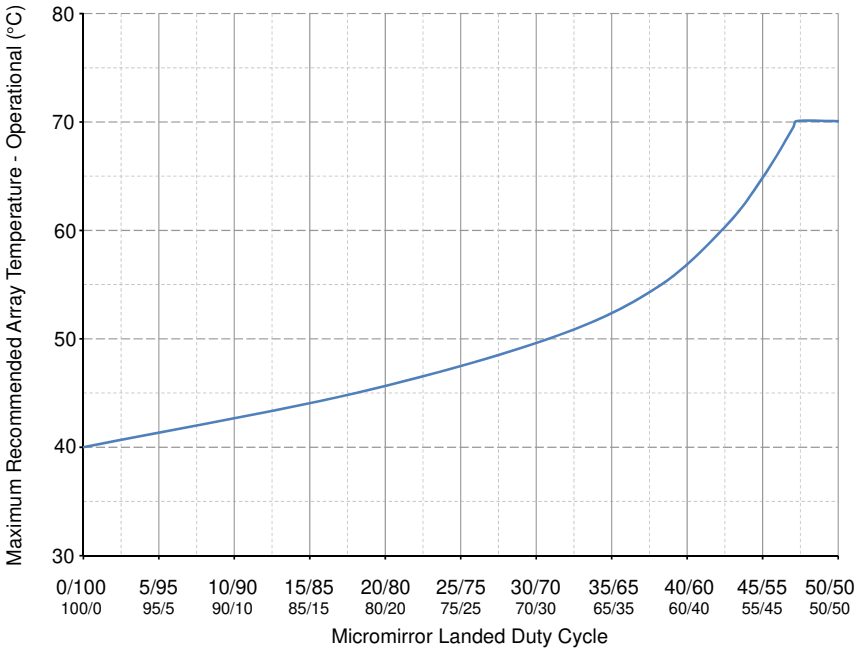


图 6-1. Maximum Recommended Array Temperature—Derating Curve

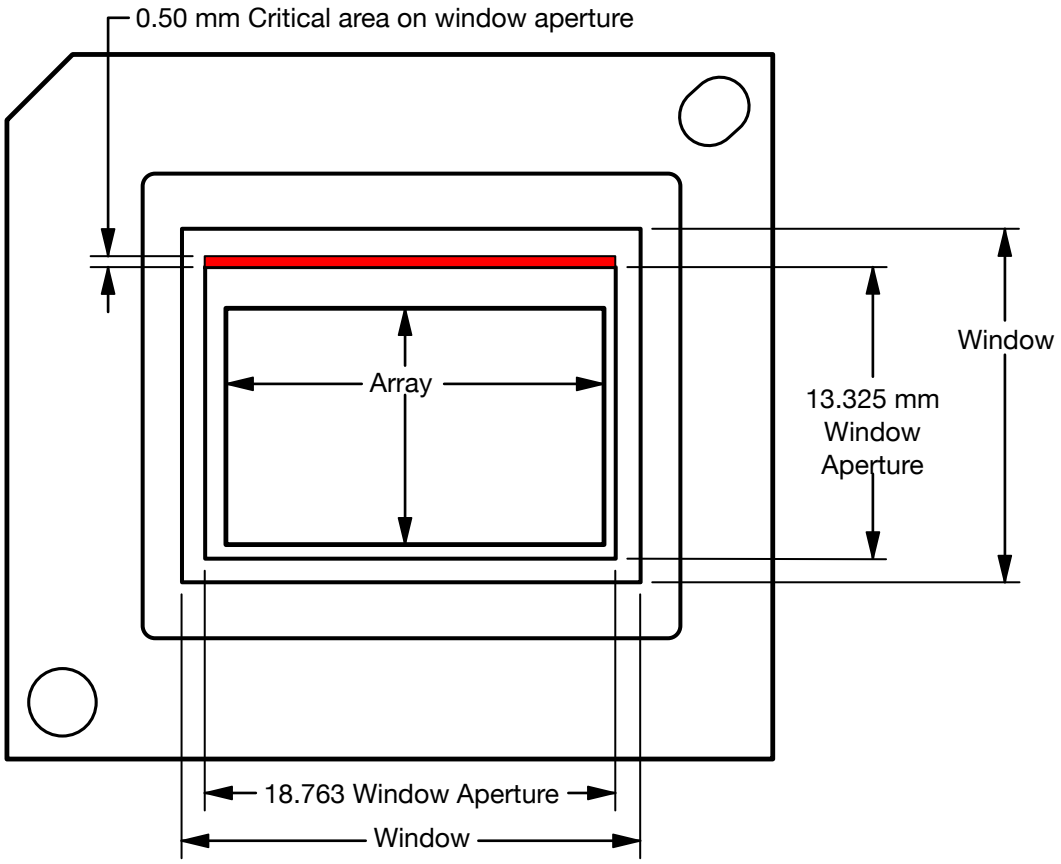


图 6-2. Illumination Overfill Diagram - Critical Area

6.5 Thermal Information

THERMAL METRIC	DLP801XE FYV 350 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)(1)	0.50	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the *Recommended Operating Conditions*.
The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.
Minimizing the light energy falling outside the window clear aperture is a design requirement of the optical system because any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Information						
I_{DD}	Supply current V_{DD} ((1))				1200	mA
I_{DDI}	Supply current V_{DDI} ((1))				340	mA
I_{CC2}	Supply current V_{CC2}				40	mA
P_{DD}	Supply power V_{DD} ((1))				2340	mW
P_{DDI}	Supply power V_{DDI} ((1))				663	mW
P_{CC2}	Supply power V_{CC2}				420	mW

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS						
V_{OH}	High-level output voltage	I_{OH} = 2 mA	0.8			× V_{DD}
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	× V_{DD}
I_{OZ}	High impedance output current	V_{DD} = 1.95 V			10	µA
I_{IL}	Low-level input current	VDD= 1.95 V, Vin = 0 V	– 60			µA
I_{IH}	High-level input current((2))	VDD = 1.95 V, Vin = VDD			200	µA
Capacitances						
C_I	Input capacitance: LVDS pins	f = 1 MHz			20	pF
C_I	Input capacitance(2)	f = 1 MHz			15	pF
C_O	Output capacitance(2)	f = 1 MHz			15	pF
C_{IM}	Input capacitance for MBRST[0:14] pins	f = 75 kHz	400	450	570	pF

(1) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than the specified limit in *Absolute Maximum Ratings*.
(2) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins

6.7 Timing Requirements

Over *Recommended Operating Conditions* (unless otherwise noted)

PARAMETER DESCRIPTION		MIN	NOM	MAX	UNIT
SCP					
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling-edge)(1)	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling-edge)(1)	900			ns
$t_{SCP\_NEG\_ENZ}$	Time between falling edge of SCPENZ and the rising edge of SCPCLK((1))	1			µs
$t_{SCP\_POS\_ENZ}$	Time between falling edge of SCPCLK and the rising edge of SCPENZ((1))	1			µs
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state).(1)			960	ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high-level)	1			$1/F_{scpclk}$
t_r	Rise time (20% to 80%). See ((2))			200	ns
t_f	Fall time (80% to 20%). See (2)			200	ns
LVDS					
t_{R_LVDS}	Rise time (20% to 80%). See ((3))			500	ps
t_{F_LVDS}	Fall time (80% to 20%). See (3)			500	ps
t_C	Clock Cycle Duration for DCLK_C and DCLK_D(4)	2.5			ns
t_W	Pulse Duration for DCLK_C/D((4))	1.19			ns
t_{SU_data}	Setup Time for High-speed data(15:0) before DCLK(4)	350			ps
t_{SU_sctrl}	Setup Time for SCTRL before DCLK(4)	330			ps
t_{H_data}	Hold time for High-speed data(15:0) after DCLK(4)	150			ps
t_{H_sctrl}	Hold Time for SCTRL after DCLK(4)	170			ps
t_{SKEW_A2B}	Skew tolerance between Channel B and Channel A((6)) ((7)) ((8))	-1.25		1.25	ns
t_{SKEW_C2D}	Skew tolerance between Channel C and Channel D(5) ((9)) ((10))	– 1.25		1.25	ns

(1) See Figure 6-3.
(2) See Figure 6-4.
(3) See Figure 6-6.
(4) See Figure 6-7.
(5) See Figure 6-8.
(6) Channel A (Bus A) includes the following LVDS pairs: DCLK_A, SCTRL_A, and D_A.

(7) Channel B (Bus B) includes the following LVDS pairs: DCLK_B, SCTRL_B, and D_B.
(8) Channel C (Bus C) includes the following LVDS pairs: DCLK_C, SCTRL_C, and D_C
(9) Channel D (Bus D) includes the following LVDS pairs: DCLK_D, SCTRL_D, and D_D.

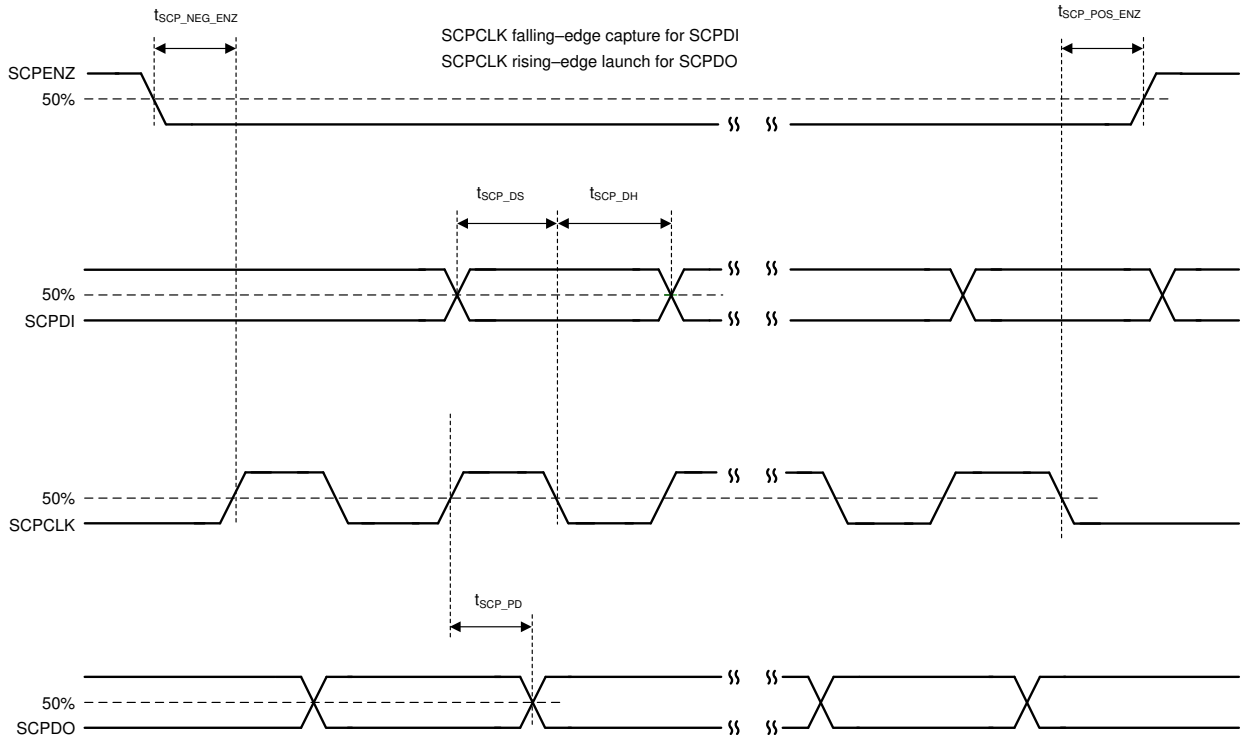


图 6-3. SCP Timing Parameters

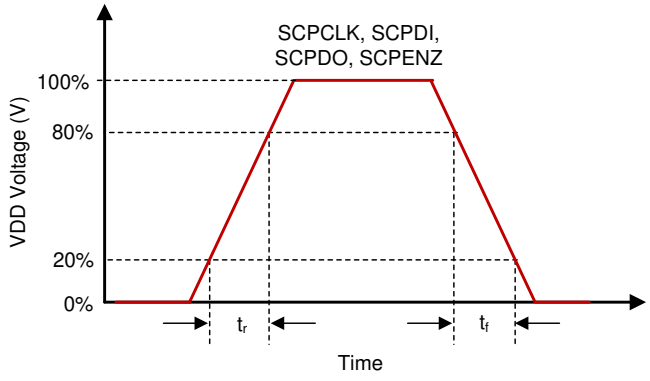


图 6-4. SCP Rise and Fall Times

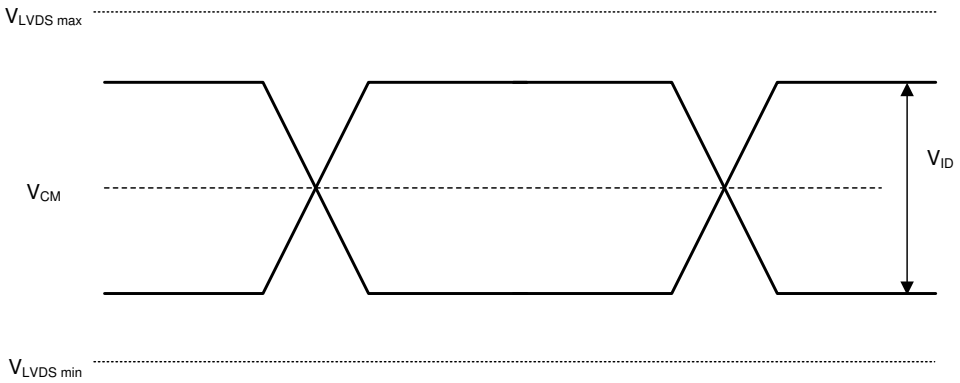


图 6-5. LVDS Waveform Parameters

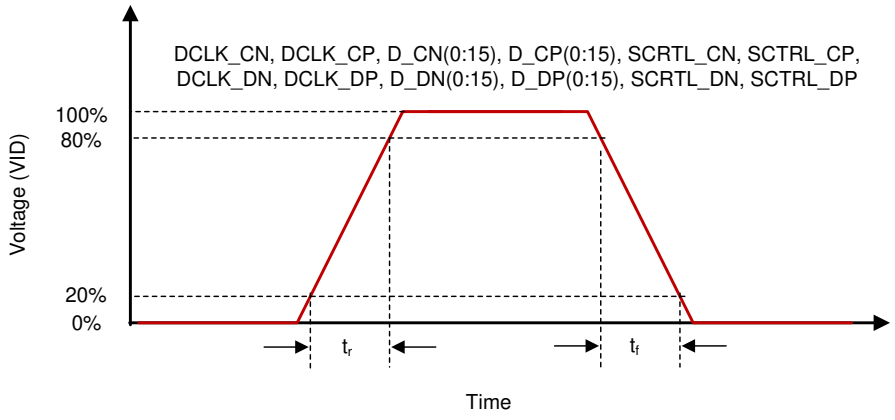


图 6-6. LVDS Rise and Fall Times

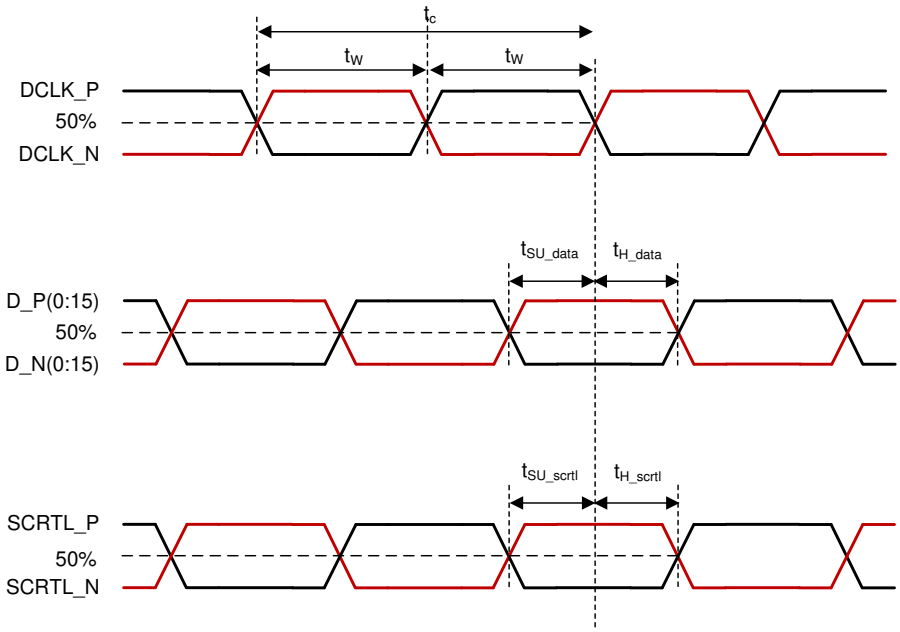


图 6-7. LVDS Timing Parameters

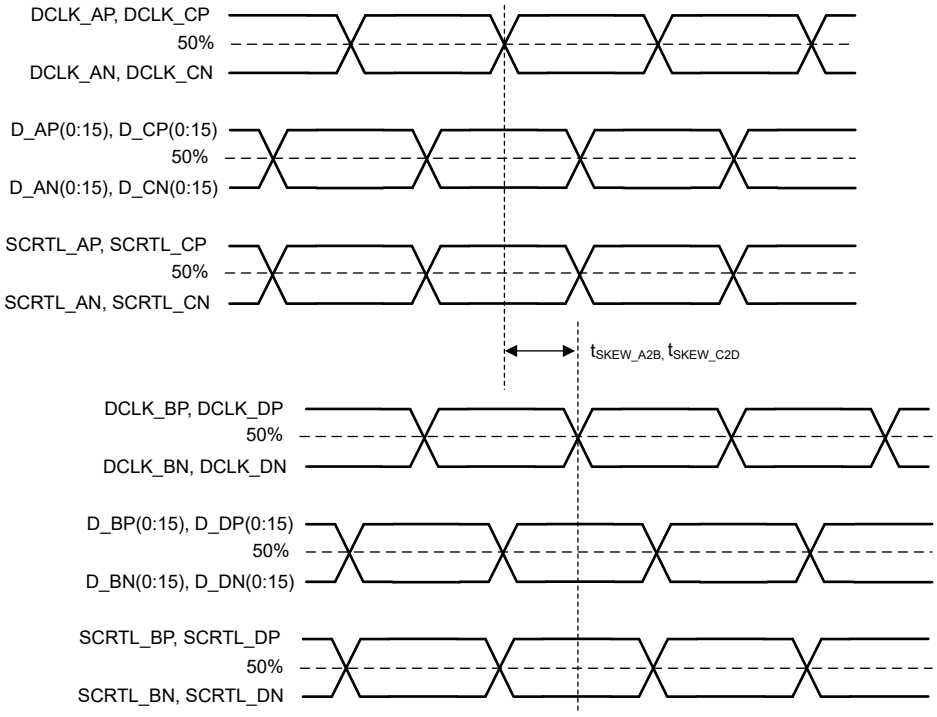


图 6-8. LVDS Skew Parameters

6.8 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
When loads are applied on both electrical and thermal interface areas				

PARAMETER	MIN	NOM	MAX	UNIT
Maximum load to be applied to the electrical interface area(1)			111	N
Maximum load to be applied to the thermal interface area(1)			111	N
When load is applied on the electrical interface area only				
Maximum load to be applied to the electrical interface area(1)			222	N
Maximum load to be applied to the thermal interface area(1)			0	N

(1) The load must be uniformly applied in the corresponding areas shown in Figure 6-9.

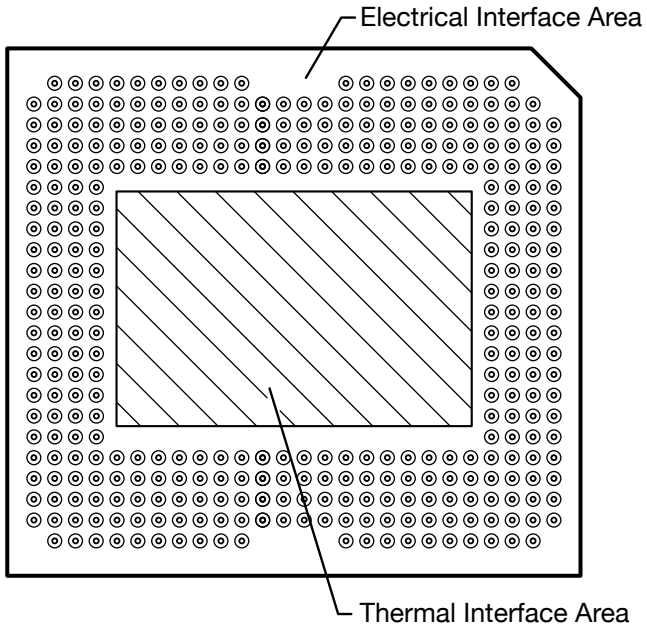


图 6-9. System Mounting Interface Loads

6.9 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
M	Number of active columns (1)	1920	micromirrors
N	Number of active rows (1)	1200	micromirrors
P	Micromirror (pixel) pitch(1)	9.0	µm
Micromirror active array width(1)	Micromirror pitch x number of active columns	17.280	mm
Micromirror active array height(1)	Micromirror pitch x number of active rows	10.800	mm
Micromirror active border (top and bottom)(2)	Pond of micromirror (POM)	12	micromirrors/side
Micromirror active border (right and left)(2)	Pond of micromirror (POM)	12	micromirrors/side

(1) See Figure 6-10.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

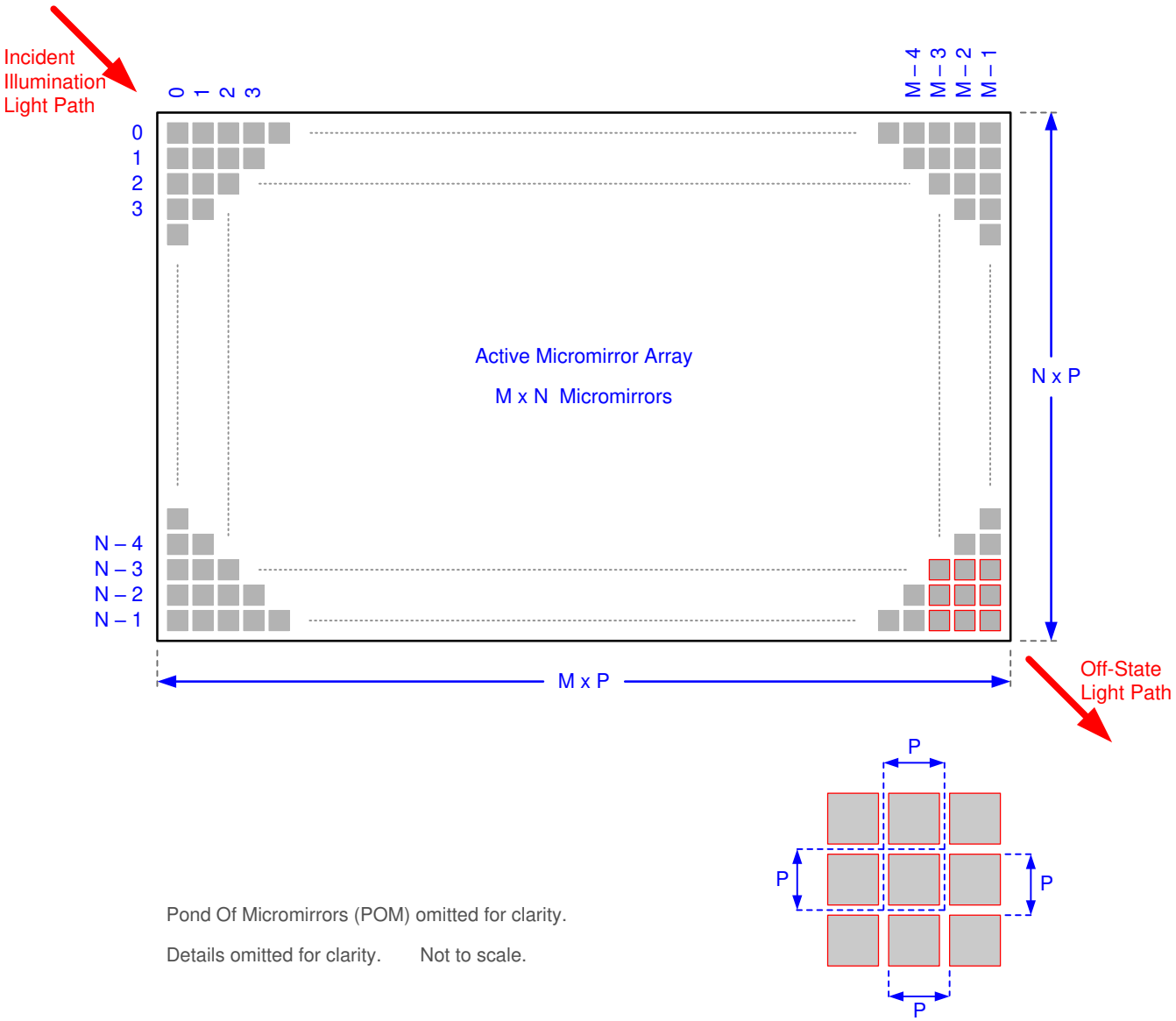


图 6-10. Micromirror Array Physical Characteristics

6.10 Micromirror Array Optical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle(2) (3) (4) (5)		Landed state((1))	13.5	14.5	15.5	degrees
Micromirror crossover time(6)		typical performance		3		µs
Micromirror switching time(7)		typical performance	8			µs
Image performance (8)	Bright pixel(s) in active area(9)	Gray 10 screen(12)			0	micromirrors
	Bright pixel(s) in the POM(9) (11)	Gray 10 screen(12)			1	
	Dark pixel(s) in the active area(10)	White screen(13)			4	
	Adjacent pixel(s)((16))	Any screen			0	
	Unstable pixel(s) in active area(15)	Any screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(5) Refer to Figure 6-11.
(6) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(7) The minimum time between successive transitions of a micromirror.
(8) Conditions of Acceptance: all DMD image performance returns are evaluated using the following projected image test conditions:
Test set degamma shall be linear.
Test set brightness and contrast shall be set to nominal.
The diagonal size of the projected image shall be a minimum of 60 inches.
The projections screen shall be 1× gain.
The projected image shall be inspected from an 8-foot minimum viewing distance.
The image shall be in focus during all image performance tests.
(9) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(10) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(11) POM definition: rectangular border of off-state mirrors surrounding the active area
(12) Gray 10 screen definition: a full screen with RGB values set to R = 10/255, G = 10/255, B = 10/255
(13) White screen definition: a full screen with RGB values set to R=255/255, G = 255/255, B = 255/255
(14) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
(15) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

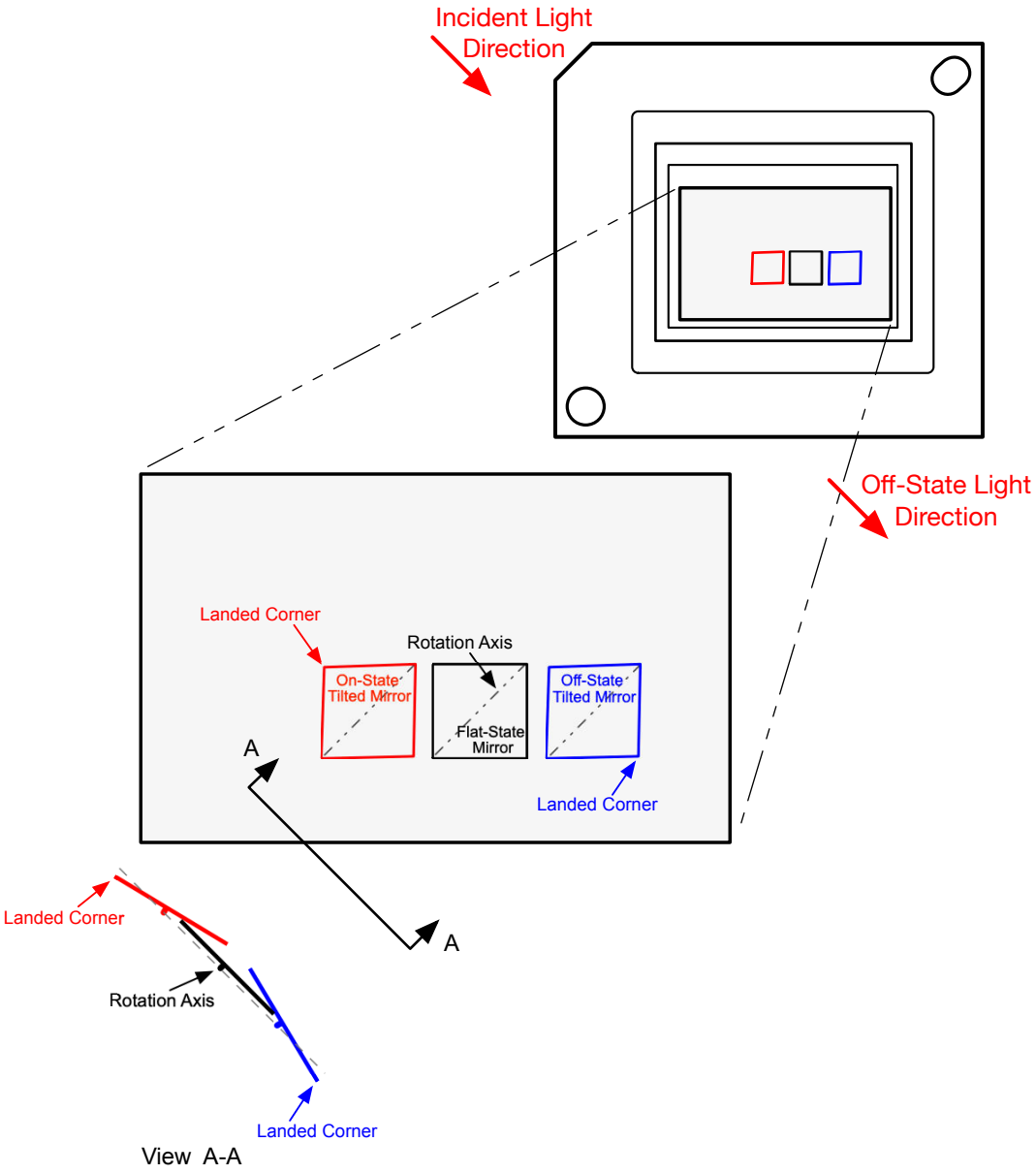


图 6-11. Micromirror Landed Orientation and Tilt

6.11 Window Characteristics

PARAMETER DESCRIPTION	Test Conditions	MIN	NOM	MAX	UNIT
Window Material			Corning EagleXG		
Window Refractive Index	546.1 nm		1.5119		

6.12 Chipset Component Usage Specification

Reliable function and operation of the DLP801XE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD

control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

备注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

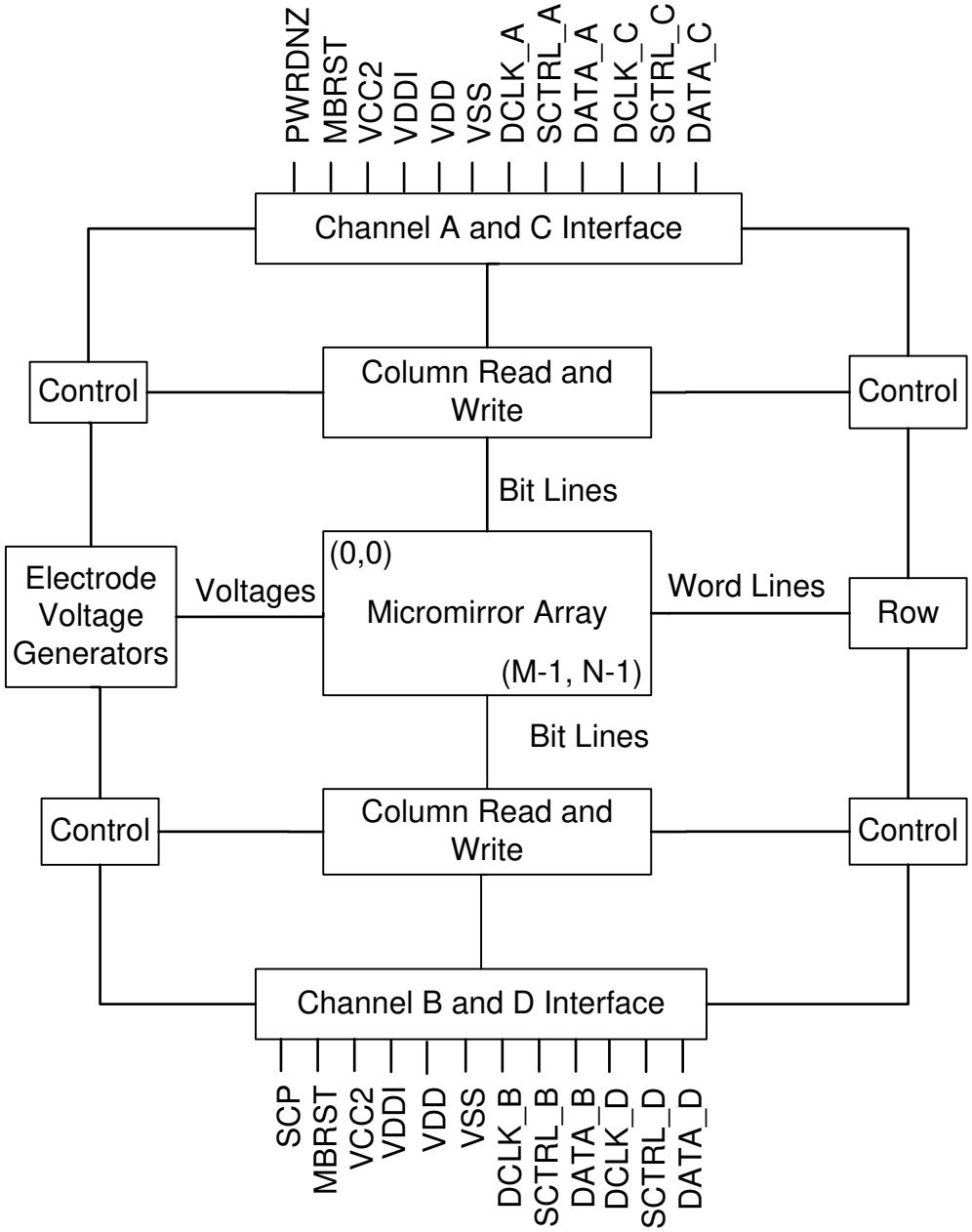
7 Detailed Description

7.1 Overview

The DMD is a 0.8-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables the micromirror array to display a full 3840 × 2400 pixel image at a 60 Hz frame rate. The electrical interface is a low voltage differential signaling (LVDS) interface. The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the 节 7.2. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.8-inch 4K+ chipset is comprised of the DLP801XE DMD, two DLPC4420 display controllers, the DLPA300 micromirror driver and the DLPA100 power management and motor driver. To ensure reliable operation, the DLP801XE DMD must always be used with the DLP display controller and the power and motor driver specified in the chipset.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Interface

The DMD requires two DC voltages: 1.8-V source for VDD and VDDI, and a 10-V supply for VCC2. In a typical configuration, 3.3 V is created by the DLPA100 power management and motor driver and is used on the DMD board to create the 1.8 V. The DLPA300 micromirror driver takes in the 12 V and creates the micromirror reset voltages.

7.3.2 Timing

The data sheet specifies timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4420 display controller. See the DLPC4420 display controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The DLP801XE has a 14.5° tilt angle which corresponds to the f/2.0 numerical aperture. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than 2° larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border or active area are possible.

7.5.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

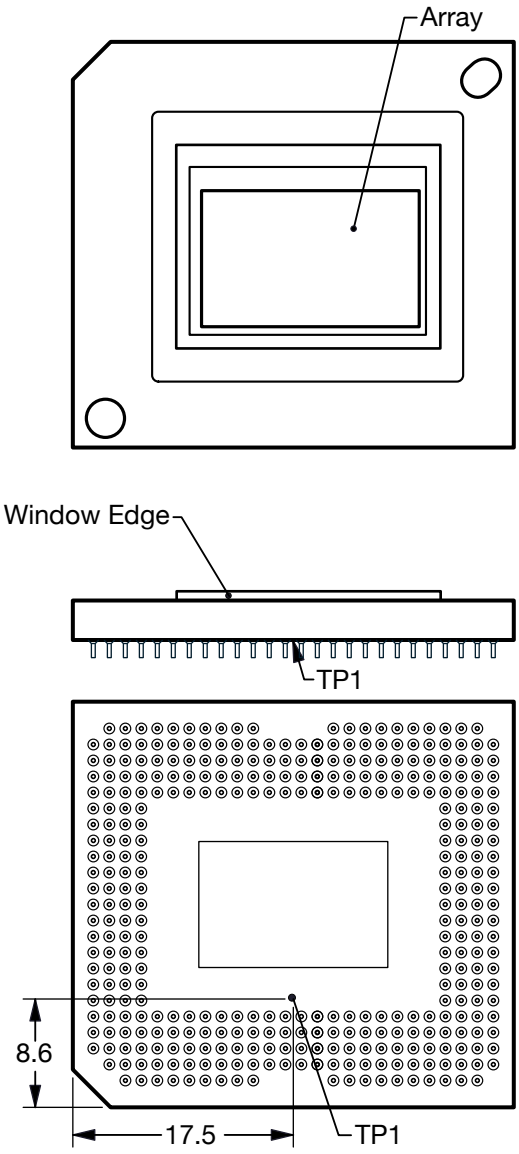


图 7-1. DMD Thermal Test Point

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from a measurement point on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in 图 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATIOM} \quad (2)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)

- $R_{ARRAY-TO-CERAMIC}$ = Thermal resistance of package specified in 节 6.5 from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.55

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.5 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 80 \text{ W (measured)} \quad (3)$$

$$T_{CERAMIC} = 45.0°C \text{ (measured)} \quad (4)$$

$$Q_{ELECTRICAL} = 1.5 \text{ W} \quad (5)$$

$$Q_{ARRAY} = 1.5 \text{ W} + (0.55 \times 80 \text{ W}) = 45.50 \text{ W} \quad (6)$$

$$T_{ARRAY} = 45.0°C + (45.50 \text{ W} \times 0.50°C/W) = 67.8°C \quad (7)$$

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 indicates that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the derating curve shown in 图 6-1.

The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use 方程式 8 to calculate the landed duty cycle of a given pixel during a given time period

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (8)$$

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities are shown in 表 7-2 and 表 7-3.

表 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
30%	50%	20%

表 7-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	30/70
0%	100%	0%	50/50
0%	0%	100%	20/80
0%	12%	0%	6/94
0%	0%	35%	7/93
60%	0%	0%	18/82
0%	100%	100%	70/30
100%	0%	100%	50/50
100%	100%	0%	80/20
0%	12%	35%	13/87
60%	0%	35%	25/75
60%	12%	0%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC4420 display controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC4420 display controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 图 7-2.

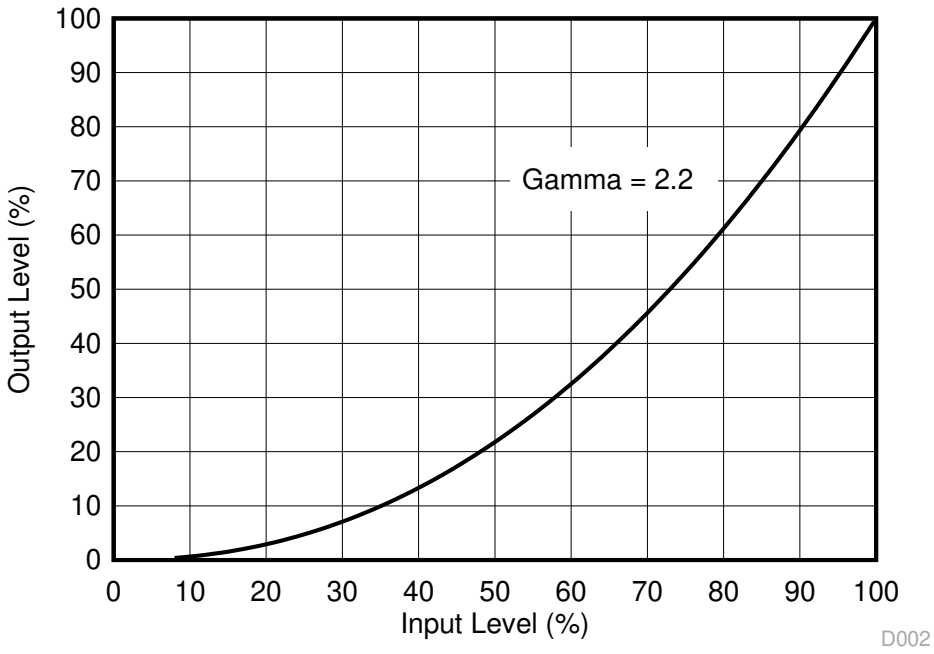


图 7-2. Example of Gamma = 2.2

From 图 7-2, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing which occurs before the DLPC4420 display controller.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the two DLPC4420 display controllers. Typical applications using the DLP801XE DMD include, smart projectors, enterprise projectors, large venue projectors and digital signage.

DMD power-up and power-down sequencing is strictly controlled by the DLPC4420 display controller through the DLPA300. Refer to *Power Supply Recommendations* for power-up and power-down specifications. To ensure reliable operation, the DLP801XE DMD must always be used with two DLPC4420 display controllers, a DLPA100 PMIC/Motor driver and a DLPA300 Micromirror Driver.

8.2 Typical Application

The DLP801XE DMD combined with two DLPC4420 display controllers and a power management device provides 4K+ resolution for bright, colorful display applications. A typical display system using RGB laser illumination combines the DLP801XE DMD, two DLPC4420 display controllers, DLPA300 micromirror driver and DLPA100 PMIC and motor driver. 图 8-1 shows a system block diagram for this configuration of the DLP 0.8-inch 4K+ chipset and additional system components needed. See 图 8-2 for a block diagram showing the system components needed along with the laser phosphor illumination for the DLP 0.8-inch 4K+chipset. The components include DLP801XE DMD, two DLPC4420 display controllers and DLPA100 PMIC and motor driver and a DLPA300 micromirror driver.

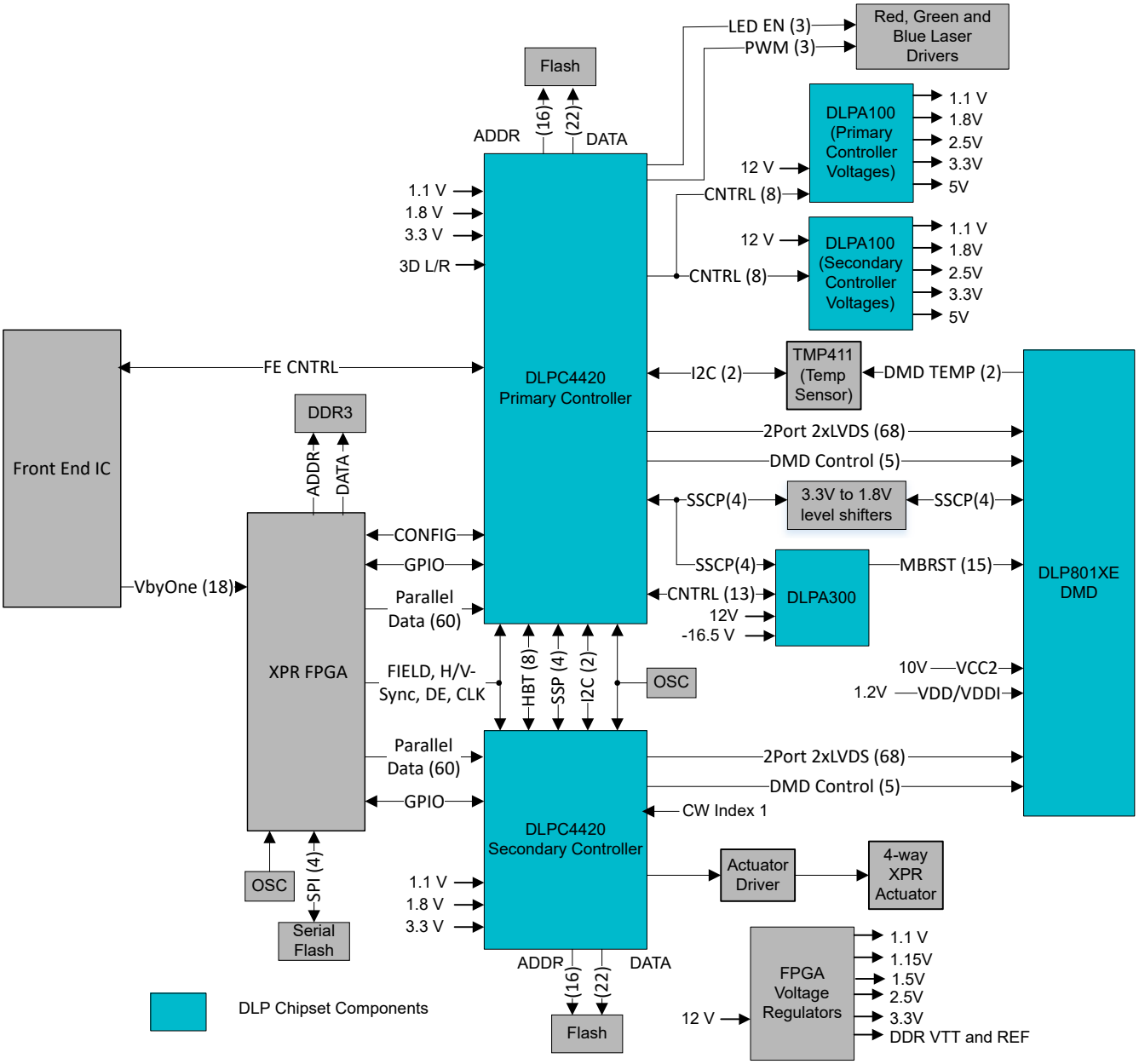


图 8-1. Typical 4K+ RGB Laser Application

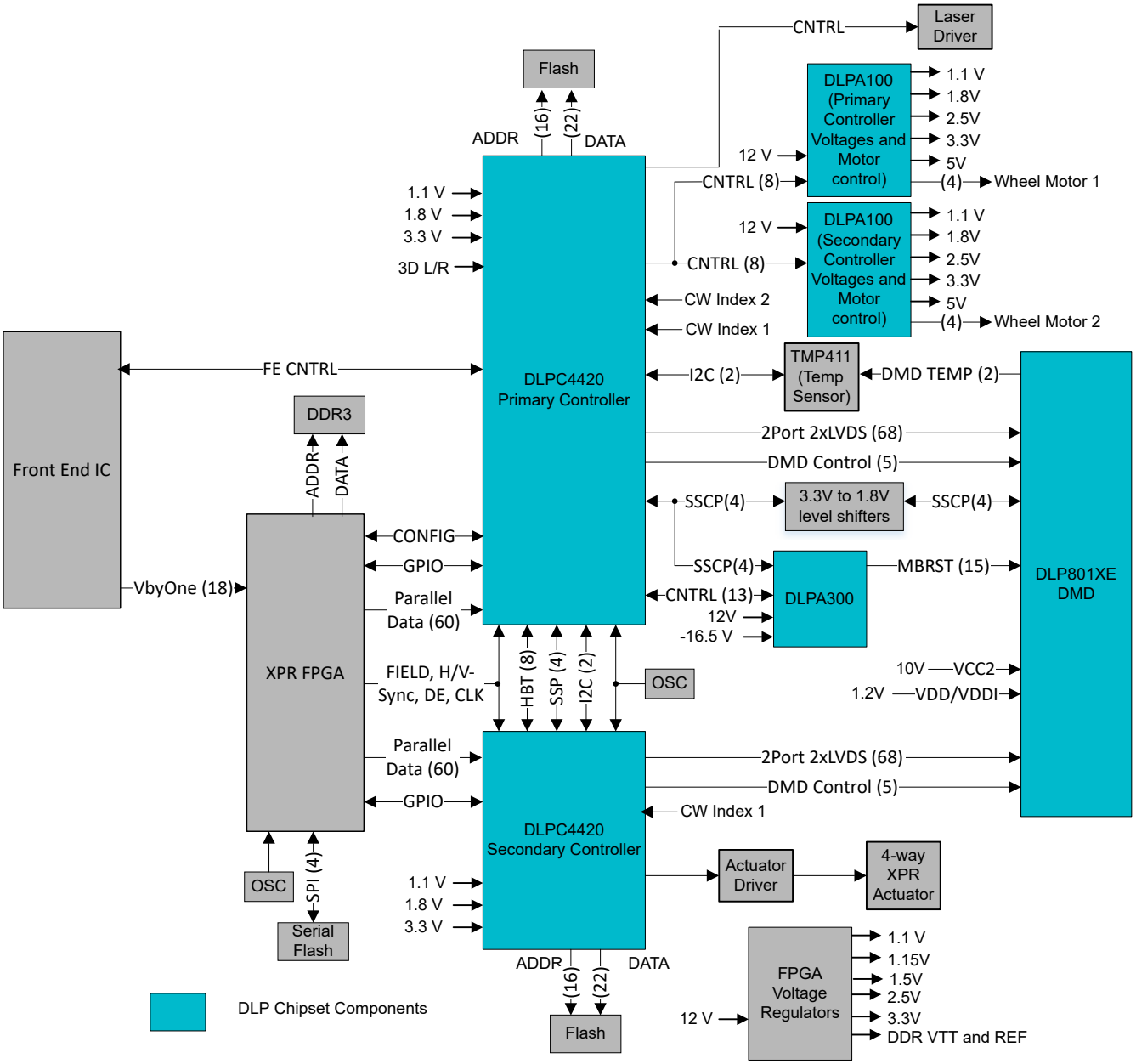


图 8-2. Typical 4k UHD Laser Phosphor Application

8.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness has a major effect on the overall system design and size.

The display system uses the DLP801XE DMD as the core imaging device and contains a 0.8-inch array of micromirrors. The DLPC4420 display controller is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver and driving the DMD over a high-speed LVDS interface. The DLPA100 PMIC serves as a voltage regulator for the controller, and color filter wheel and phosphor wheel motor control. The DLPA300 provides the DMD reset control.

8.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP801XE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with two DLPC4420 display controllers, the DLPA300 micromirror driver and the DLPA100 PMIC and motor driver.

8.2.3 Application Curve

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determines the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. 图 8-3 describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit.

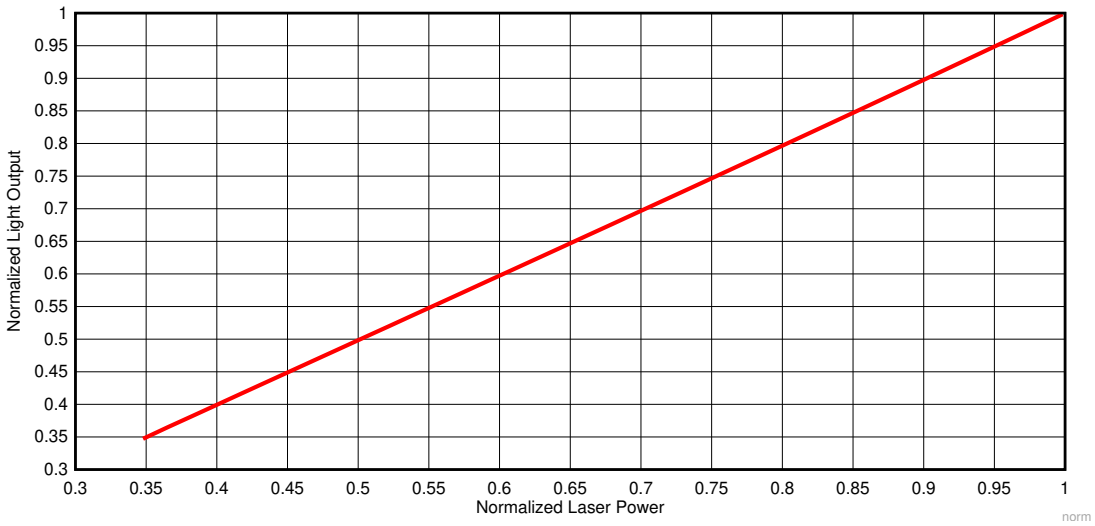
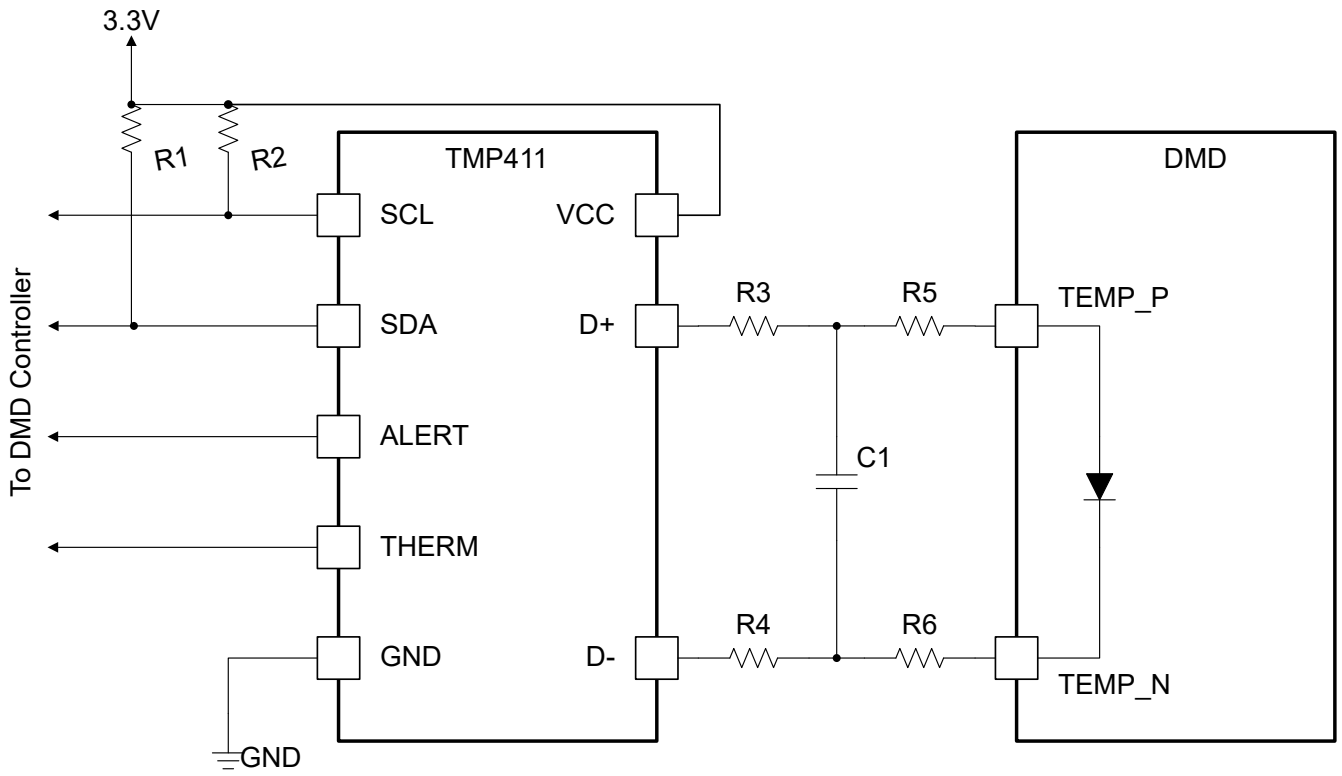


图 8-3. Normalized Light Output vs. Normalized Laser Power for Laser Phosphor Illumination

8.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in 图 8-4. The software application contains functions to configure the TMP411 to read the DLP801XE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, etc. All communication between the TMP411 and the DLPC4420 display controller happens over the I^2C interface. The TMP411 connects to the DMD via pins outlined in 节 5.

Leave TEMP_N and TEMP_P pins unconnected (NC) if the temp sensor is not used.



A. Details omitted for clarity.
B. See the TMP411 datasheet for system board layout recommendation.
C. See the TMP411 datasheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
D. R5 = 0 Ω. R6 = 0 Ω. Place 0-Ω resistors close to the DMD package pins.

图 8-4. TMP411 Sample Schematic

9 Power Supply Recommendations

9.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: VDD, VDDI, and VCC2. VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC4420 display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VDD, VDDI and VCC2 power supplies have to be coordinated during power-up and power-down operations. VSS must also be connected. Failure to meet any of the below requirements results in a significant reduction in the reliability and lifetime of the DMD. Refer to 图 9-1.

9.2 DMD Power Supply Power-Up Procedure

- During power-up, VDD and VDDI must always start and settle before VCC2 is are applied to the DMD.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in 节 6.1 and in 节 6.4.
- During power-up, LVCMOS input pins must not be driven high until after VDD and VDDI have settled at operating voltages listed in 节 6.4 table.

9.3 DMD Power Supply Power-Down Procedure

- During power-down, VDD and VDDI must be supplied until after VCC2 is discharged to within the specified limit of ground. Refer to 节 6.4.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in 节 6.1 and in 节 6.4.
- During power-down, LVCMOS input pins must be less than specified in 节 6.4.

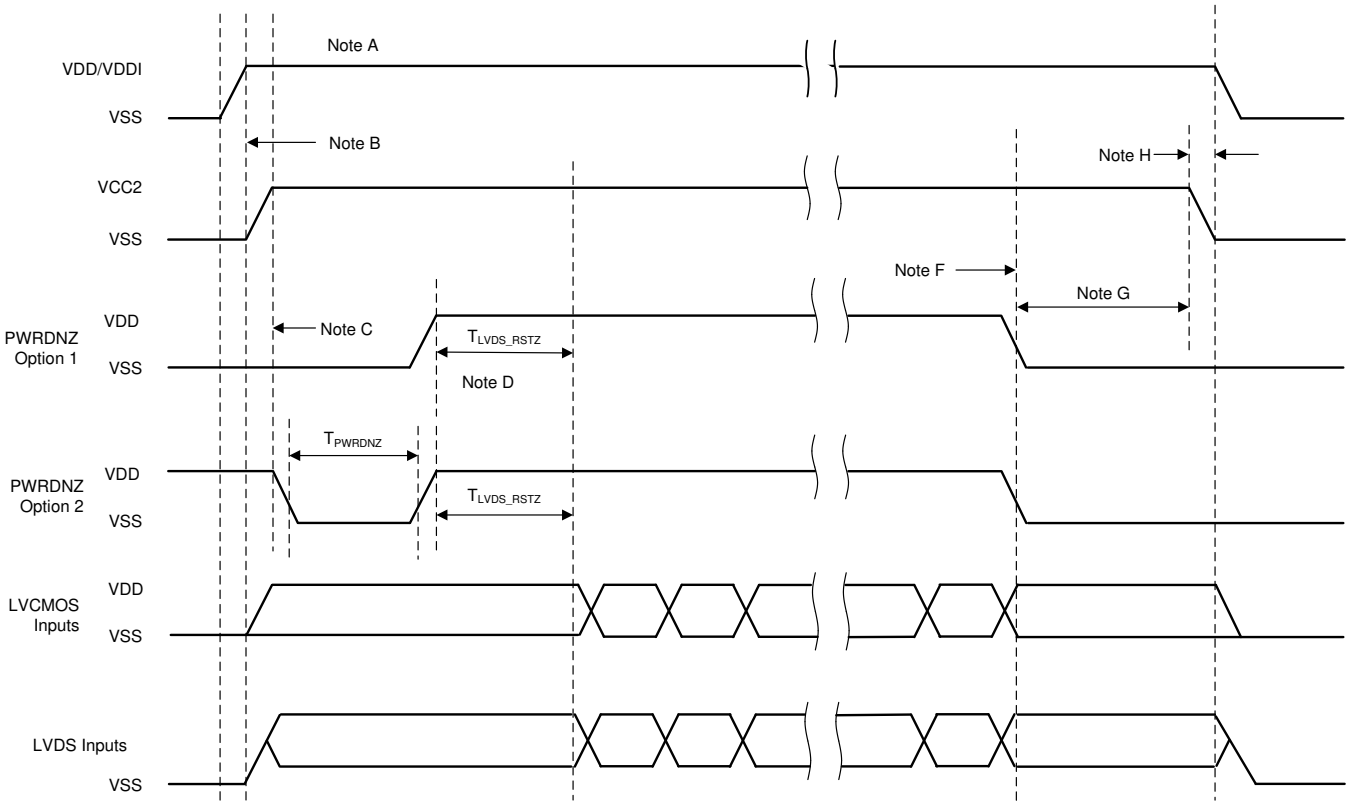


图 9-1. DMD Power Supply Sequencing Requirements

A. See *Pin Configuration and Functions* for pin functions.
B. VDD must be up and stable prior to VCC2 powering up.
C. PWRDNZ has two turn on options. Option 1: PWRDNZ does not go high until VDD and VCC2 are up and stable, or Option 2: PWRDNZ must be pulsed low for a minimum of T_{PWRDNZ}, or 10 ns after VDD and VCC2 are up and stable.
D. There is a minimum of T_{LVDS_ARSTZ}, or 2 μs, wait time from PWRDNZ going high for the LVDS receiver to recover.
E. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates the PWRDNZ and disables VCC2.
F. Under power-loss conditions, where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, PWRDNZ goes low.
G. VDD must remain high until after VCC2 goes low.
H. To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit in 节 6.4.

10 Layout

10.1 Layout Guidelines

The DLP801XE DMD is part of a chipset that is controlled by the two DLPC4420 display controllers in conjunction with the DLP300 micromirror driver and the DLPA100 power and motor driver. These guidelines are targeted at designing a PCB board with the DLP801XE DMD. The DLP801XE DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic utilizing dual edge clock rates up to 400MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTL signals. Solid planes are required for DMD_P1P8V and Ground. The target impedance for the PCB is 50 Ω ±10% with the LVDS traces being 100 Ω ±10% differential. TI recommends using an 8-layer stack-up as described in 表 10-1.

10.2 Layout Example

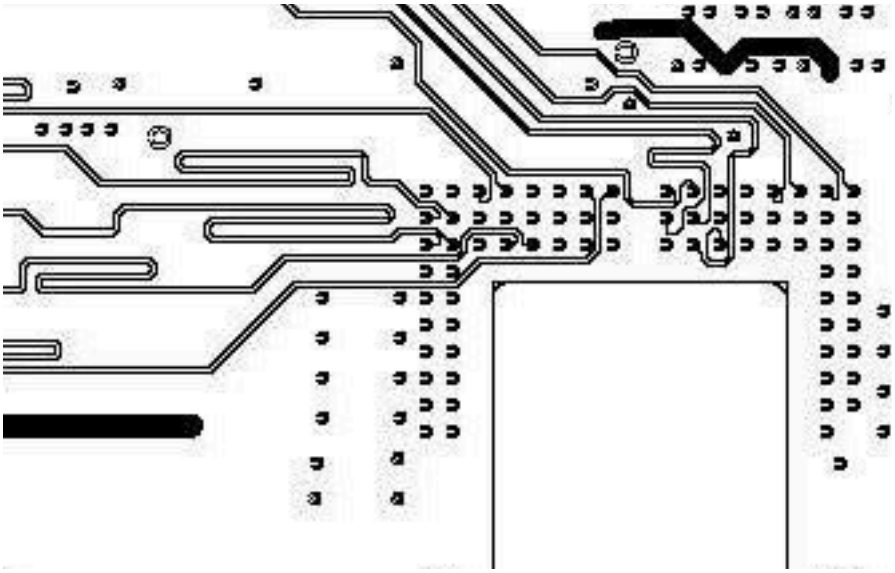


图 10-1. Typical example for matching LVDS signal lengths by serpentine sections

10.2.1 Layers

The layer stack-up and copper weight for each layer is shown in 表 10-1. Small sub-planes are allowed on signal routing layers to connect components to major sub-planes on top/bottom layers if necessary.

表 10-1. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A - DMD only	1.5	DMD, escapes, low frequency signals, power sub-planes.
2	Ground	1	Solid ground plane (net GND).
3	Signal	0.5	50 Ω and 100 Ω differential signals
4	Ground	1	Solid ground plane (net GND)
5	VDD and VDDI	1	+1.8-V power plane
6	Signal	0.5	50 Ω and 100 Ω differential signals
7	Ground	1	Solid ground plane (net GND).
8	Side B - All other Components	1.5	Discrete components, low frequency signals, power sub-planes

10.2.2 Impedance Requirements

TI recommends that the board has matched impedance of 50 Ω ±10% for all signals. The exceptions are listed in 表 10-2.

表 10-2. Special Impedance Requirements

SIGNAL TYPE	SIGNAL NAME	IMPEDANCE (Ω)
A channel LVDS differential pairs	DDAP(0:15), DDAN(0:1A)	100 ±10% differential across each pair
	DCLKA_P, DCLKA_N	
	SCTRL_AP, SCTRL_AN	
B channel LVDS differential pairs	DDBP(0:15), DDBN(0:15)	100 ±10% differential across each pair
	DCLKB_P, DCLKB_N	
	SCTRL_BP, SCTRL_BN	
C channel LVDS differential pairs	DDCP(0:15), DDCN(0:15)	100 ±10% differential across each pair
	DCLKC_P, DCLKC_N	
	SCTRL_CP, SCTRL_CN	
D channel LVDS differential pairs	DDDP(0:15), DDDN(0:15)	100 ±10% differential across each pair
	DCLKD_P, DCLKD_N	
	SCTRL_DP, SCTRL_DN	

10.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005” /0.005” design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1” minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

10.2.3.1 Voltage Signals

表 10-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
GND	15	Maximize trace width to connecting pin
3.3-V Supply Rail	15	Maximize trace width to connecting pin
VDD, VDDI	15	Maximize trace width to connecting pin
MBRST(0,14)	15	Use 10 mil etch to connect all signals/voltages from DLPA300 to DLP801XE
VCC2	15	Create mini plane from Voltage regulator to DLP801XE

11 Device and Documentation Support

11.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.2 Device Support

11.2.1 Device Nomenclature

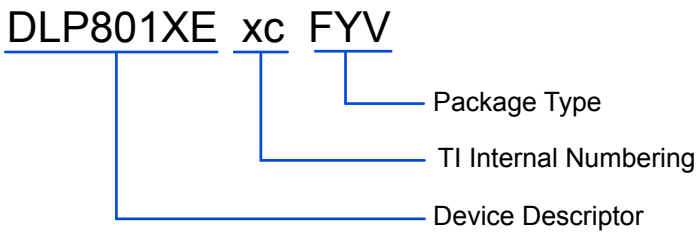


图 11-1. Part Number Description

11.3 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 图 11-2. The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

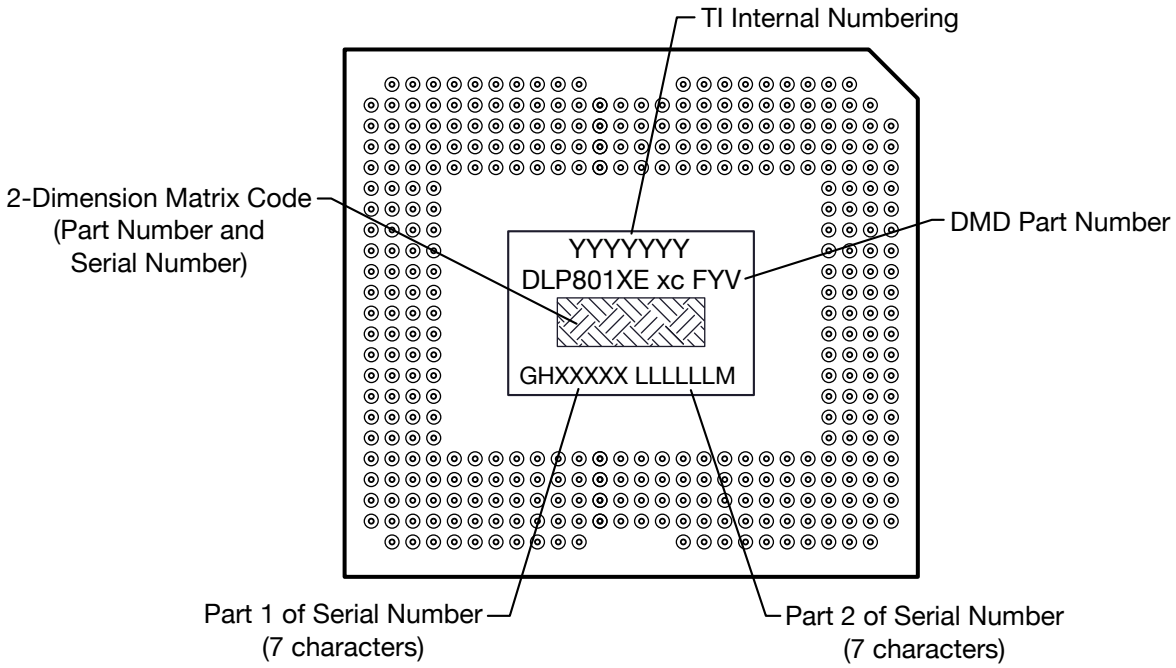


图 11-2. DMD Marking Locations

11.4 Documentation Support

11.4.1 Related Documentation

For related documentation see the following:

- *DLPA100 Power and Motor Driver Data Sheet*
- *DLPA300 DMD Micromirror Driver Data Sheet*
- *DLPC4420 Display Controller Data Sheet*

11.5 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.6 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.7 Trademarks

TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.8 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.9 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking
DLP801XEA0FYV	PREVIEW	CPGA	FYV	350	21	Green	Call TI	NA		节 11.3

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP801XEA0FYV	ACTIVE	CPGA	FYV	350	21	RoHS & Green	Call TI	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

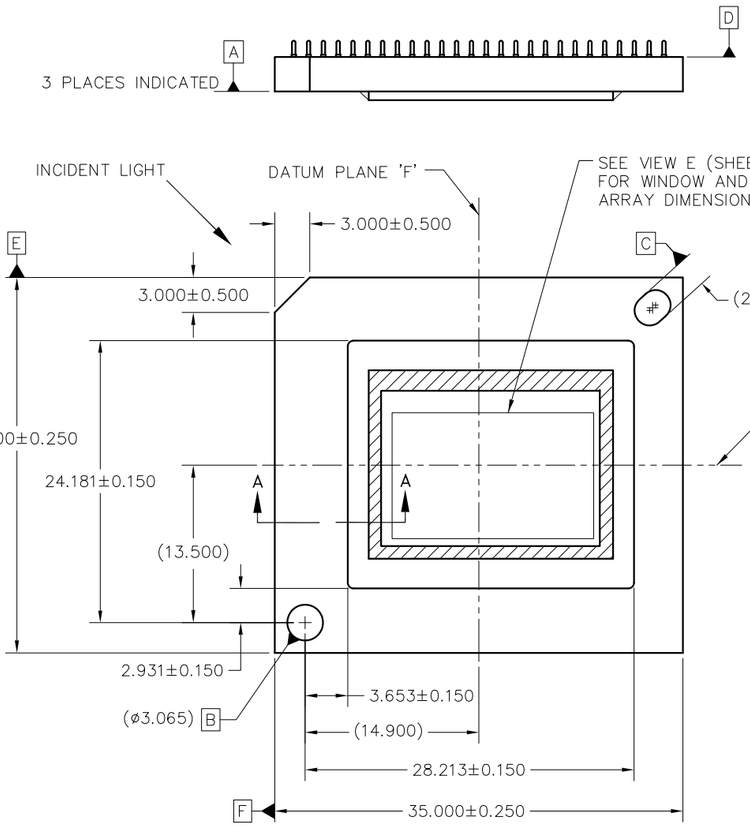
DWG NO 2517029 SH 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2187184, INITIAL RELEASE	04/22/2020	F. ARMSTRONG

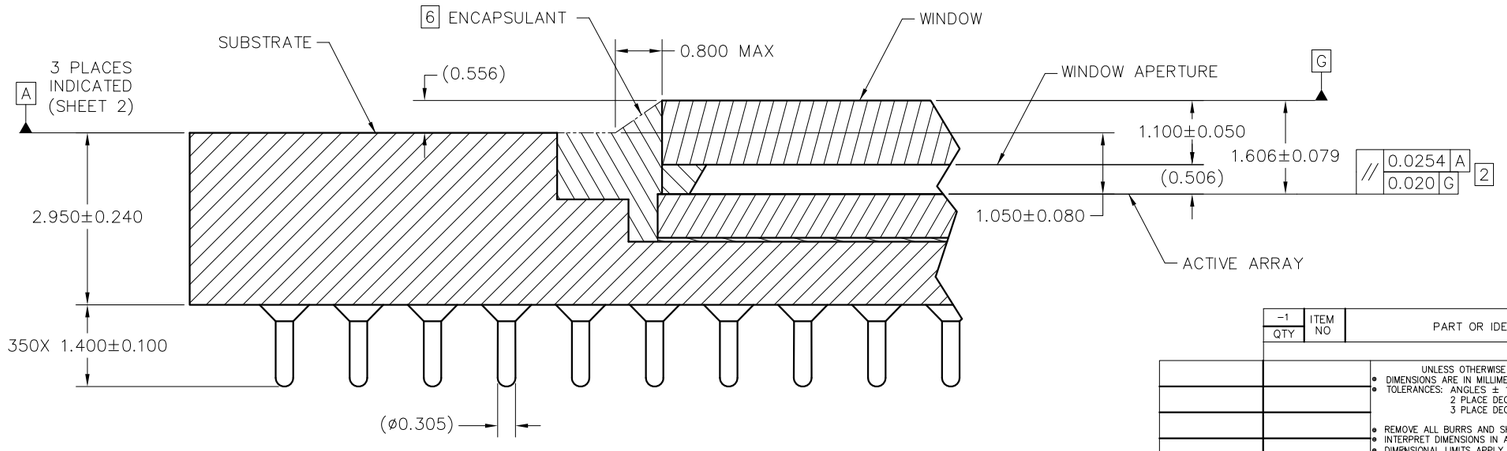
NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES ARE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.



F – SHT. 4

F – SHT. 4



SECTION A–A
SCALE 20/1

PARTS LIST

–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5–1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

DWN	F. ARMSTRONG 03/05/2020
ENGR	F. ARMSTRONG 03/05/2020
QA	S. HUDGENS 04/27/2020
CQE	M. DORAK 04/27/2020

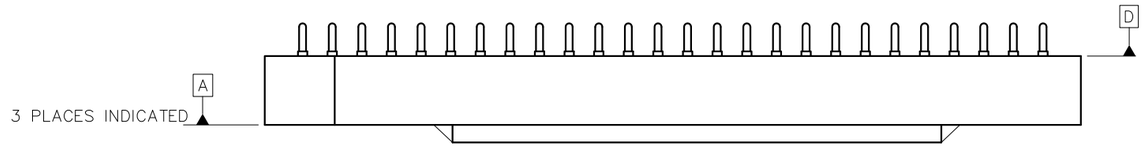
TEXAS INSTRUMENTS
Dallas, Texas

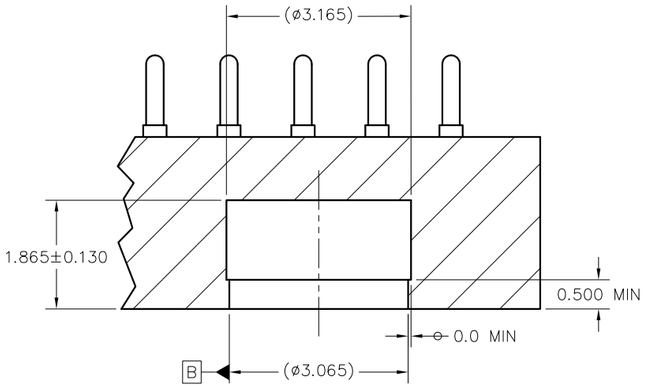
ICD, MECHANICAL, DMD
.8" WUXGA MHEP 2XLVDS
SERIES 600 (FYV PACKAGE)

THIRD ANGLE PROJECTION	NEXT ASSY	USED ON
	NONE	0314DA
	APPLICATION	

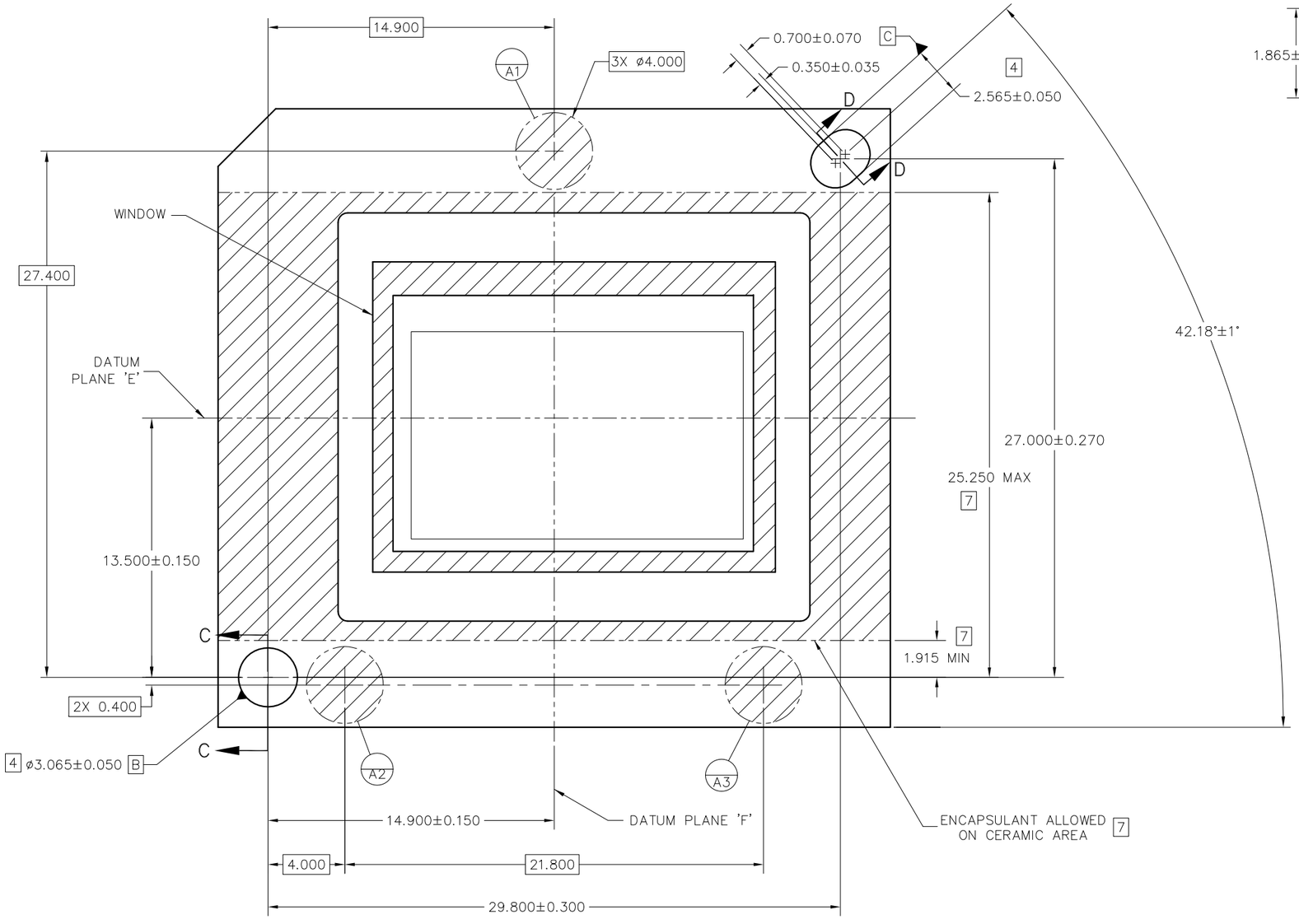
SIZE D | DRAWING NO 2517029 | REV A | SCALE 4/1 | SHEET 1 OF 4

ACED1g

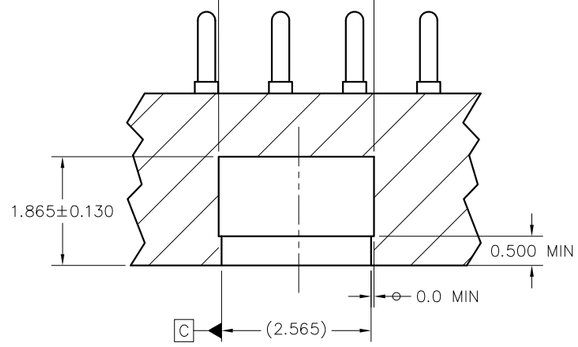




SECTION C–C
DATUM B
SCALE 16/1



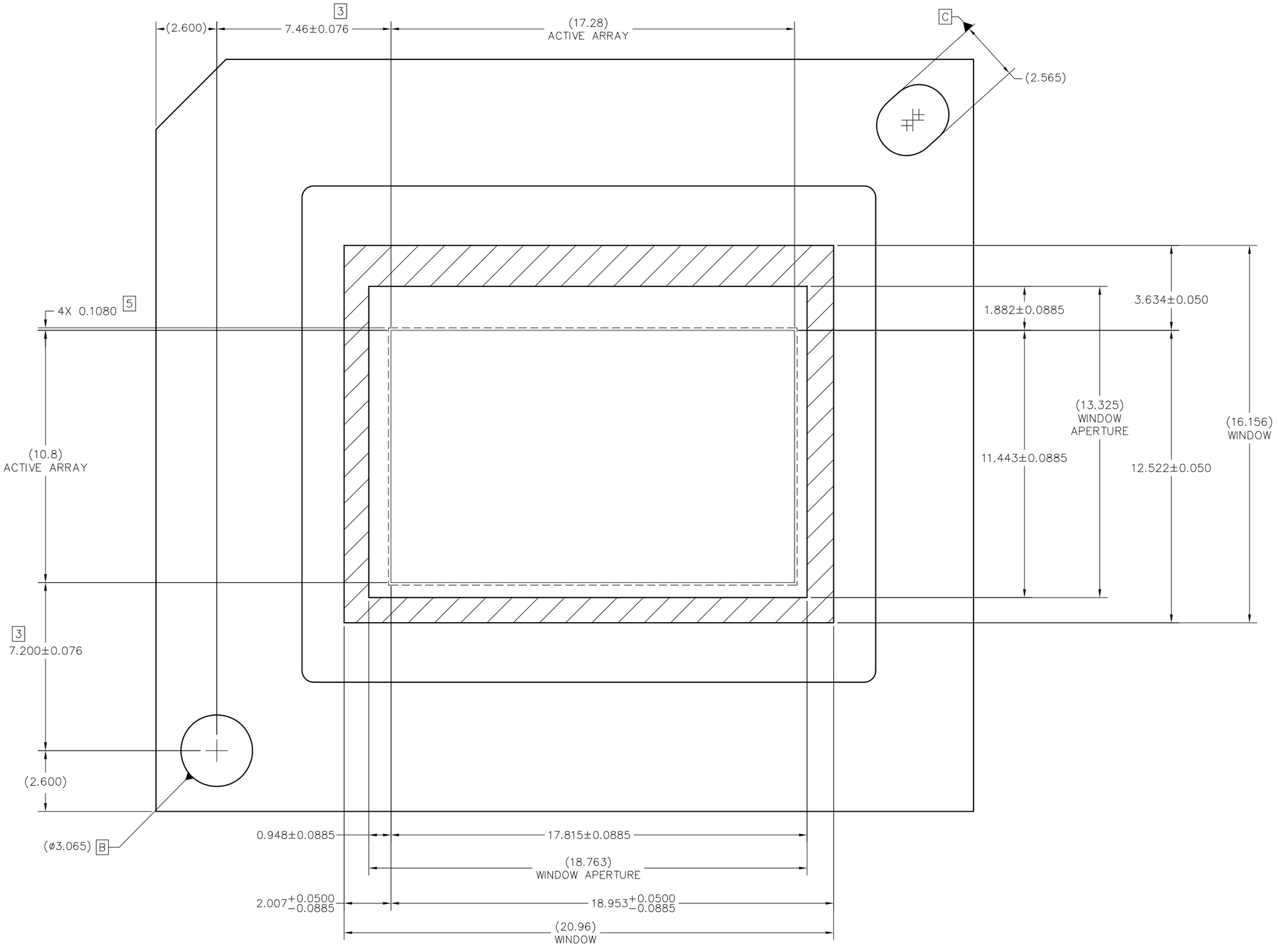
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2517029	REV A
		SCALE 4/1	SHEET 2	

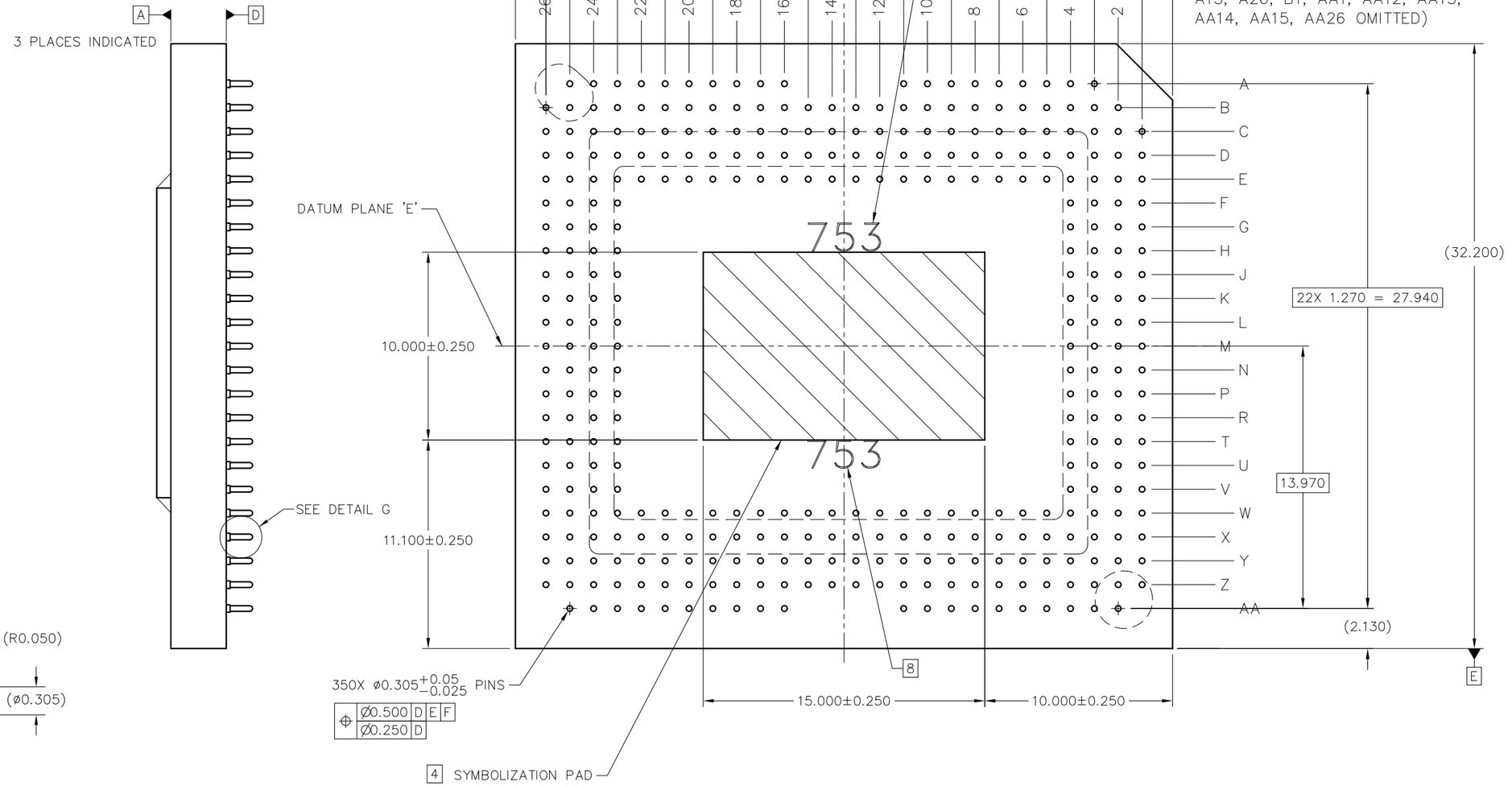
ACED2c



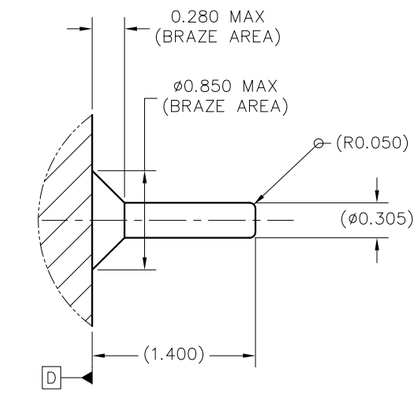
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

Texas Instruments, Dallas, Texas	DWN	DATE	SIZE D	DRAWING NO 2517029	REV A
	ISSUE DATE		SCALE 4/1	SHEET 3	

ACED2c



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1



DETAIL G (350 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D / SCALE 4/1 / DRAWING NO 2517029 / REV A / SHEET 4

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