

DRV2901 具有宽电源电压、用于超声波清洗的单通道 PWM 输入压电传感器驱动器

1 特性

- 12V 至 48V 宽电源电压工作范围
- 支持高达 50W 的峰值功率
- 具有 90mΩ 输出 MOSFET 的高效功率级
- 用于加电保护的上电复位，无任何电源定序
- 集成式自保护电路，包括
 - 欠压保护
 - 过热保护
 - 过载保护
 - 短路保护
- 采用 44 引脚 HTSSOP 封装 (DDV)

2 应用范围

- 热成像摄像头
- 交通监控摄像头
- 机器视觉摄像机
- 无线安防摄像头
- 无人机视觉

3 说明

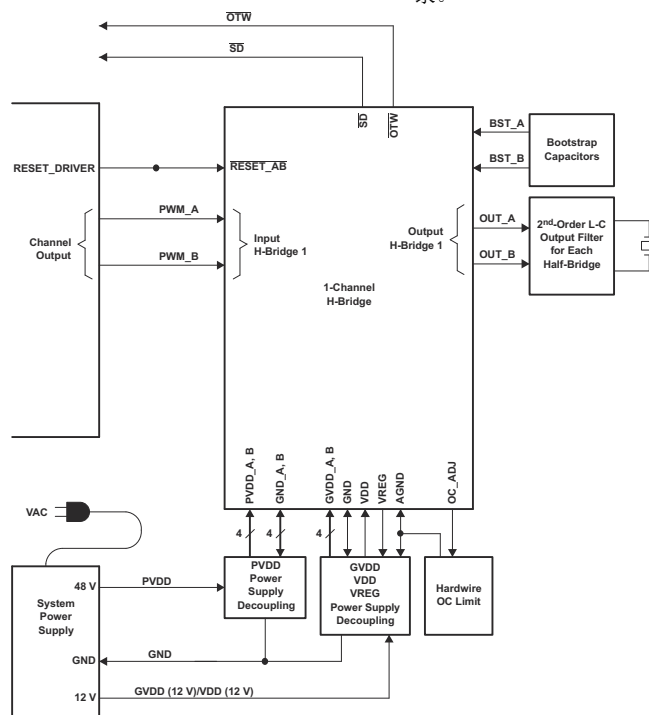
DRV2901 是一款高性能镜头清洁剂传感器驱动器。该系统仅需一个简单的无源 LC 解调滤波器即可提供高质量、高效的放大功能，并符合 EMI 标准。该器件需要两个电源，一个为 12V，用于 GVDD 和 VDD，另外一个为 12V 至 48V，用于 PVDD。由于内部上电复位，DRV2901 不需要上电时序控制。

DRV2901 具有一个片上集成创新保护系统，可保护器件免受可能损坏系统的各种故障条件的影。这些保护是短路保护、过流保护、欠压保护和过热保护。DRV2901 具有一个全新的专有限流电路，可降低在高电平瞬态期间器件关断的可能性。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|---------|---------------------------|----------------|
| DRV2901 | 44 引脚散热薄型小外形尺寸封装 (HTSSOP) | 14.0mm x 6.1mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



DRV2901 功能方框图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| DATE | REVISION | NOTES |
|--------------|----------|------------------|
| January 2023 | * | Initial release. |

5 Pin Configuration and Functions

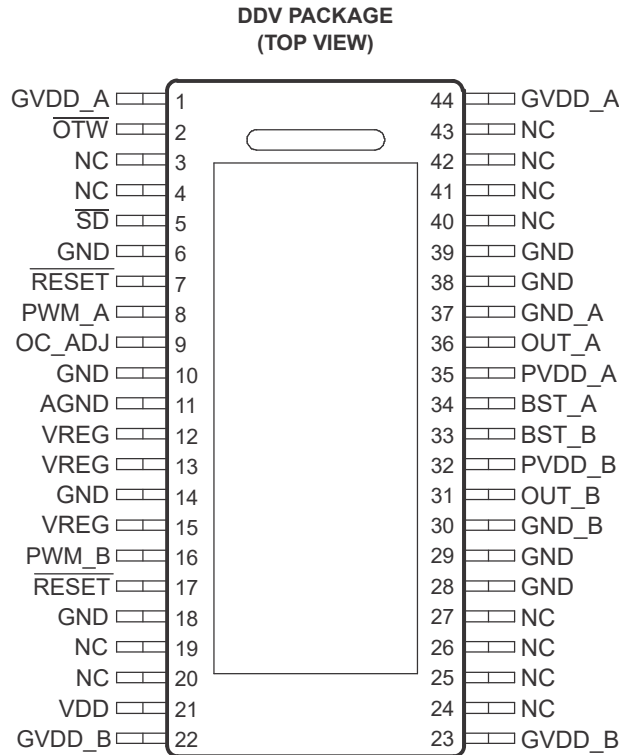


图 5-1. DDV Package 44-Pin HTSSOP PowerPad Top View

表 5-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|--------|--|---------------------|---|
| NAME | NO. | | |
| AGND | 11 | P | Analog ground |
| BST_A | 34 | P | HS bootstrap supply (BST), external .033- μ F capacitor to OUT_A required |
| BST_B | 33 | P | HS bootstrap supply (BST), external .033- μ F capacitor to OUT_B required |
| GND | 6, 10, 14, 18, 28, 29, 38, 39 | P | Ground. |
| GND_A | 37 | P | Power ground for half-bridge A |
| GND_B | 30 | P | Power ground for half-bridge B |
| GVDD_A | 1, 44 | P | Gate-drive voltage supply requires 0.1- μ F capacitor to AGND |
| GVDD_B | 22, 23 | P | Gate-drive voltage supply requires 0.1- μ F capacitor to AGND |
| NC | 3, 4, 19, 20, 24, 25, 26, 27, 40, 41, 42, 43 | — | Do not connect. |
| OC_ADJ | 9 | O | Analog overcurrent programming pin requires resistor to ground |
| OTW | 2 | O | Overtemperature warning signal, open-drain, active-low |
| OUT_A | 36 | O | Output, half-bridge A |
| OUT_B | 31 | O | Output, half-bridge B |
| PVDD_A | 35 | P | Power supply input for half-bridge A requires close decoupling of 0.01- μ F capacitor in parallel with a 1.0- μ F capacitor to GND_A. |
| PVDD_B | 32 | P | Power supply input for half-bridge B requires close decoupling of 0.01- μ F capacitor in parallel with a 1.0- μ F capacitor to GND_B. |
| PWM_A | 8 | I | Input signal for half-bridge A |

表 5-1. Pin Functions (continued)

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------|------------|---------------------|--|
| NAME | NO. | | |
| PWM_B | 16 | I | Input signal for half-bridge B |
| RESET | 7, 17 | I | Reset signal for half-bridge A and B, active-low |
| SD | 5 | O | Shutdown signal, open-drain, active-low |
| VDD | 21 | P | Power supply for digital voltage regulator requires a 47- μ F capacitor in parallel with a 0.1- μ F capacitor to GND for decoupling. |
| VREG | 12, 13, 15 | P | Digital regulator supply filter pin requires 0.1- μ F capacitor to AGND. |

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted ⁽¹⁾

| | |
|--|-------------------|
| VDD to AGND | - 0.3 V to 13.2 V |
| GVDD_X to AGND | - 0.3 V to 13.2 V |
| PVDD_X to GND_X ⁽²⁾ | - 0.3 V to 71 V |
| OUT_X to GND_X ⁽²⁾ | - 0.3 V to 71V |
| BST_X to GND_X ⁽²⁾ | - 0.3 V to 79.7 V |
| VREG to AGND | - 0.3 V to 4.2 V |
| GND_X to GND | - 0.3 V to 0.3 V |
| GND_X to AGND | - 0.3 V to 0.3 V |
| GND to AGND | - 0.3 V to 0.3 V |
| PWM_X, OC_ADJ, M1, M2, M3 to AGND | - 0.3 V to 4.2 V |
| RESET_X, \overline{SD} , \overline{OTW} to AGND | - 0.3 V to 7 V |
| Maximum continuous sink current (\overline{SD} , \overline{OTW}) | 9 mA |
| Maximum operating junction temperature range, T _J | 0°C to 125°C |
| Storage temperature | - 40°C to 125°C |
| Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Minimum pulse duration, low | 50 ns |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per AEC Q100-011 | ±500 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

| | | | MIN | TYP | MAX | UNIT |
|---------------------|--|---|------|-----|------|------|
| PVDD_X | Half-bridge supply | DC supply voltage | 0 | 50 | 52.5 | V |
| GVDD_X | Supply for logic regulators and gate-drive circuitry | DC supply voltage | 10.8 | 12 | 13.2 | V |
| VDD | Digital regulator input | DC supply voltage | 10.8 | 12 | 13.2 | V |
| L _{Output} | Output-filter inductance | Minimum output inductance under short-circuit condition | 5 | 10 | | μH |
| F _{PWM} | PWM frame rate | | 192 | 384 | 432 | kHz |
| T _J | Junction temperature | | 0 | | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DRV2901 | UNIT |
|-------------------------------|--|----------------------------|------|
| | | DDV 44-PINS HTSSOP | |
| | | JEDEC STANDARD 4 LAYER PCB | |
| R _{θJA} | Junction-to-ambient thermal resistance | 50.7 | °C/W |

| THERMAL METRIC ⁽¹⁾ | | DRV2901 | | UNIT |
|-------------------------------|--|----------------------------|--|------|
| | | DDV 44-PINS HTSSOP | | |
| | | JEDEC STANDARD 4 LAYER PCB | | |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.36 | | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 24.4 | | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 0.19 | | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 24.2 | | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

$R_L = 6 \Omega$, $F_{PWM} = 384 \text{ kHz}$, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

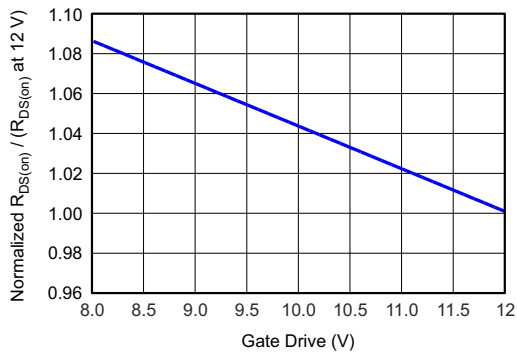
| PARAMETER | | TEST CONDITIONS | DRV2900 | | | UNIT |
|---|--|---|---------|-----|------|------------|
| | | | MIN | TYP | MAX | |
| Internal Voltage Regulator and Current Consumption | | | | | | |
| VREG | Voltage regulator, only used as a reference node | VDD = 12 V | 2.95 | 3.3 | 3.65 | V |
| IVDD | VDD supply current | Operating, 50% duty cycle | 10 | | | mA |
| | | Idle, reset mode | 6 | | | |
| IGVDD_X | Gate supply current per half-bridge | 50% duty cycle | 8 | | | mA |
| | | Reset mode | 0.3 | | | |
| IPVDD_X | Half-bridge idle current | 50% duty cycle, without output filter or load | 15 | | | mA |
| | | Reset mode, no switching | 500 | | | |
| Output Stage MOSFETs | | | | | | |
| $R_{DSon,LS}$ | Drain-to-source resistance, LS | $T_J = 25^\circ\text{C}$, includes metallization resistance, GVDD = 12 V | 90 | | | m Ω |
| $R_{DSon,HS}$ | Drain-to-source resistance, HS | $T_J = 25^\circ\text{C}$, includes metallization resistance, GVDD = 12 V | 90 | | | m Ω |
| I/O Protection | | | | | | |
| $V_{UVP,G}$ | Undervoltage protection limit, GVDD_X | | 8.5 | | | V |
| $V_{UVP,hyst}^{(1)}$ | | | 400 | | | mV |
| OTW ⁽¹⁾ | Overtemperature warning | | 115 | 125 | 135 | °C |
| OTW _{HYST} ⁽¹⁾ | Temperature drop needed below OTW temp. for OTW to be inactive after the OTW event | | 25 | | | °C |
| OTE ⁽¹⁾ | Overtemperature error | | 145 | 155 | 165 | °C |
| OTE-OTW _{differential} ⁽¹⁾ | OTE-OTW differential | | 25 | | | °C |
| OTE _{HYST} ⁽¹⁾ | A reset needs to occur for \overline{SD} for be released following an OTE event. | | 25 | | | °C |
| OLPC | Overload protection counter | $F_{PWM} = 384 \text{ kHz}$ | 1.3 | | | ms |
| I_{OC} | Overcurrent limit protection | Resistor—programmable, nominal, $R_{OCP} = 22 \text{ k}\Omega$ | 12 | | | A |
| I_{OCT} | Overcurrent response time | Time from application of short condition to Hi-Z of affected 1/2 bridge | 250 | | | ns |
| R_{OCP} | OC programming resistor range | Resistor tolerance = 5% | 22 | 69 | | k Ω |

$R_L = 6\ \Omega$, $F_{PWM} = 384\ \text{kHz}$, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

| PARAMETER | TEST CONDITIONS | DRV2901 | | | UNIT |
|--------------------------------------|---|---|-----|-----|---------------|
| | | MIN | TYP | MAX | |
| R_{PD} | Internal pull-down resistor at the output of each half-bridge | Connected when $\overline{\text{RESET}}$ is active to provide bootstrap capacitor charge. Not used in SE mode | | | $k\Omega$ |
| Static Digital Specifications | | | | | |
| V_{IH} | High-level input voltage | PWM_A, PWM_B, RESET_AB | | | V |
| V_{IL} | Low-level input voltage | | | | V |
| Leakage | Input leakage current | -100 | | 100 | μA |
| OTW/SHUTDOWN (SD) | | | | | |
| R_{INT_PU} | Internal pullup resistance, $\overline{\text{OTW}}$ to VREG, $\overline{\text{SD}}$ to VREG | 20 | 26 | 35 | $k\Omega$ |
| V_{OH} | High-level output voltage | Internal pullup resistor | | | V |
| | | External pullup of 4.7 $k\Omega$ to 5 V | | | |
| V_{OL} | Low-level output voltage | $I_O = 4\ \text{mA}$ | | | V |
| FANOUT | Device fanout $\overline{\text{OTW}}$, $\overline{\text{SD}}$ | No external pullup | | | Devices |

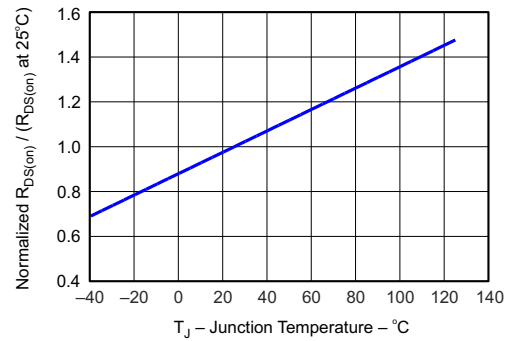
(1) Specified by design

6.6 Typical Characteristics



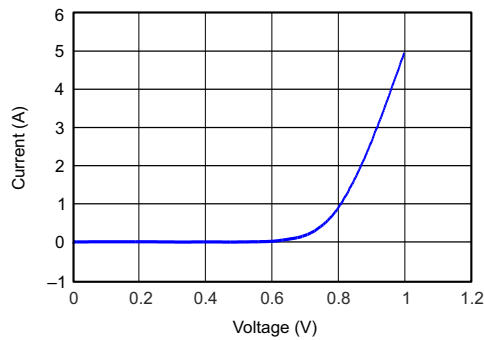
$T_J = 25^\circ\text{C}$

图 6-1. Normalized $R_{DS(on)}$ vs Gate Drive



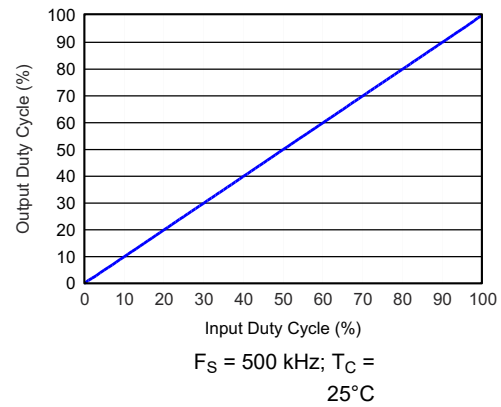
GVDD = 12 V

图 6-2. Normalized $R_{DS(on)}$ vs Junction Temperature



$T_J = 25^\circ\text{C}$

图 6-3. Drain To Source Diode Forward On Characteristics



$F_S = 500 \text{ kHz}; T_C = 25^\circ\text{C}$

图 6-4. Output Duty Cycle vs Input Duty Cycle

7 Detailed Description

7.1 Block Diagrams

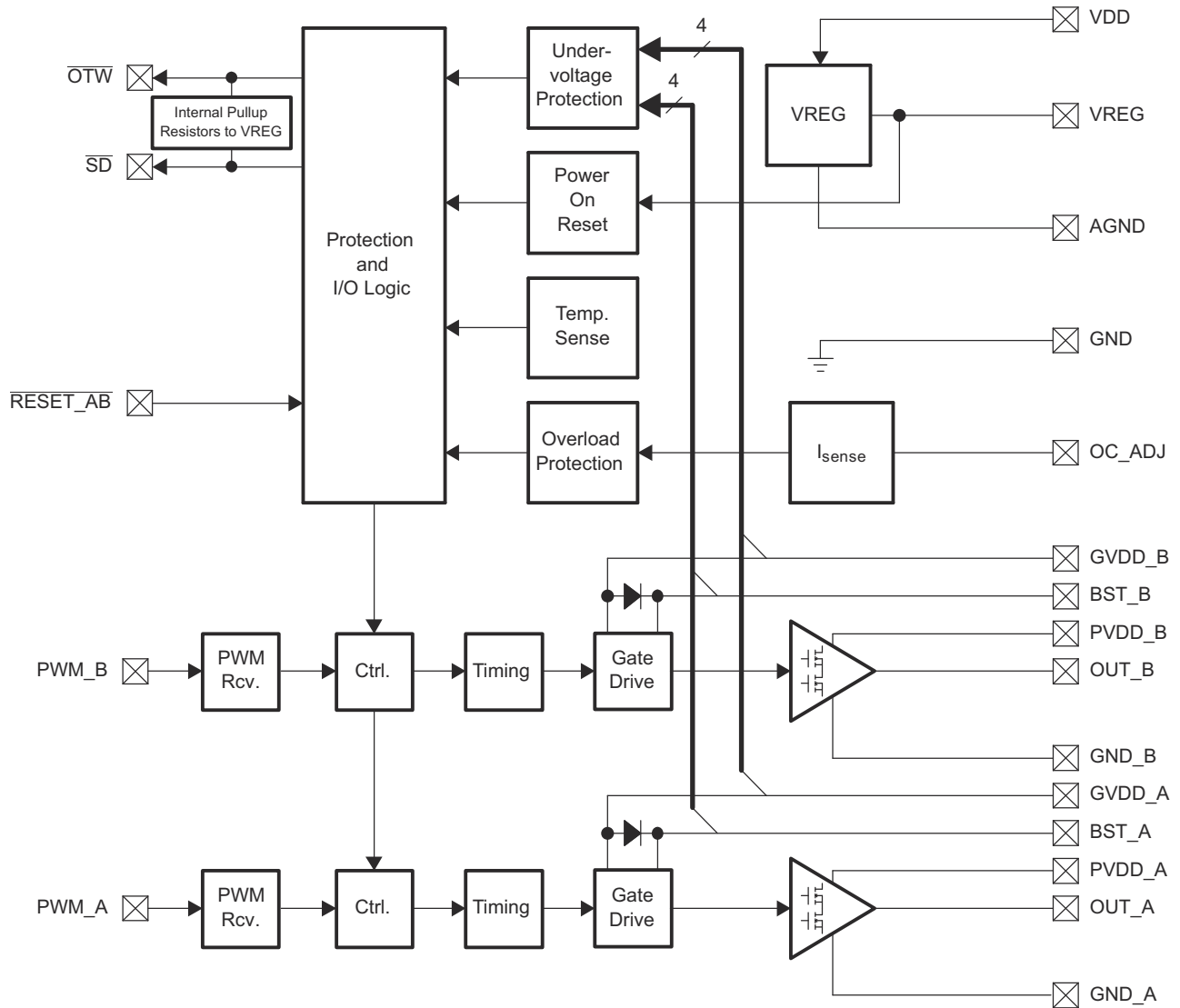


图 7-1. System Block Diagram

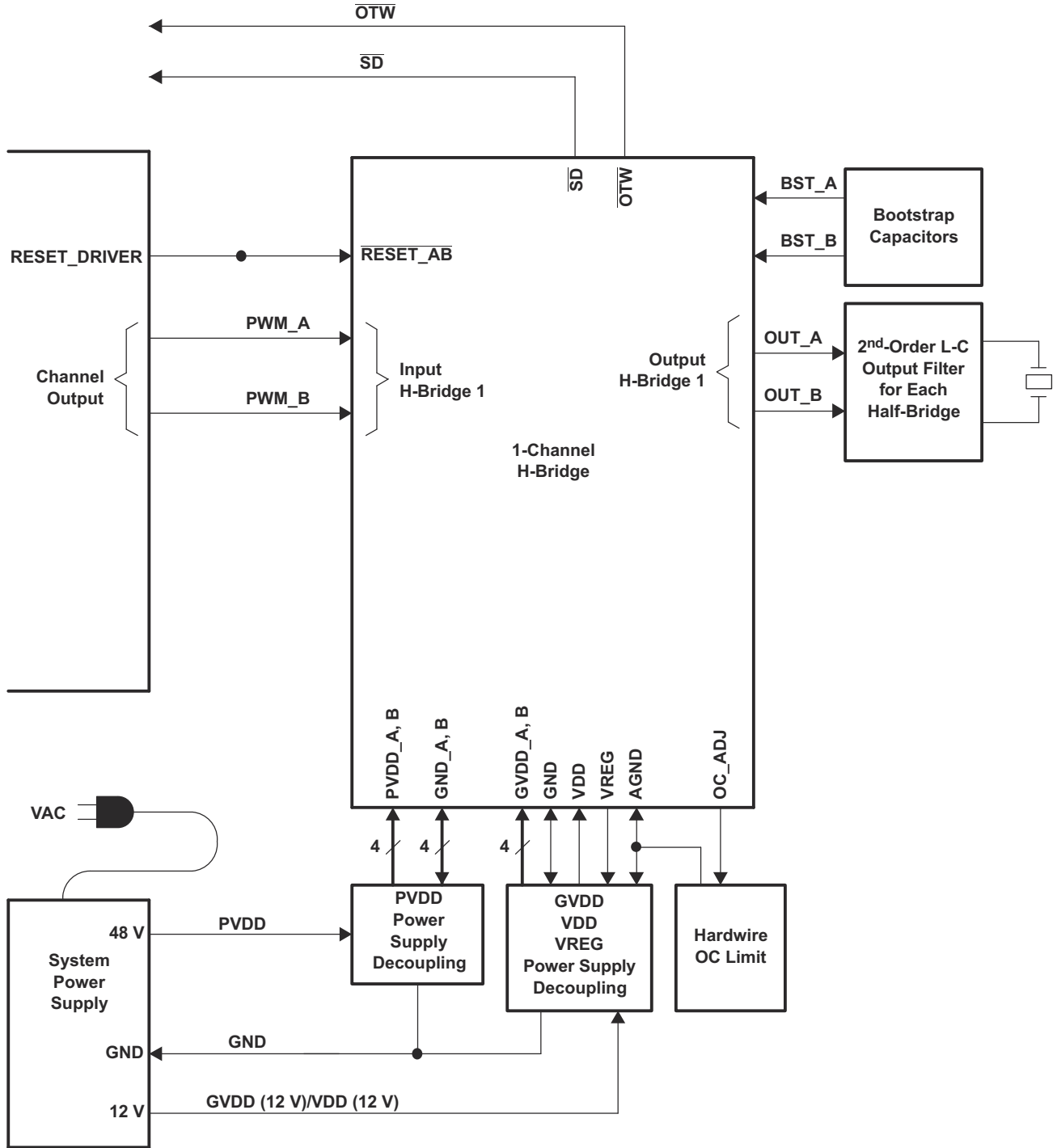


图 7-2. Functional Block Diagram

7.2 Feature Description

7.2.1 Error Reporting

The \overline{SD} and \overline{OTW} pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown, such as overtemperature shut down, overcurrent shut-down, or undervoltage protection, is signaled by the \overline{SD} pin going low. Likewise, \overline{OTW} goes low when the device junction temperature exceeds 125°C (see 表 7-1).

表 7-1. Protection Mode Signal Descriptions

| SD | OTW | DESCRIPTION |
|----|-----|--|
| 0 | 0 | Overtemperature warning and (overtemperature shut down or overcurrent shut down or undervoltage protection) occurred |
| 0 | 1 | Overcurrent shut-down or GVDD undervoltage protection occurred |
| 1 | 0 | Overtemperature warning |
| 1 | 1 | Device under normal operation |

TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system microcontroller and responding to an $\overline{\text{OTW}}$ signal by reducing the load current to prevent further heating of the device resulting in device overtemperature shutdown (OTSD).

To reduce external component count, an internal pullup resistor to internal VREG (3.3 V) is provided on both $\overline{\text{SD}}$ and $\overline{\text{OTW}}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

7.2.2 Device Reset

Reset pin is provided for control of the H-bridge. When $\overline{\text{RESET_AB}}$ is asserted low, the power-stage FETs in H-bridge are forced into a high-impedance (Hi-Z) state.

A rising-edge transition on reset input allows the device to resume operation after a shut-down fault and clears the fault and $\overline{\text{SD}}$ pin.

7.2.3 Device Protection System

7.2.3.1 Overcurrent (OC) Protection With Current Limiting and Overload Detection

The device has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. See the following table for OC-adjust resistor values. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, i.e., it performs a current-limiting function rather than prematurely shutting down during combinations of high-level transients and extreme load impedance drops. If the high-current situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. Current limiting and overload protection are independent for half-bridges A and B

- For the lowest-cost bill of materials in terms of component selection, the OC threshold measure should be limited, considering the power output requirement and minimum load impedance. Higher-impedance loads require a lower OC threshold.
- The demodulation-filter inductor must retain at least 5 μH of inductance at twice the OC threshold setting.

Unfortunately, most inductors have decreasing inductance with increasing temperature and increasing current (saturation). To some degree, an increase in temperature naturally occurs when operating at high output currents, due to core losses and the dc resistance of the inductor's copper winding. A thorough analysis of inductor saturation and thermal properties is strongly recommended.

Setting the OC threshold too low might cause issues such as lack of enough output power and/or unexpected shutdowns due to too-sensitive overload detection.

For added flexibility, the OC threshold is programmable within a limited range using a single external resistor connected between the OC_ADJ pin and AGND. (See the *Electrical Characteristics* section of this data sheet for information on the correlation between programming-resistor value and the OC threshold.) It should be noted that a properly functioning overcurrent detector assumes the presence of a properly designed demodulation filter at the power-stage output. Short-circuit protection is not provided directly at the output pins of the power stage but only on the transducer terminals (after the demodulation filter). It is required to follow certain guidelines when selecting the OC threshold and an appropriate demodulation inductor:

| OC-Adjust Resistor Values (k Ω) | Max. Current Before OC Occurs (A) |
|---|-----------------------------------|
| 22 | 12.2 |

| OC-Adjust Resistor Values (k Ω) | Max. Current Before OC Occurs (A) |
|---|-----------------------------------|
| 27 | 10.5 |
| 47 | 6.4 |
| 68 | 4.0 |
| 100 | 3.0 |

7.2.3.2 Overtemperature Protection

The DRV2901 has a two-level temperature-protection system that asserts an active-low warning signal (\overline{OTW}) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 155°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and \overline{SD} being asserted low. OTE is latched in this case and $\overline{RESET_AB}$ must be asserted low.

7.2.3.3 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the DRV2901 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.8 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and \overline{SD} being asserted low. The device automatically resumes operation when all supply voltage on the bootstrap capacitors have increased above the UVP threshold.

8 Applications and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV2901 is a high performance lens cleaner transducer driver. This device requires two power supplies, at 12 V for GVDD and VDD, and 12 V to 48 V for PVDD. The DRV2901 does not require power-up sequencing due to internal power-on reset.

8.2 Typical Application

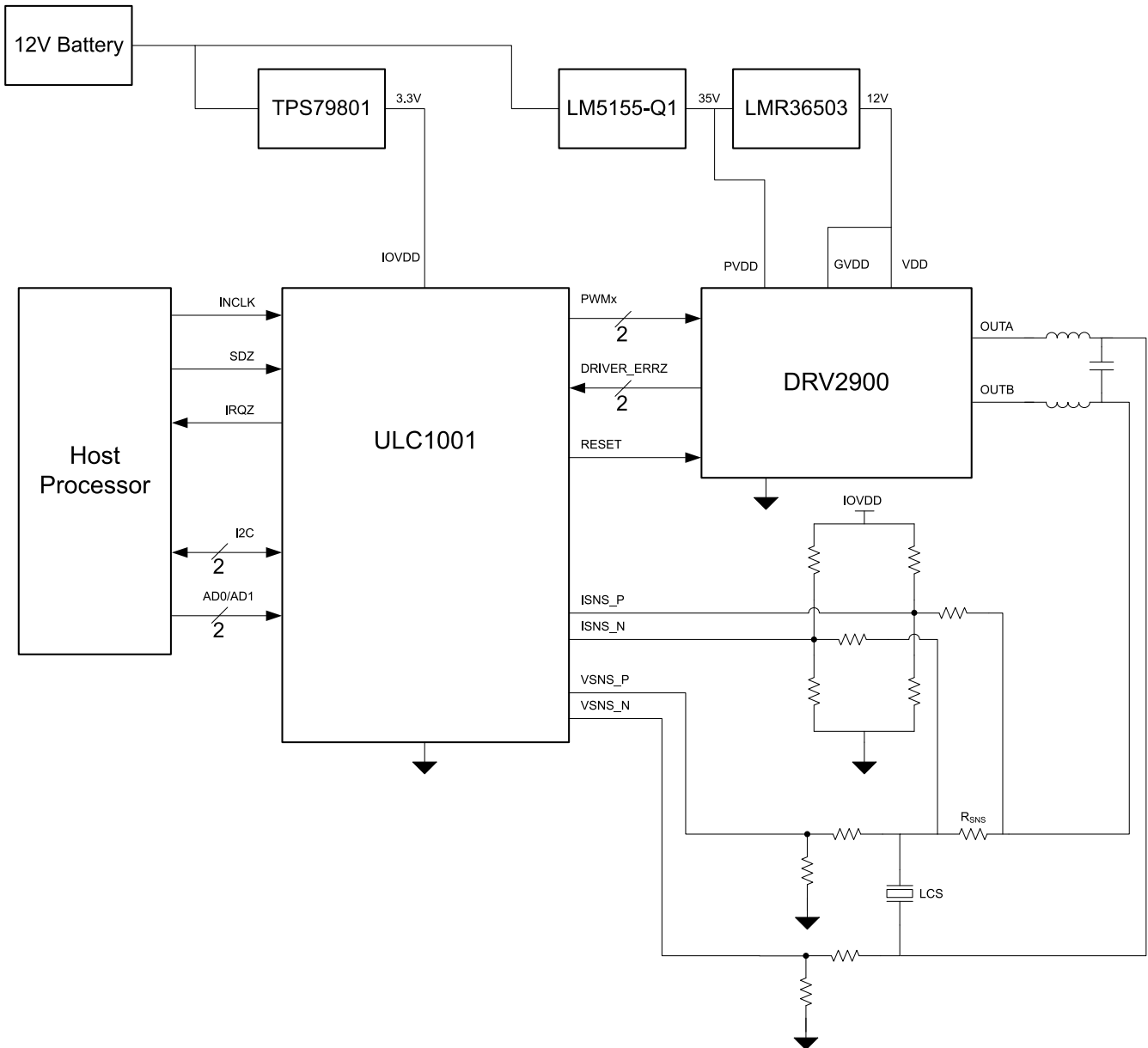


图 8-1. Typical System Diagram

9 Power Supply Recommendations

9.1 System Power-up/power-down Sequence

9.1.1 Powering Up

The DRV2901 does not require a power-up sequence. The outputs of the H-bridges remain in a high impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET_AB}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

9.1.2 Powering Down

The DRV2901 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET_AB}}$ low during power down, thus preventing any artifacts.

9.2 System Design Recommendations

9.2.1 VDD Pin

The transient current in VDD pin could be significantly higher than average current through VDD pin. A low resistive path to GVDD should be used. A 22- μF to 47- μF capacitor should be placed on VDD pin beside the 100-nF to 1- μF decoupling capacitor to provide a constant voltage during transient.

9.2.2 VREG Pin

The VREG pin is used for internal logic and should not be used as a voltage source for external circuitry. The capacitor on VREG pin should be connected to AGND.

9.2.3 OTW Pin

$\overline{\text{OTW}}$ reporting indicates the device approaching high junction temperature. This signal can be used with MCU to decrease system power when $\overline{\text{OTW}}$ is low in order to prevent OT shut down at a higher temperature.

No external pull up resistor or 3.3 V power supply is needed for 3.3 V logic. The $\overline{\text{OTW}}$ pin has an internal pullup resistor connecting to an internal 3.3 V to reduce external component count. For 5 V logic, an external pull up resistor to 5 V is needed.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| DRV2901DDVR | ACTIVE | HTSSOP | DDV | 44 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV2901 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

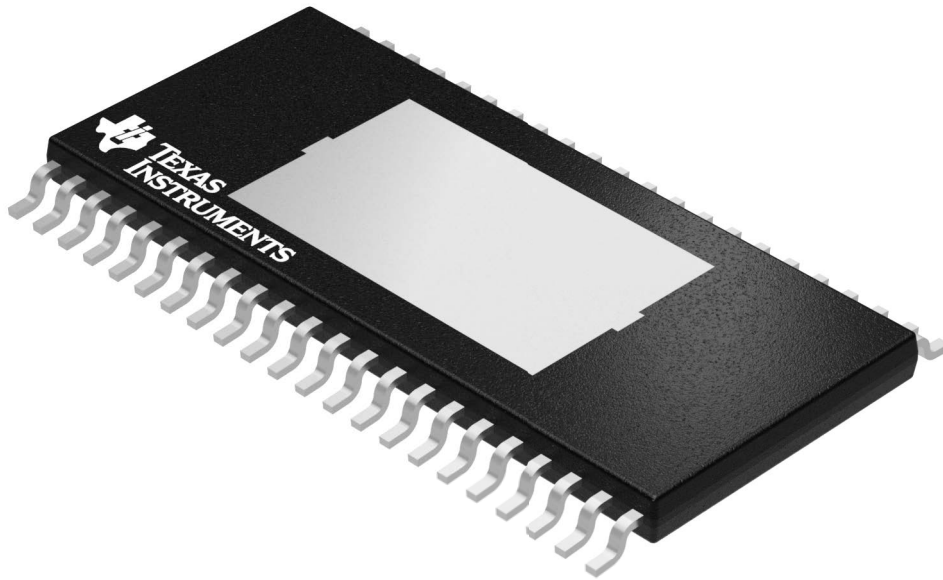

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV2901DDVR | HTSSOP | DDV | 44 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

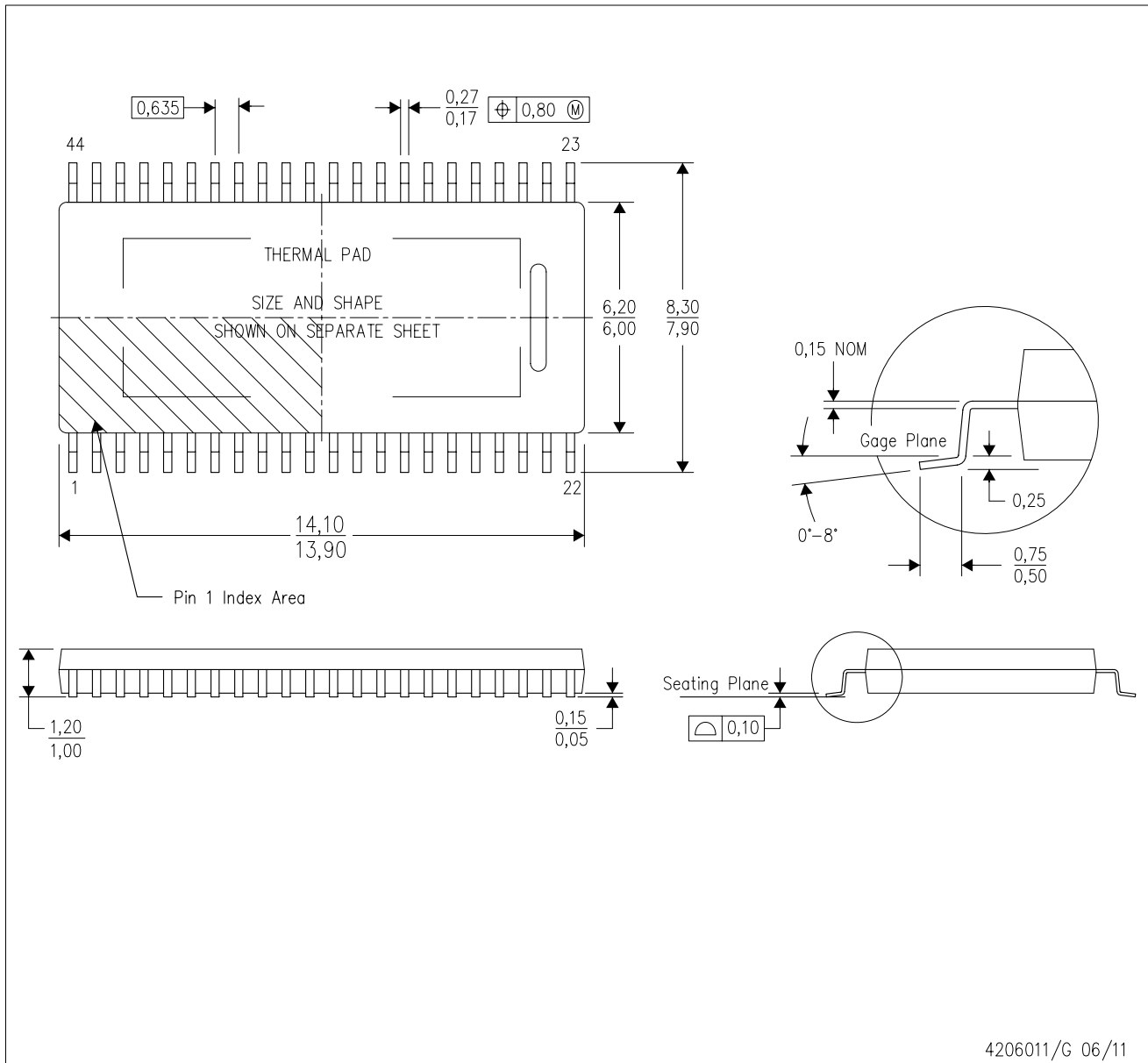
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DRV2901DDVR | HTSSOP | DDV | 44 | 2000 | 350.0 | 350.0 | 43.0 |



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

MECHANICAL DATA

DDV (R-PDSO-G44) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



4206011/G 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

DDV (R-PDSO-G44)

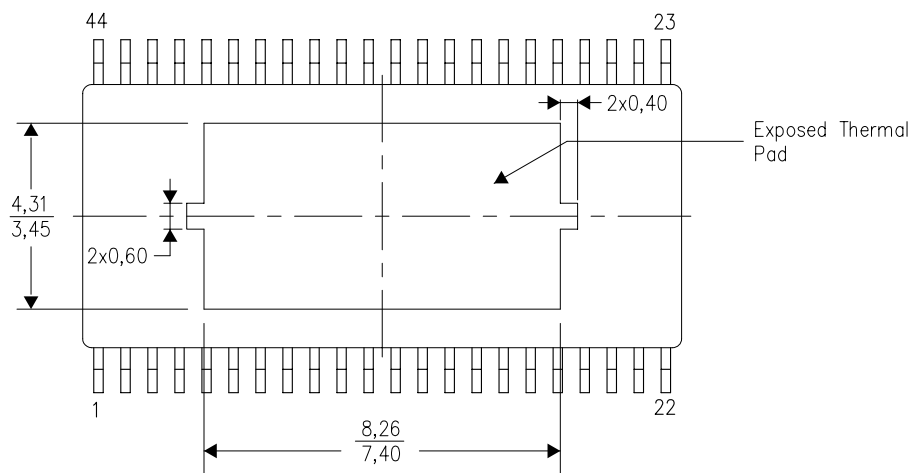
PowerPAD™ SMALL OUTLINE PACKAGE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206975-4/D 07/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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