ESD1LIN24-Q1、ESD751-Q1 和 ESD761-Q1 用于车载网络的汽车类 24V 单通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级 ESD 保护：
  - ±30kV、±22kV 或 ±15kV 接触放电
  - ±30kV、±22kV 或 ±15kV 气隙放电
- ISO 10605（330pF，330Ω）ESD 保护：
  - ±30kV、±22kV 或 ±15kV 接触放电
  - ±30kV、±22kV 或 ±15kV 气隙放电
- 24V 工作电压
- 双向 ESD 保护
- 低钳位电压可保护下游元件
- 符合 AEC-Q101 标准
- 温度范围：–55°C 至 +150°C
- I/O 电容 = 2.3pF、1.6pF 或 1.1pF（典型值）
- 采用业界通用封装：SOD-323 (DYF)、SOD-523 (DYA) 和 0402 尺寸无引线封装 (DPY)
- 引线式封装，用于自动光学检测 (AOI)

2 应用

- 汽车车载网络：
  - 本地互连网络 (LIN)
  - 单线 CAN ESD 保护
- 工业控制网络：
  - DeviceNet
  - 智能配电系统

3 说明

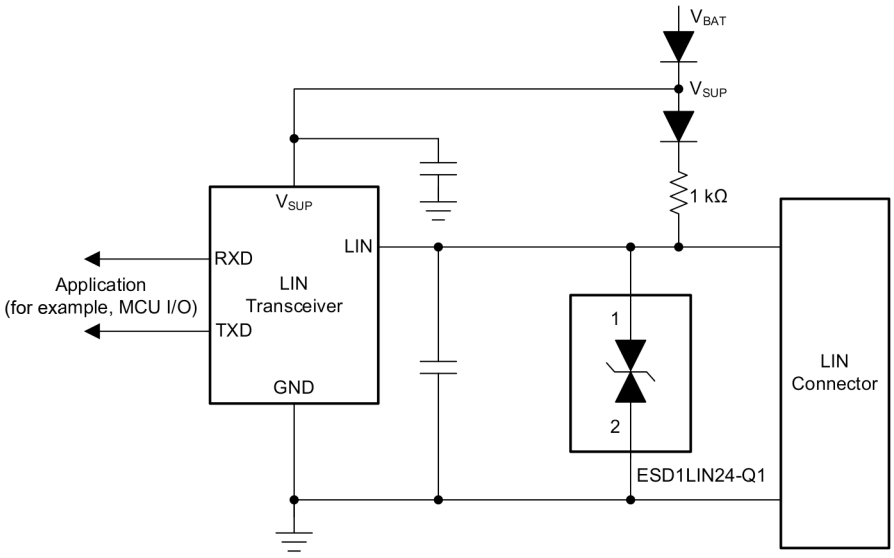
ESD1LIN24-Q1、ESD751-Q1 和 ESD761-Q1 是适用于本地互连网络 (LIN) 的单通道低电容双向 ESD 保护器件。这些器件旨在耗散超过 IEC 61000-4-2 国际标准所规定最高水平（分别为 ±30kV 接触放电、±30kV 气隙放电，±22kV 接触放电、±22kV 气隙放电以及 ±15kV 接触放电、±15kV 气隙放电）的接触 ESD 冲击。低动态电阻和低钳位电压有助于保护系统免受瞬态事件的影响。这种保护很关键，因为汽车系统在控制安全设备时需要高度的稳健性和可靠性。

ESD1LIN24-Q1 和 ESD751-Q1 均采用引线式封装，可轻松实现直通式布线。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
ESD1LIN24-Q1	DYF（SOD-323，2）	2.50mm × 1.20mm
ESD751-Q1	DYA（SOD-523，2）	1.60mm × 0.80mm
ESD761-Q1	DPY（X1SON，2）	1.00mm × 0.60mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



典型应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (November 2022) to Revision C (December 2022)	Page
• 将 ESD1LIN24-Q1 和 ESD761-Q1 器件的状态从*预告信息*更改为*“量产数据”*	1

Changes from Revision A (September 2022) to Revision B (November 2022)	Page
• 将 ESD751-Q1 器件的状态从*预告信息*更改为*量产数据*	1

5 Pin Configuration and Functions

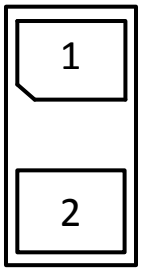


图 5-1. DPY Package, 2-Pin X1SON (Top View)

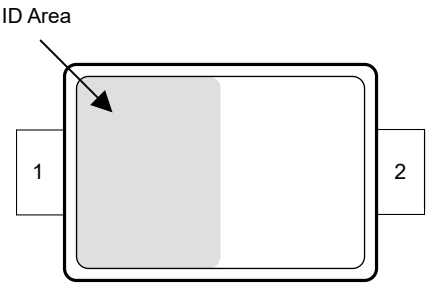


图 5-2. DYF Package, 2-Pin SOD-323 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected IO
GND	2	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		DEVICE	MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 Power (t_p - 8/20 µs) at 25°C	ESD1LIN24-Q1		159	W
		ESD751-Q1		102	
		ESD761-Q1		65	
I_{PP}	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C	ESD1LIN24-Q1		4.3	A
		ESD751-Q1		2.8	
		ESD761-Q1		1.8	
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	
T_{stg}	Storage temperature		-65	155	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001(1)	± 2500	V
		Charged device model (CDM), per AEC Q101-005	± 1000	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

			DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD1LIN24-Q1	±30000	V
			ESD751-Q1	±22000	
			ESD761-Q1	±15000	
		IEC 61000-4-2 Air-gap Discharge, all pins	ESD1LIN24-Q1	±30000	
			ESD751-Q1	±22000	
			ESD761-Q1	±15000	

6.4 ESD Ratings - ISO Specification

				DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge	ISO 10605, 150-pF, 330-Ω, IO	ESD1LIN24-Q1	± 30000	V
				ESD751-Q1	± 22000	
				ESD761-Q1	± 15000	
			ISO 10605, 330-pF, 330-Ω, IO	ESD1LIN24-Q1	± 30000	
				ESD751-Q1	± 22000	
				ESD761-Q1	± 15000	
		Air-gap discharge	ISO 10605, 150-pF, 330-Ω, IO	ESD1LIN24-Q1	± 30000	
				ESD751-Q1	± 22000	
				ESD761-Q1	± 15000	
			ISO 10605, 330-pF, 330-Ω, IO	ESD1LIN24-Q1	± 30000	
				ESD751-Q1	± 22000	
				ESD761-Q1	± 15000	

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

6.6 Thermal Information

THERMAL METRIC(1)		ESD1LIN24-Q1	ESD751-Q1	ESD761-Q1	UNIT
		DYF (SOD-323)	DYA (SOD-523)	DPY (X1SON)	
		2 PINS	2 PINS	2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	705.4	746.3	282.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	315	301.2	150.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	561.5	509.6	98.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	145	81.8	9.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	550.2	503.0	97.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			-24		24	V
V_{BRF}	Breakdown voltage(1)	I_{IO} = 10 mA, IO to GND		25.5		35.5	V
V_{BRR}	Breakdown voltage(1)	I_{IO} = -10 mA, IO to GND		-35.5		-25.5	V
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 4.3 A, t_p = 8/20 µs, IO to GND and GND to IO	ESD1LIN24-Q1		37		V
		I_{PP} = 2.8 A, t_p = 8/20 µs, IO to GND and GND to IO	ESD751-Q1		36.5		
		I_{PP} = 1.8 A, t_p = 8/20 µs, IO to GND and GND to IO	ESD761-Q1		36.3		

6.7 Electrical Characteristics (continued)

over T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{CLAMP}	Clamping voltage(3)	I_{PP} = 16 A, TLP, IO to GND and GND to IO	ESD1LIN24-Q1		40		V
			ESD751-Q1		41.5		
			ESD761-Q1		42.5		V
I_{LEAK}	Leakage current	V_{IO} = ±24 V, IO to GND		-50	1	50	nA
R_{DYN}	Dynamic resistance(3)		ESD1LIN24-Q1		0.5		Ω
			ESD751-Q1		0.6		
			ESD761-Q1		0.53		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, V_{pp} = 30 mV, IO to GND	ESD1LIN24-Q1		2.3	3.8	pF
			ESD751-Q1		1.6	2.7	
			ESD761-Q1		1.1	1.8	

(1) V_{BRF} and V_{BRR} are defined as the voltage when ±10 mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

6.8 Typical Characteristics – ESD751

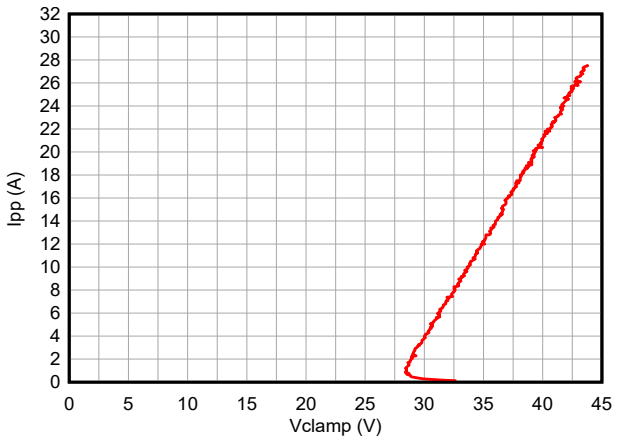


图 6-1. Positive TLP Curve

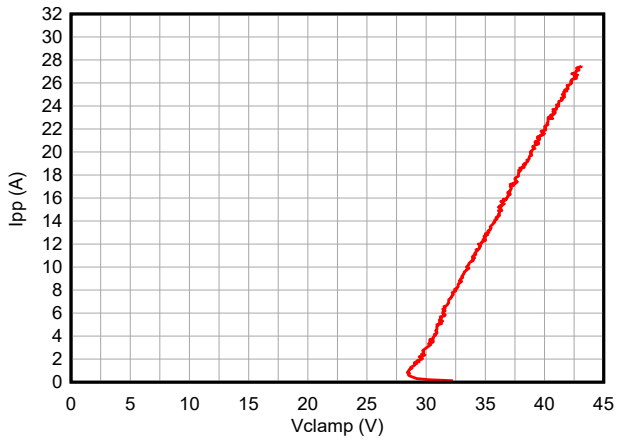


图 6-2. Negative TLP Curve

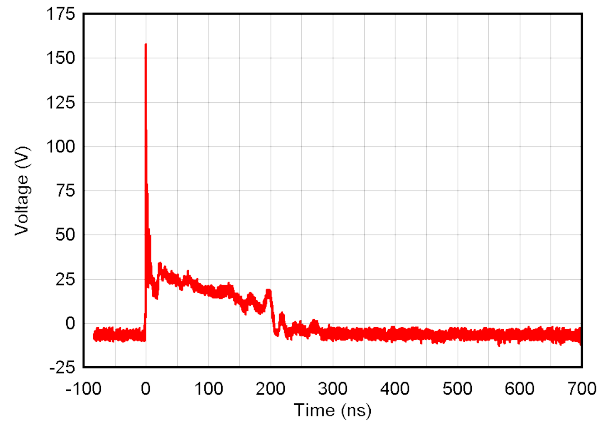


图 6-3. +8-kV Clamped IEC Waveform

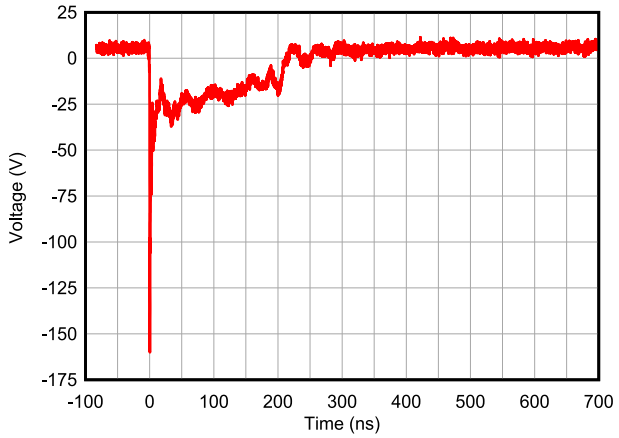


图 6-4. -8-kV Clamped IEC Waveform

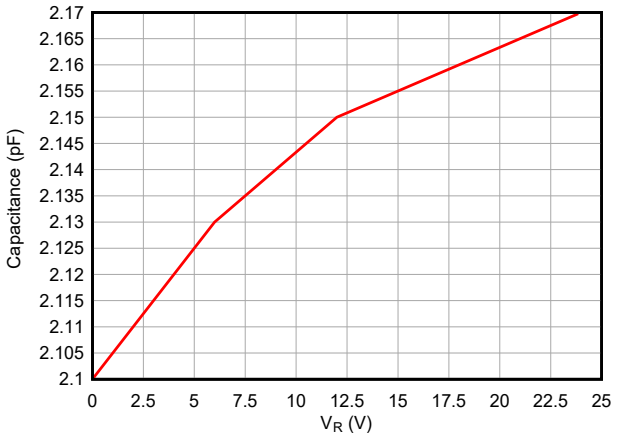


图 6-5. Capacitance vs. Bias Voltage

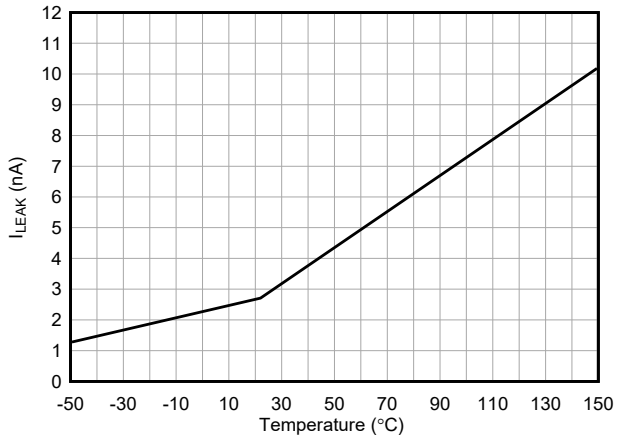


图 6-6. Leakage Current vs. Temperature

6.9 Typical Characteristics – ESD1LIN24

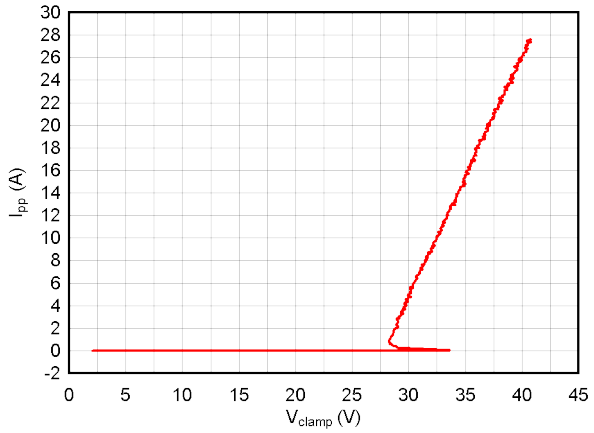


图 6-7. Positive TLP Curve

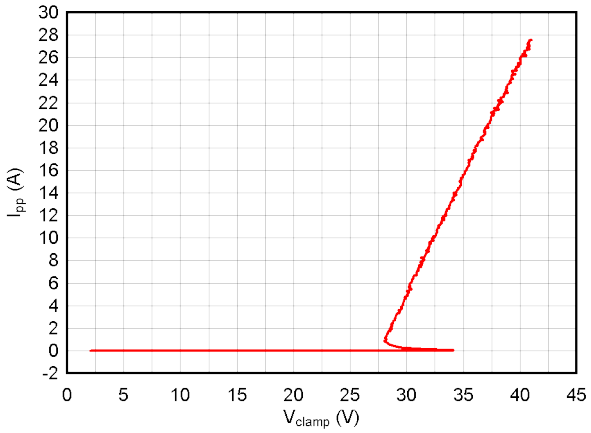


图 6-8. Negative TLP Curve

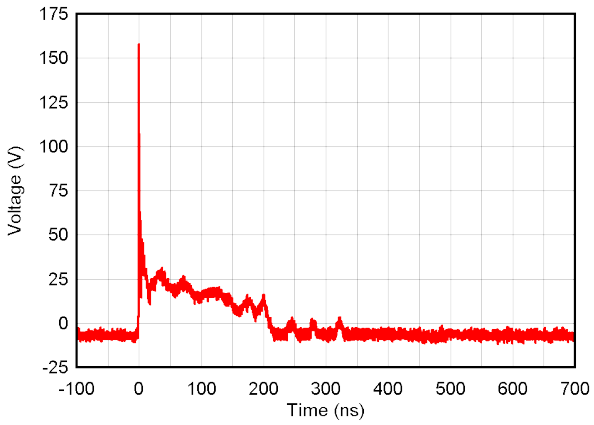


图 6-9. +8-kV Clamped IEC Waveform

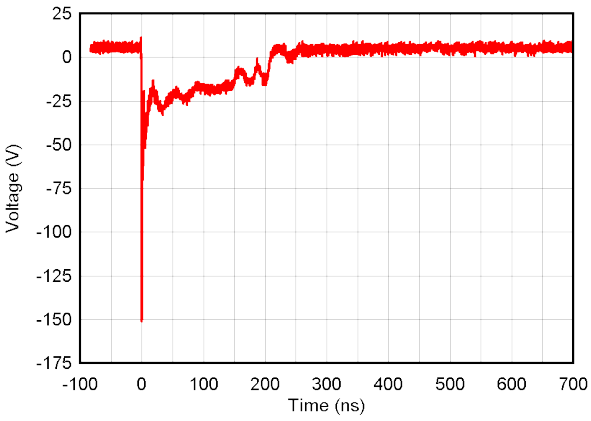


图 6-10. –8-kV Clamped IEC Waveform

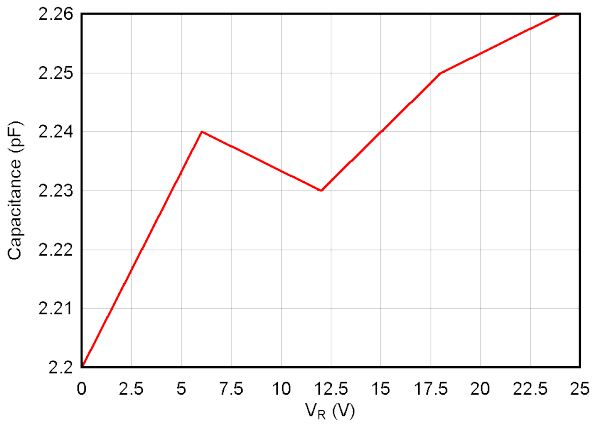


图 6-11. Capacitance vs. Bias Voltage

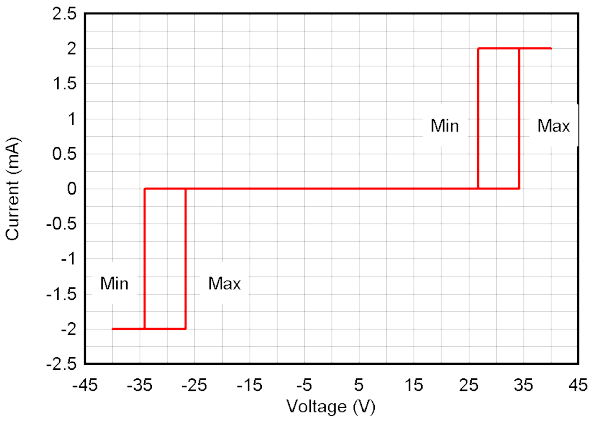


图 6-12. DC Voltage Sweep I-V Curve

6.10 Typical Characteristics - ESD761

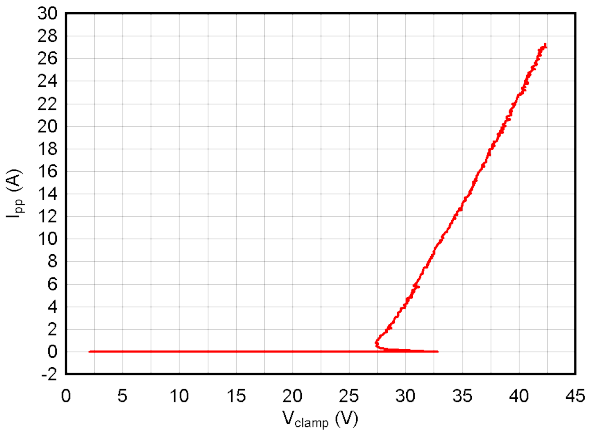


图 6-13. Positive TLP Curve

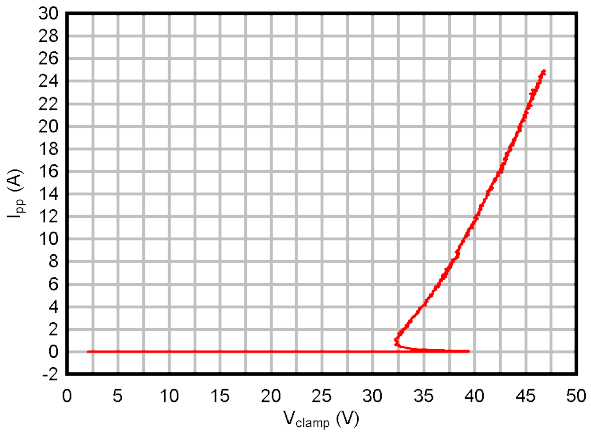


图 6-14. Negative TLP Curve

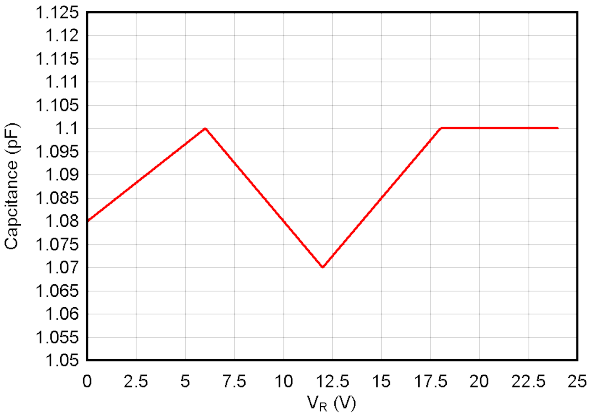


图 6-15. Capacitance vs. Bias Voltage

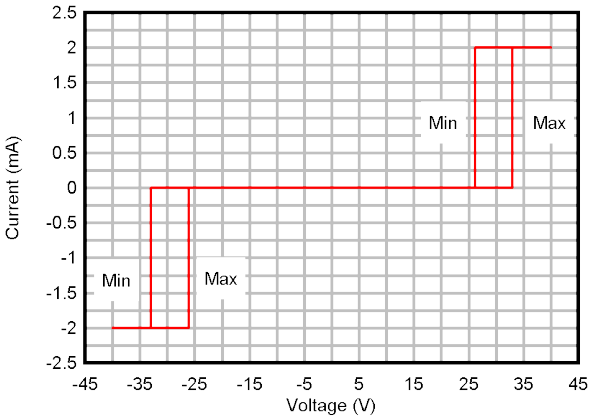


图 6-16. DC Voltage Sweep I-V Curve

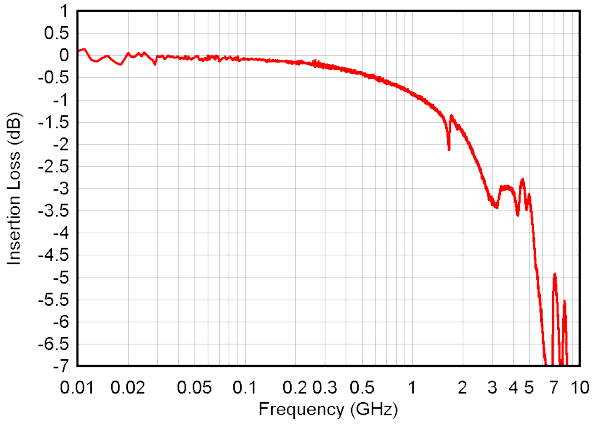


图 6-17. Insertion Loss

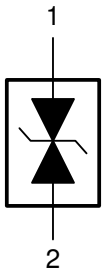
7 Detailed Description

7.1 Overview

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single-channel ESD diodes available in industry standard packages (SOD-323 and SOD-523) which are convenient for automatic optical inspection as well as a smaller leadless package X1SON (DPY). These products offer ISO 10605 ESD ratings of (±30- kV Contact, ±30-kV Airgap), (±22-kV Contact, ±22- kV Airgap), and (±15-kV Contact, ±15-kV Airgap), respectively. The 2.3 pF, 1.6 pF, and 1.1 pF line capacitance of these ESD protection diodes are suitable for LIN applications that support data rates from 20 Kbps to 10 Mbps.

Typical application of these products is the ESD circuit protection for LIN transceivers used in automotive applications. These devices are commonly used for ESD protection inside automotive electronic control units (ECUs) for head lights, door modules, climate control, roof control, wipers, cluster, audio, and many other automotive applications.

7.2 Functional Block Diagram



7.3 Feature Description

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single-channel bidirectional ESD diodes with a high ESD protection level. These devices have a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. The breakdown is bidirectional so these protection devices can prevent system damage if battery leads are swapped. Low leakage allows the diodes to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes these ESD devices work at extensive temperatures in most environments.

7.3.1 IEC 61000-4-5 Surge Protection

The I/O pins of the ESD1LIN24-Q1, ESD751-Q1, ESD761-Q1 have the following surge ratings (8/20 µs waveform): 4.3A, 2.8 A, and 1.8 A, respectively. An ESD-surge clamp diverts this current to ground.

7.3.2 IO Capacitance

The capacitance between the I/O pins of the ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 devices are as follows: 2.3 pF, 1.6 pF, and 1.1 pF, respectively. The capacitance of these devices support data rates for LIN up to 10 Mbps.

7.3.3 Dynamic Resistance

The I/O pins feature an ESD clamp that have a low R_{DYN} of 0.48 Ω for the ESD1LIN24-Q1, 0.6 Ω for the ESD751-Q1, and 0.58 Ω for the ESD761-Q1.

7.3.4 DC Breakdown Voltage

The DC breakdown voltage between the I/O pins is a minimum of ± 25.5 V. This shields sensitive equipment from surges above the reverse standoff voltage of ± 24 V.

7.3.5 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 50 nA (maximum) with a bias of ± 24 V.

7.3.6 Clamping Voltage

The I/O pins of the ESD1LIN24-Q1 feature an ESD clamp that is capable of clamping the voltage to 37 V (I_{PP} = 4.3 A) and 37.7 V (I_{PP} = 16 A for TLP). The I/O pins of the ESD751-Q1 feature an ESD clamp that is capable of clamping the voltage to 36.5 V (I_{PP} = 2.8 A) and 39.7 V (I_{PP} = 16 A for TLP). The I/O pins of the ESD761-Q1 feature an ESD clamp that is capable of clamping the voltage to 36.3 V (I_{PP} = 1.8 A) and 39.3 V (I_{PP} = 16 A for TLP).

7.3.7 Industry Standard Packages

The ESD1LIN24-Q1 and ESD751-Q1 feature industry standard SOD-323 (DYF) and SOD-523 (DYA) leaded packages for automatic optical inspection (AOI). The ESD761-Q1 is offered in the leadless X1SON (DPY) package

7.4 Device Functional Modes

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single channel passive clamps that have low leakage during normal operation when the voltage between I/O and GND is below V_{RWM}, and activate when the voltage between I/O and GND goes above V_{BR}. During ISO 10605 ESD events, transient voltages from ±30 kV to ±15 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 are single channel TVS diodes which are used to provide a path to ground for dissipating ESD events on LIN signal lines. The LIN signal lines are typically routed throughout the automobile to connect between the different ECUs. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

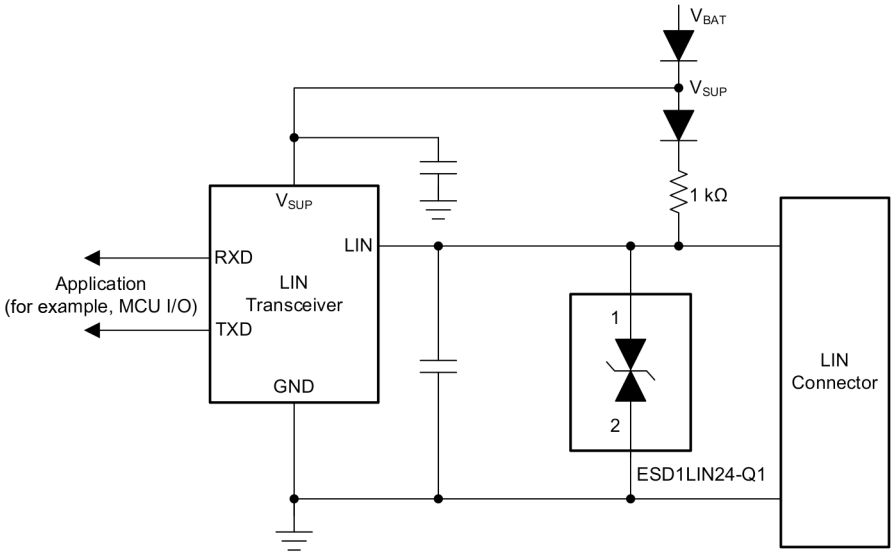


图 8-1. Typical Application

8.2.1 Design Requirements

For this design example, the ESD1LIN24-Q1 is used to provide ESD protection to a LIN transceiver. The parameters listed in 表 8-1 are the known design parameters for this application.

表 8-1. Design Parameters for Typical Applications

Design Parameter	Value
Diode configuration	Bidirectional
V_{IO} signal range	Up to 18 V
V_{RWM}	±24 V
Jumpstart short to battery event on V_{IO}	±24 V
Data rate	Up to 10 Mbps
Pullup resistor	1 kΩ

8.2.2 Detailed Design Procedure

The ESD1LIN24-Q1, ESD751-Q1, and ESD761-Q1 have a V_{RWM} of ±24 V to protect the diode from being damaged during a short to battery event that can occur by reversing the terminal connections during jumpstart. The bidirectional characteristic ensures both positive and negative polarity are protected. The low capacitance of 5 pF or less permits data rates up to 10 Mbps, which allows the designer to meet the requirements for LIN. The 1 kΩ and VSUP diode allows the LIN signal to be pulled up to a diode drop below the battery voltage.

8.2.3 Application Curves

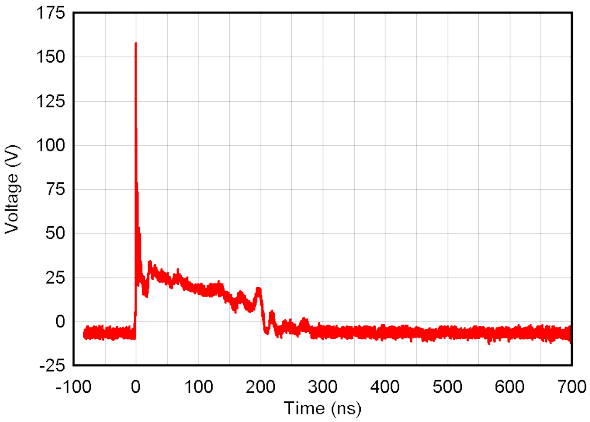


图 8-2. +8-kV Clamped IEC Waveform

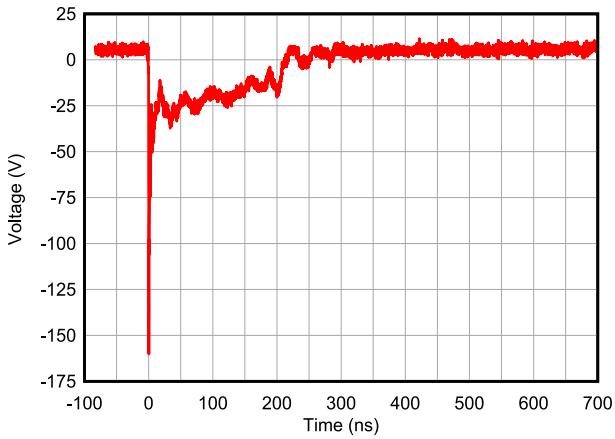


图 8-3. −8-kV Clamped IEC Waveform

9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, therefore there is no requirement to power it. Ensure that the maximum voltage specifications for each pin is not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or 2 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

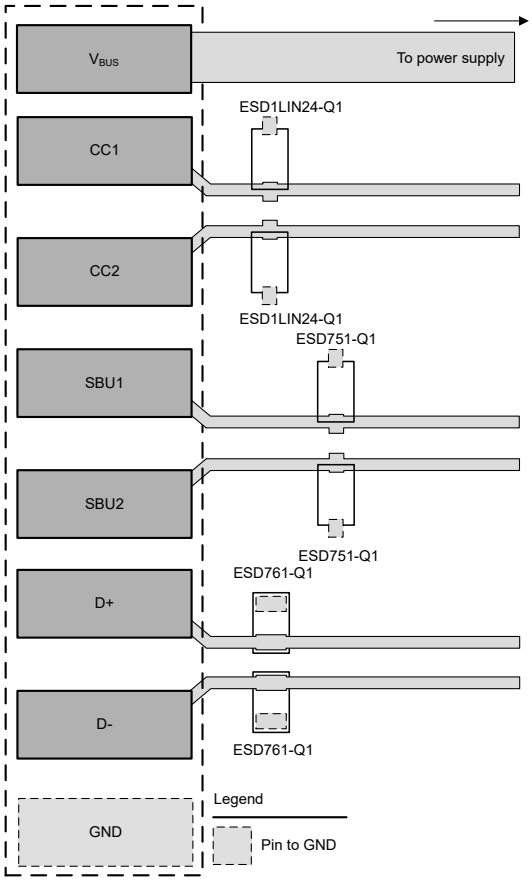


图 10-1. Layout Recommendation

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD1LIN24DYFRQ1	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	2QKF	Samples
ESD751DYARQ1	ACTIVE	SOT-5X3	DYA	2	8000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	1MO	Samples
ESD761DPYRQ1	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 150	NF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ESD1LIN24-Q1, ESD751-Q1, ESD761-Q1 :

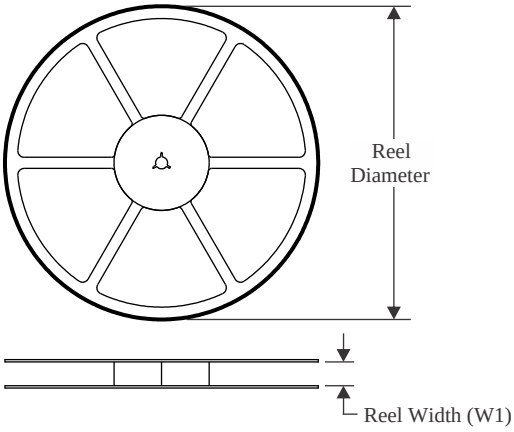
- Catalog : ESD1LIN24, ESD751, ESD761

NOTE: Qualified Version Definitions:

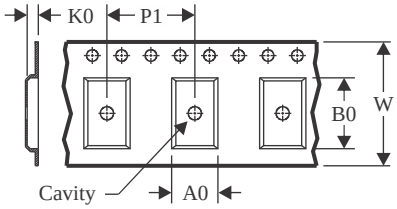
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

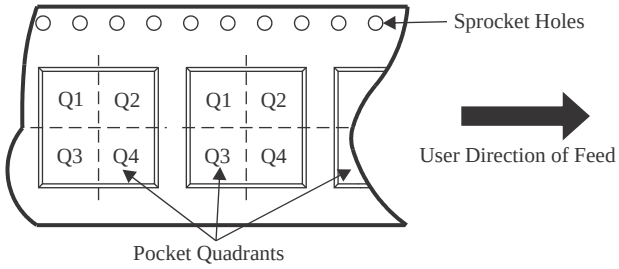


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

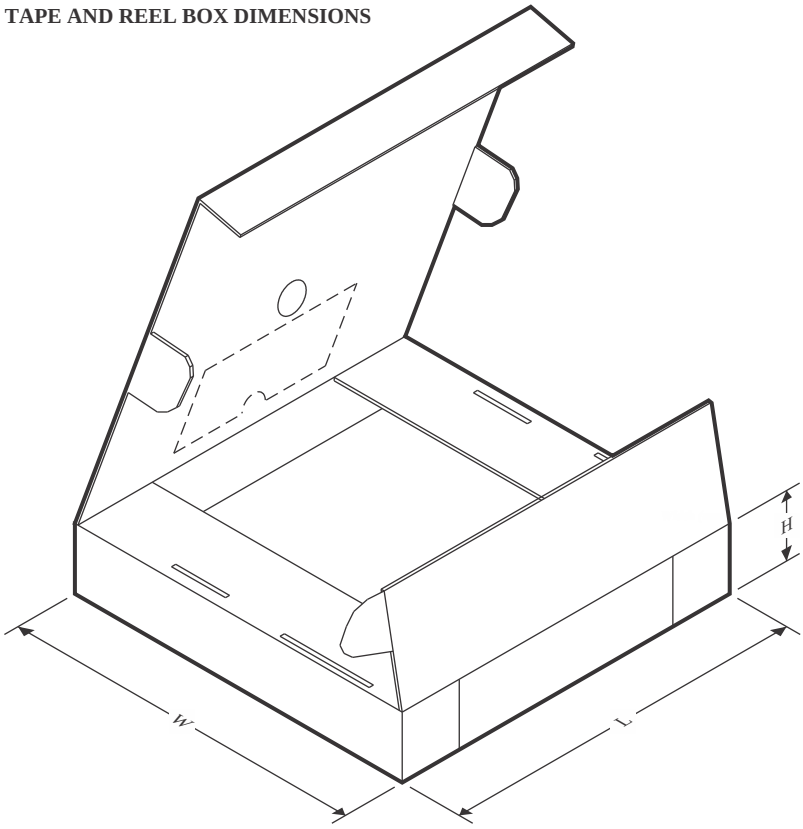
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD1LIN24DYFRQ1	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
ESD751DYARQ1	SOT-5X3	DYA	2	8000	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1
ESD761DPYRQ1	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

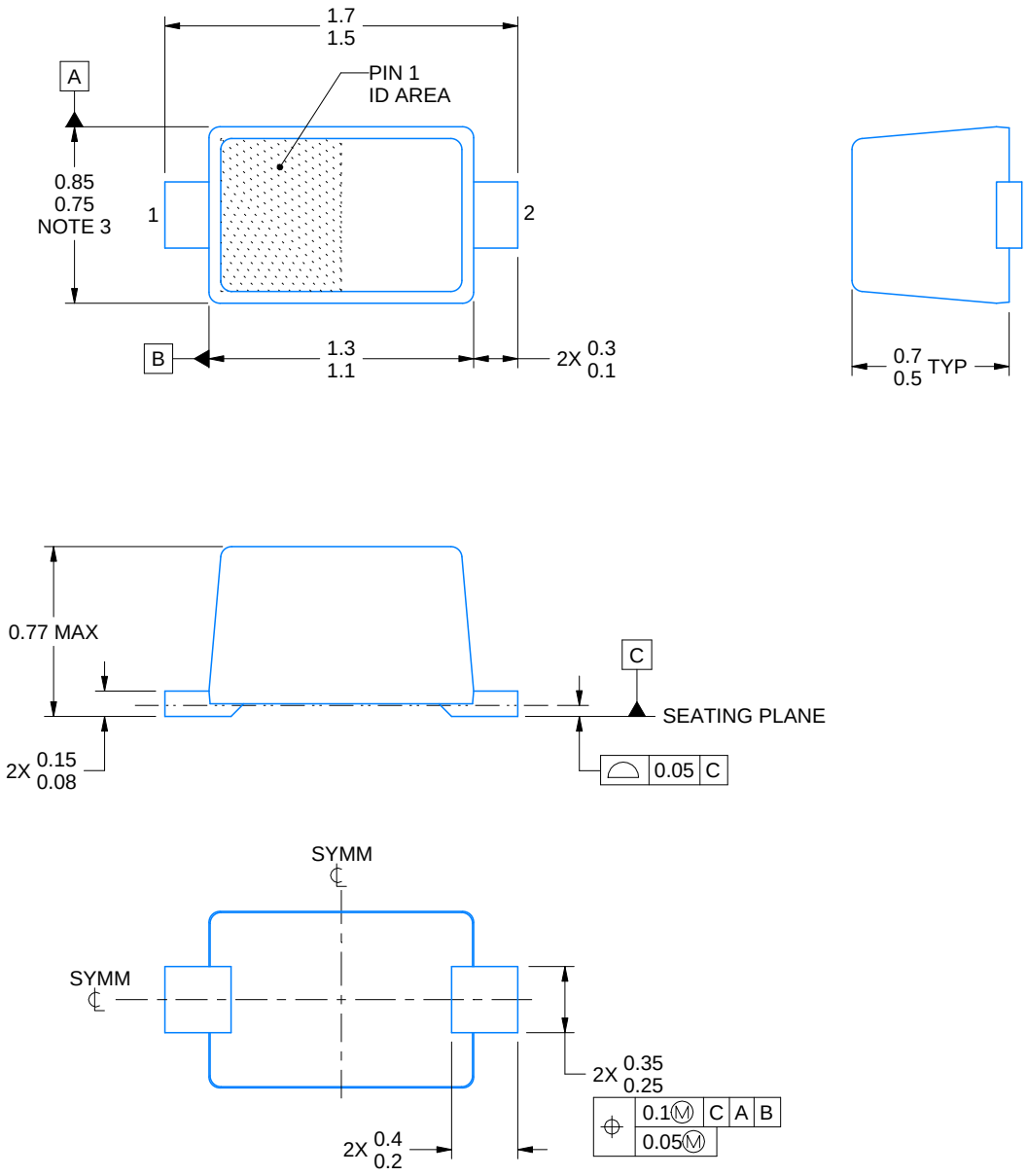
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD1LIN24DYFRQ1	SOT	DYF	2	3000	210.0	200.0	42.0
ESD751DYARQ1	SOT-5X3	DYA	2	8000	210.0	200.0	42.0
ESD761DPYRQ1	X1SON	DPY	2	10000	205.0	200.0	33.0

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

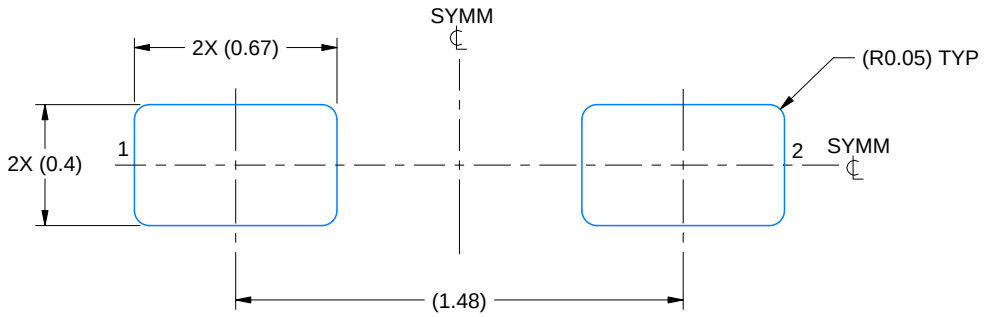
PLASTIC SMALL OUTLINE



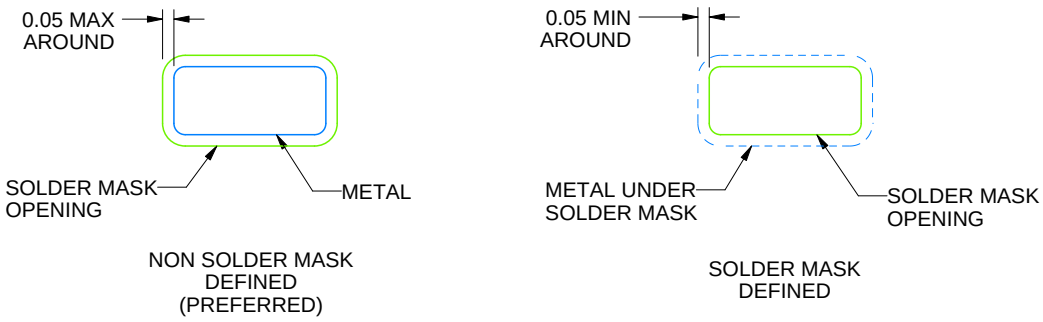
4224978/B 09/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

4224978/B 09/2021

NOTES: (continued)

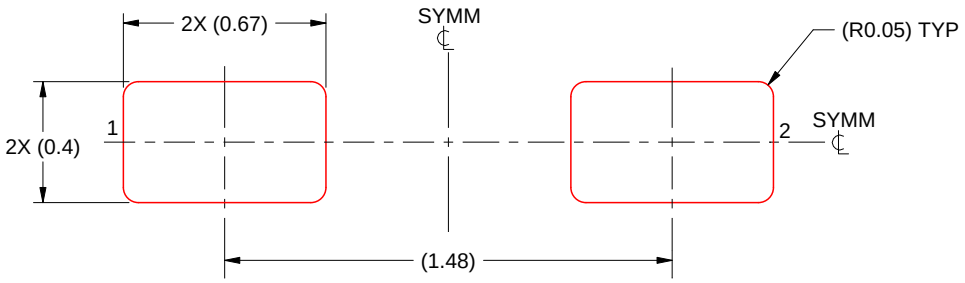
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



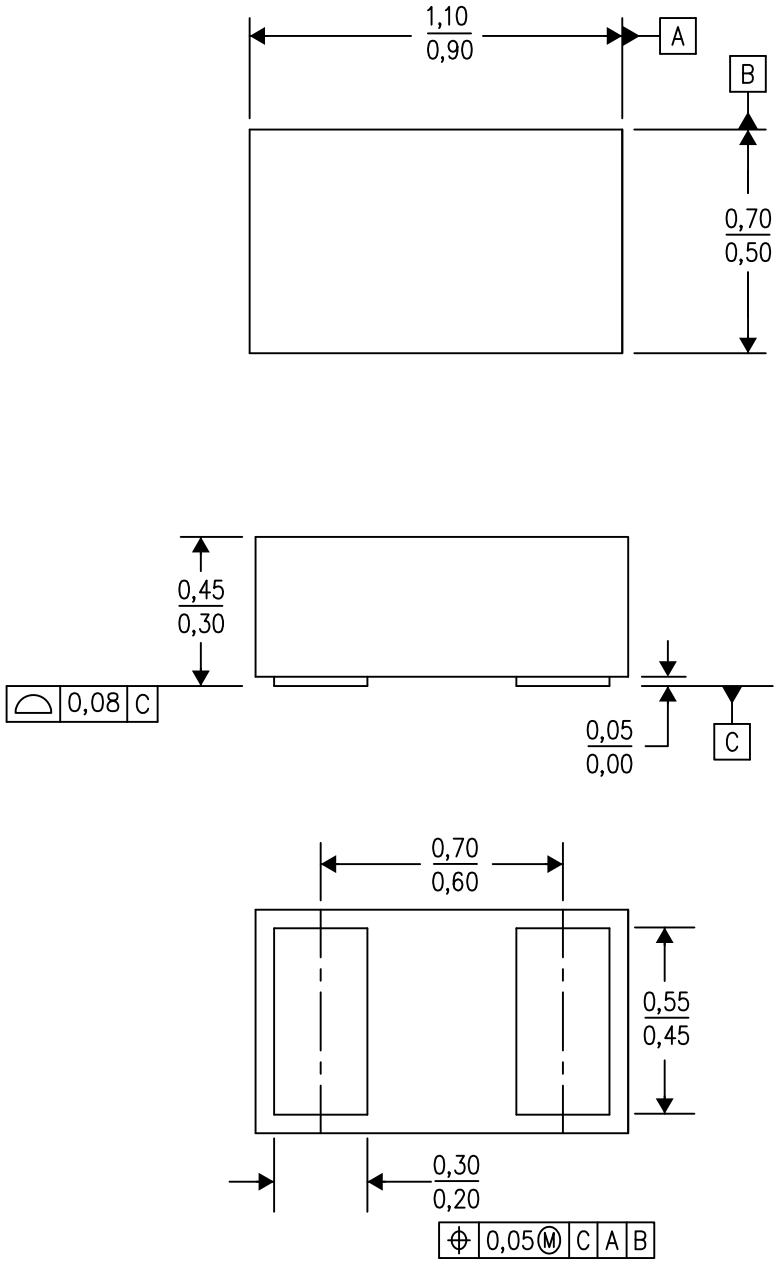
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/B 09/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



4211012/D 08/14

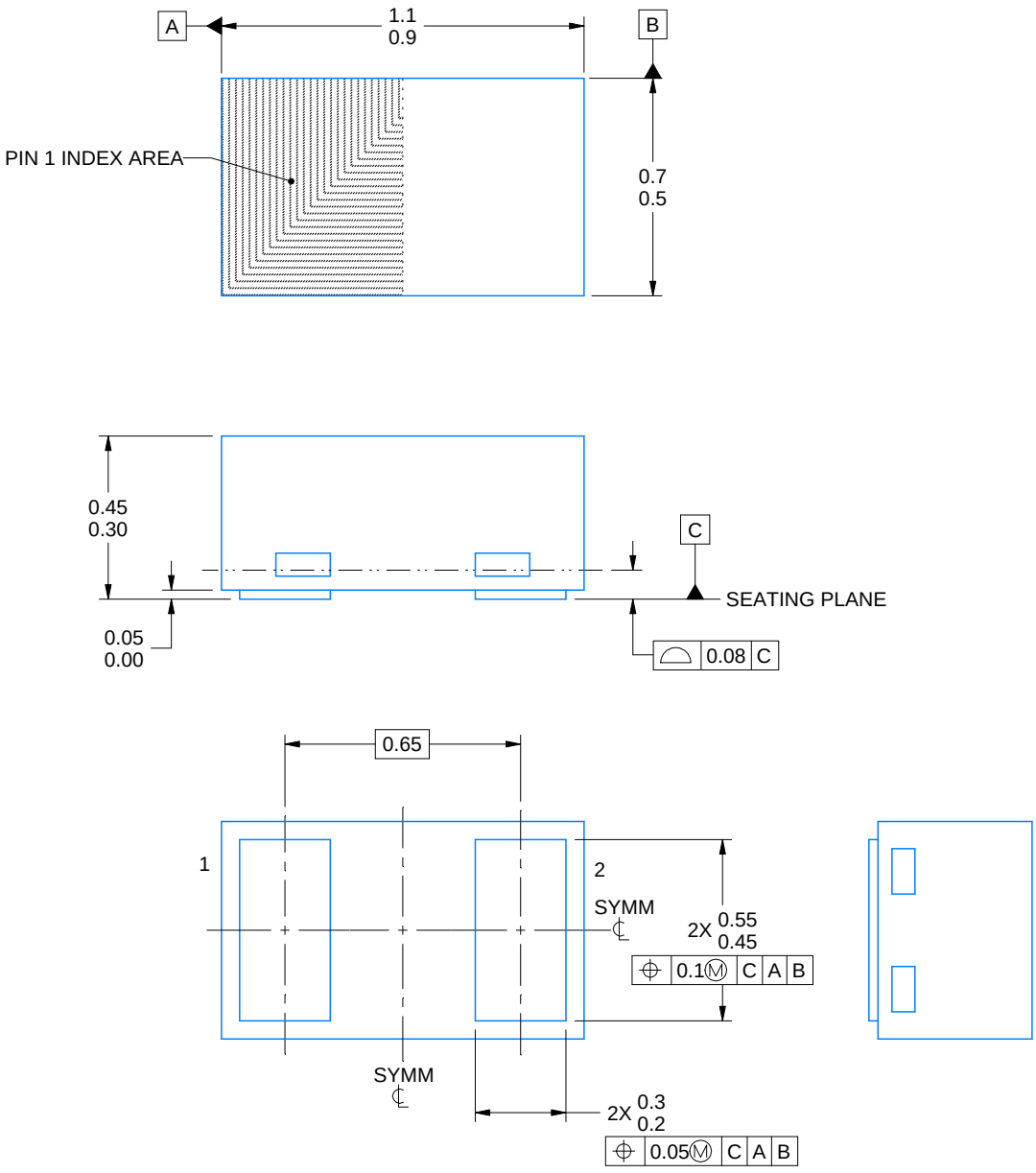
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

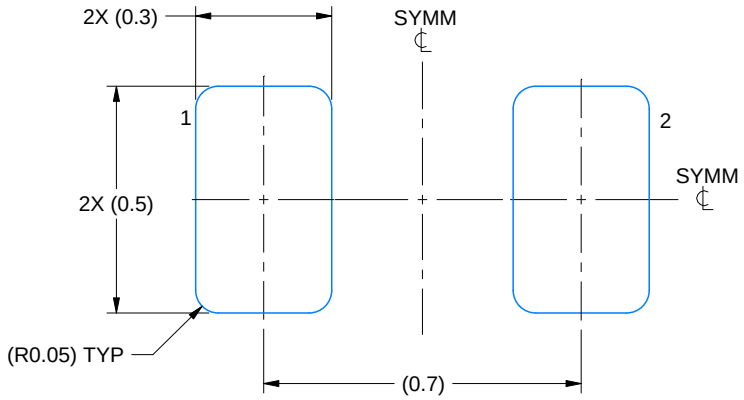
PLASTIC SMALL OUTLINE - NO LEAD



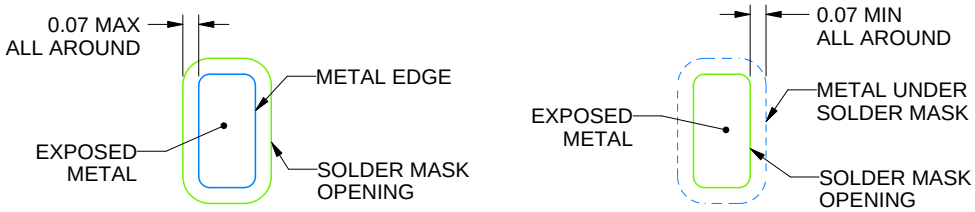
4224561/B 03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

4224561/B 03/2021

NOTES: (continued)

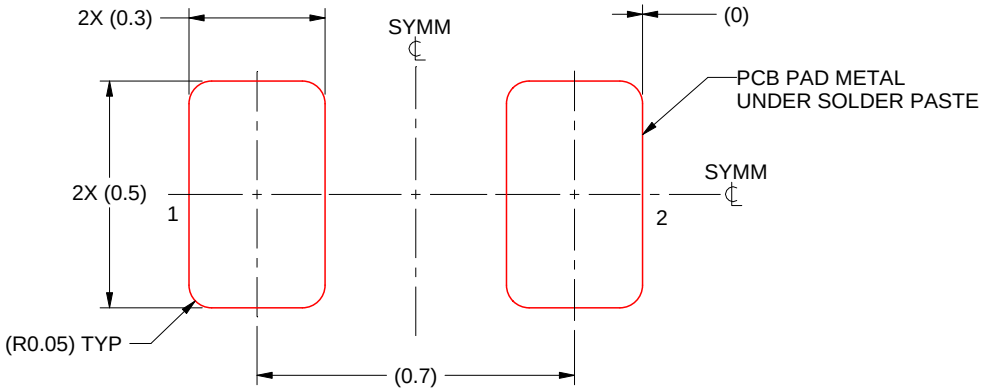
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/B 03/2021

NOTES: (continued)

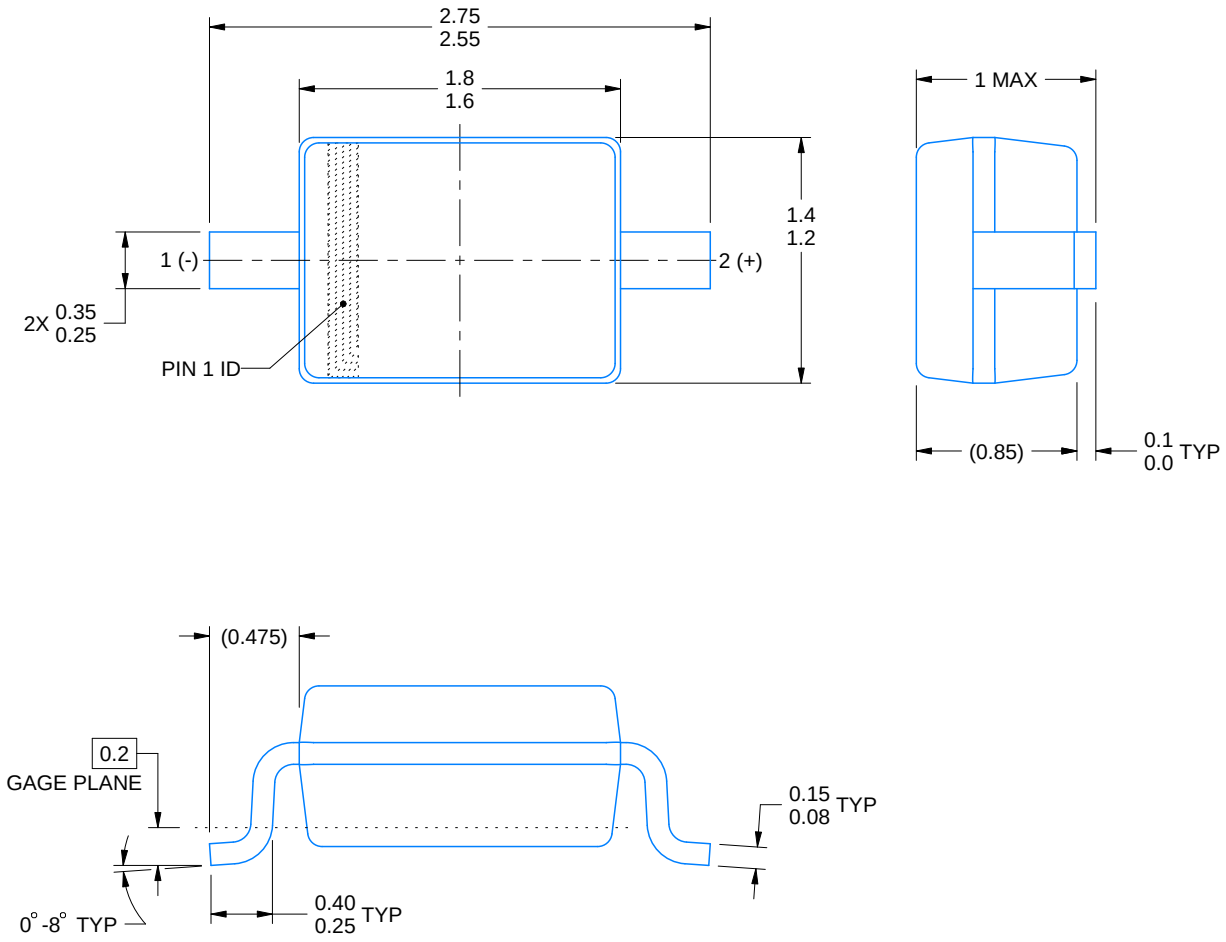
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYF0002A

SOT(SOD-323) - 1 mm max height

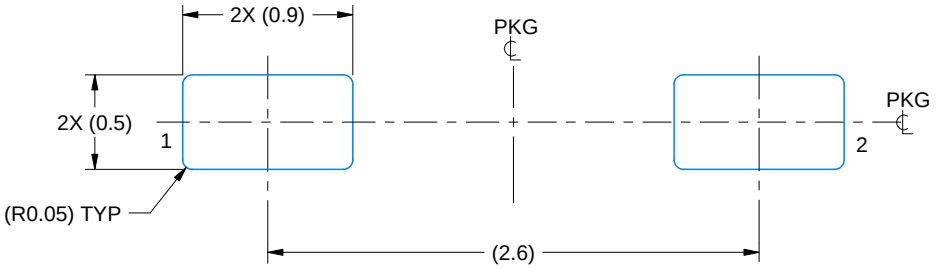
SMALL OUTLINE TRANSISTOR



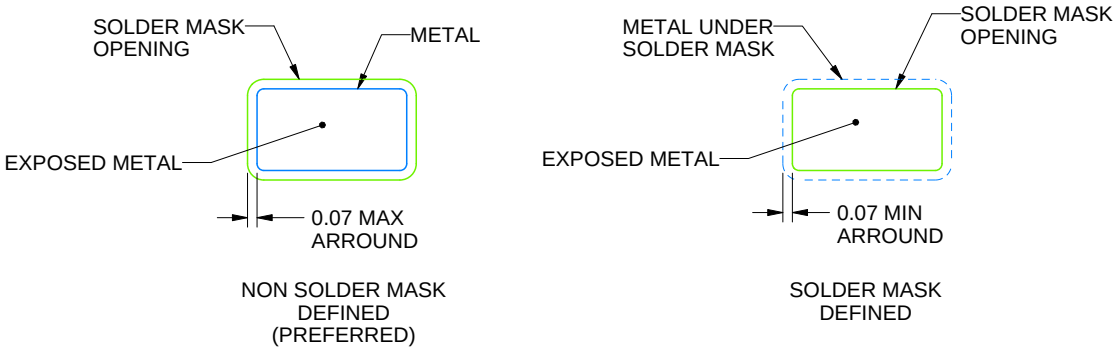
4228484/A 02/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4228484/A 02/2022

NOTES: (continued)

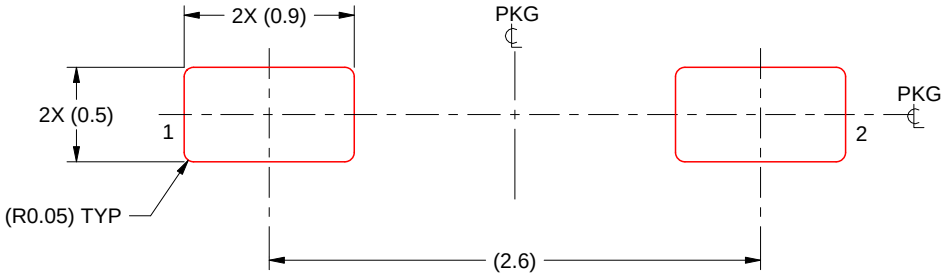
3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4228484/A 02/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265