

JFE2140 超低噪声、匹配低栅电流双离散音频 N 通道 JFET



Texas Instruments
Burr-Brown Audio

1 特性

- 超低噪声：
 - 电压噪声：
 - 1 kHz 时为 $0.9 \text{ nV}/\sqrt{\text{Hz}}$, $I_{DS} = 5 \text{ mA}$
 - 1 kHz 时为 $1.1 \text{ nV}/\sqrt{\text{Hz}}$, $I_{DS} = 2 \text{ mA}$
 - 电流噪声：1 kHz 时为 $1.6 \text{ fA}/\sqrt{\text{Hz}}$
- 低 V_{GS} 失配：4 mV (最大值)
- 低栅极电流：10 pA (最大值)
- 低输入电容： $V_{DS} = 5 \text{ V}$ 时为 13 pF
- 高栅漏电压和栅源击穿电压：-40 V
- 高跨导：30 mS
- 封装：SOIC, 2mm × 2mm WSON (预发布)

2 应用

- 麦克风输入
- 水听器 and 船用设备
- DJ 控制器、混频器和其他 DJ 设备
- 专业音频混合器或控制平面
- 吉他放大器和其他乐器放大器
- 状态监控传感器

3 说明

JFE2140 是使用德州仪器 (TI) 现代高性能模拟双极工艺构建的 Burr-Brown™ 匹配对分立式 JFET。JFE2140 具有以前较旧的分立式 JFET 技术所不具备的性能。JFE2140 在所有电流范围内均提供出色的噪声性能，静态电流可由用户设置，范围为 50 μA 至 20

mA。当偏置电流为 5 mA 时，该器件会产生 $0.9 \text{ nV}/\sqrt{\text{Hz}}$ 的输入参考噪声，从而以极高的输入阻抗 ($>1 \text{ T}\Omega$) 提供超低噪声性能。此外，可按照 $\pm 4 \text{ mV}$ 测试 JFET 之间的匹配性，确保差分对配置具有低失调电压和高 CMRR 性能。JFE2140 还具有连接到独立钳位节点的集成二极管，无需添加高泄漏、非线性外部二极管即可提供保护。

JFE2140 可承受 40V 的高漏源电压，以及低至 -40V 的栅源电压和栅漏电压。该器件额定工作温度范围为 -40°C 至 +125°C。

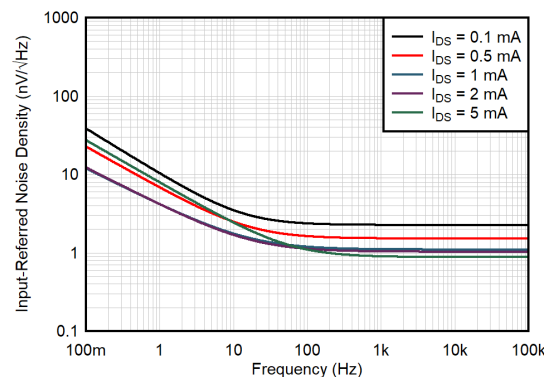
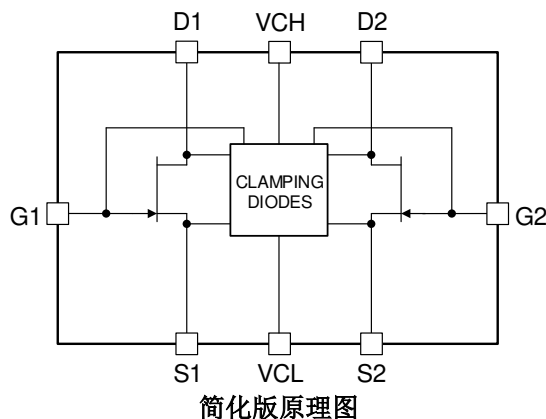
器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
JFE2140	WSON (8) - 预发布	2.00mm × 2.00mm
	SOIC (8)	4.90mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

器件概述

参数		值
V_{GSS}	栅源电压	-40 V
V_{DSS}	漏源电压	$\pm 40 \text{ V}$
C_{ISS}	输入电容	13 pF
$V_{GS1} - V_{GS2}$	差分栅源电压匹配	$\pm 4 \text{ mV}$
T_J	结温	-40°C 至 +125°C
I_{DSS}	漏源饱和电流	18 mA



超低输入电压噪声



Table of Contents

1 特性	1	8.4 Device Functional Modes.....	13
2 应用	1	9 Application and Implementation	14
3 说明	1	9.1 Application Information.....	14
4 Revision History	2	9.2 Typical Applications.....	18
5 Pin Configuration and Functions	3	10 Power Supply Recommendations	21
6 Specifications	4	11 Layout	21
6.1 Absolute Maximum Ratings.....	4	11.1 Layout Guidelines.....	21
6.2 ESD Ratings.....	4	11.2 Layout Example.....	21
6.3 Recommended Operating Conditions.....	4	12 Device and Documentation Support	22
6.4 Thermal Information.....	4	12.1 Device Support.....	22
6.5 Electrical Characteristics.....	6	12.2 Documentation Support.....	23
6.6 Typical Characteristics.....	7	12.3 接收文档更新通知.....	23
7 Parameter Measurement Information	11	12.4 支持资源.....	23
7.1 AC Measurement Configurations.....	11	12.5 Trademarks.....	23
8 Detailed Description	12	12.6 Electrostatic Discharge Caution.....	23
8.1 Overview.....	12	12.7 术语表.....	23
8.2 Functional Block Diagram.....	12	13 Mechanical, Packaging, and Orderable Information	23
8.3 Feature Description.....	12		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (August 2021) to Revision A (March 2022)	Page
• Changed ESD JEDEC specification to JS-002	4
• Changed gate-to-source voltages from -1.2 V to -1.3 V ($100\ \mu\text{A}$), -0.9 V to -1.1 V (2 mA)	6
• Changed Y-axis range from 0 to 33 to 0 to 16 on Figure 6-1, <i>Drain-to-Source Current vs Gate-to-Source Voltage</i>	7

5 Pin Configuration and Functions

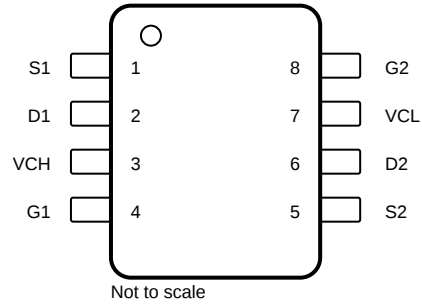


图 5-1. D (8-Pin SOIC) Package, Top View

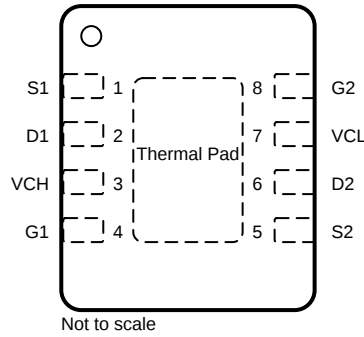


图 5-2. DSG (8-Pin WSON, Preview) Package, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D1	2	Output	Drain, channel 1
D2	6	Output	Drain, channel 2
G1	4	Input	Gate, channel 1
G2	8	Input	Gate, channel 2
S1	1	Output	Source, channel 1
S2	5	Output	Source, channel 2
VCH	3	—	Positive diode clamp voltage. Float this pin if clamp diodes are not used.
VCL	7	—	Negative diode clamp voltage. Float this pin if clamp diodes are not used.
Thermal Pad	Thermal Pad	—	Exposed thermal pad. This pad is internally connected to the V_{CL} node. Connect this pad to the same node as V_{CL} or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V_{DS}	Drain-to-source voltage	- 40	40	V
V_{GS}, V_{GD}	Gate-to-source voltage, gate-to-drain voltage	- 40	0.1	V
V_{VCH}	Voltage between VCH to D, G, or S		40	V
V_{VCL}	Voltage between VCL to D, G, or S	- 40		
I_{VCL}, I_{VCH}	Clamp diode current	DC	20	mA
		50-ms pulse ⁽³⁾	200	
I_{DS}	Drain-to-source current	- 50	50	mA
I_{GS}, I_{GD}	Gate-to-source current, gate-to-drain current	- 20	20	mA
T_A	Ambient temperature	- 55	150	°C
T_J	Junction temperature	- 55	150	°C
T_{stg}	Storage temperature	- 55	175	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All gate, drain and source voltages are referred to the same-channel JFET (that is, V_{GS} applies to both V_{G1S1} and V_{G2S2}).
- (3) Maximum diode current pulse specified for 50 ms at 1% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I_{DS}	Drain-to-source current	0.02		I_{DSS}	mA
V_{GS}	Gate-to-source voltage	- 1.2		0	V
T_J	Specified temperature	- 40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		JFE2140	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.4	°C/W

THERMAL METRIC ⁽¹⁾		JFE2140	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $I_{DS} = 2\text{ mA}$, $V_{DS} = 10\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
NOISE								
e_n	Input-referred noise	$I_{DS} = 100\ \mu\text{A}$	$f = 1\ \text{kHz}$		2.5		$\text{nV}/\sqrt{\text{Hz}}$	
			$f = 10\ \text{Hz}$		5.4			
			$f = 0.1\ \text{Hz to } 10\ \text{Hz}$		0.26		μV_{PP}	
		$I_{DS} = 2\ \text{mA}$	$f = 1\ \text{kHz}$		1.1		$\text{nV}/\sqrt{\text{Hz}}$	
			$f = 10\ \text{Hz}$		2.4			
			$f = 0.1\ \text{Hz to } 10\ \text{Hz}$		0.12		μV_{PP}	
e_i	Input current noise, each input	$f = 1\ \text{kHz}$, $I_{DS} = 2\ \text{mA}$, $V_{DS} = 5\ \text{V}$			1.6		$\text{fA}/\sqrt{\text{Hz}}$	
INPUT CURRENT								
I_G	Input gate current	$V_{DS} = 2\ \text{V}$, $V_{VCH} = 5\ \text{V}$, $V_{VCL} = -5\ \text{V}$			1	± 10	pA	
		$V_{DS} = 0\ \text{V}$, $V_{GS} = -30\ \text{V}$			0.2	± 60		
		$V_{DS} = 0\ \text{V}$, $V_{GS} = -30\ \text{V}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			0.85	nA
		$V_{DS} = 0\ \text{V}$, $V_{GS} = -30\ \text{V}$		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			9	
INPUT VOLTAGE								
V_{GSS}	Gate-to-source breakdown voltage	$V_{DS} = 0\ \text{V}$, $I_G = -100\ \mu\text{A}$				-40	V	
V_{GSC}	Gate-to-source cutoff voltage	$V_{DS} = 10\ \text{V}$, $I_{DS} = 0.1\ \mu\text{A}$		-1.5	-1.15	-0.9	V	
V_{GS}	Gate-to-source voltage	$I_{DS} = 100\ \mu\text{A}$		-1.3	-0.85	-0.7	V	
		$I_{DS} = 2\ \text{mA}$		-1.1	-0.6	-0.5		
ΔV_{GS}	Differential V_{GS} mismatch	$I_{DS} = 2\ \text{mA}$			1	4	mV	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		1.1	4.2		
	Differential V_{GS} mismatch drift	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			1.7	± 10	$\mu\text{V}/^\circ\text{C}$	
INPUT IMPEDANCE								
R_{IN}	Gate input resistance	$V_{GS} = -30\ \text{V to } -1\ \text{V}$, $V_{DS} = 0\ \text{V}$			1		$\text{T}\Omega$	
C_{ISS}	Input capacitance	$V_{DS} = 0\ \text{V}$			17		pF	
		$V_{DS} = 5\ \text{V}$			13			
OUTPUT								
I_{DSS}	Drain-to-source saturation current	$V_{GS} = 0\ \text{V}$		12	18	23	mA	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	10		28		
	Drain-to-source saturation current ratio	$V_{GS} = 0\ \text{V}$, I_{DSS1} / I_{DSS2}		0.95	1	1.05		
	Transconductance	$I_{DS} = 100\ \mu\text{A}$			2.1		mS	
		$I_{DS} = 2\ \text{mA}$			10			
G_{FS}	Full conduction transconductance	$V_{GS} = 0\ \text{V}$		24	30		mS	
V_{DSS}	Drain-to-source breakdown voltage	$I_{DS} = 100\ \mu\text{A}$		40	43		V	
C_{OSS}	Output capacitance	$I_{DS} = 2\ \text{mA}$			4.5		pF	

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $I_{DS} = 2\text{ mA}$, common-source configuration, and $V_{DS} = 10\text{ V}$ (unless otherwise noted)

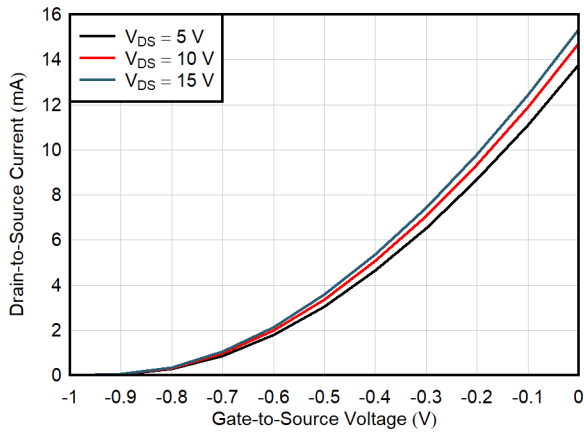


图 6-1. Drain-to-Source Current vs Gate-to-Source Voltage

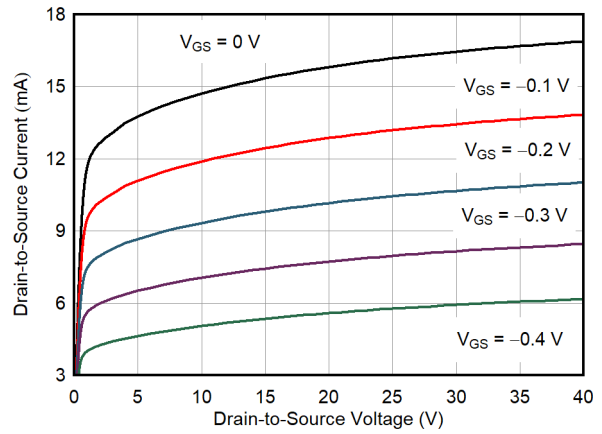


图 6-2. Drain-to-Source Current vs Drain-to-Source Voltage

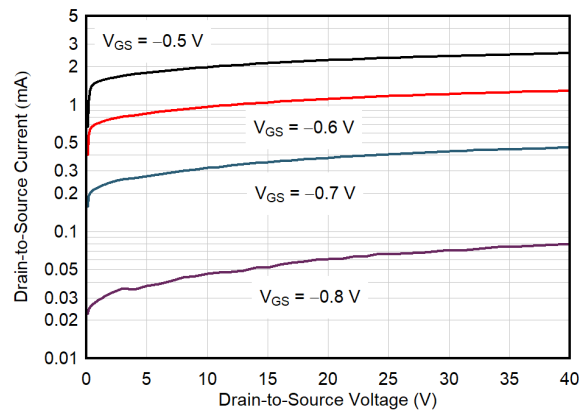


图 6-3. Drain-to-Source Current vs Drain-to-Source Voltage

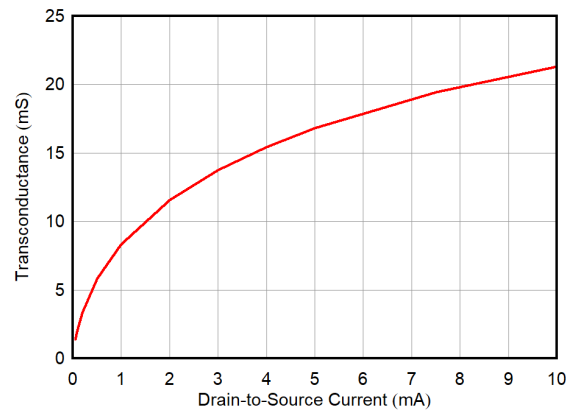


图 6-4. Common Source Transconductance vs Drain-to-Source Current

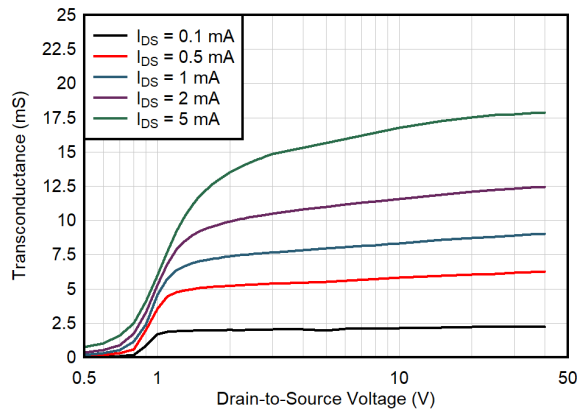


图 6-5. Common Source Transconductance vs Drain-to-Source Voltage

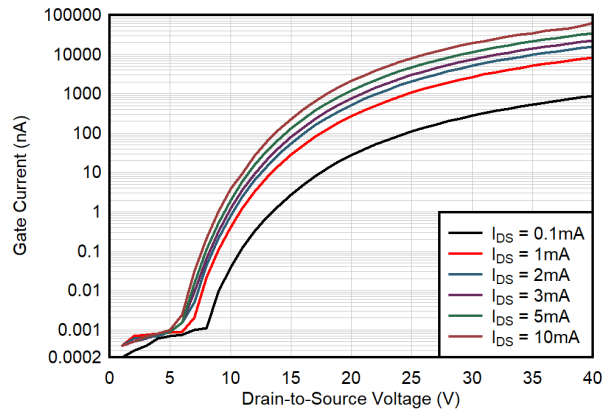
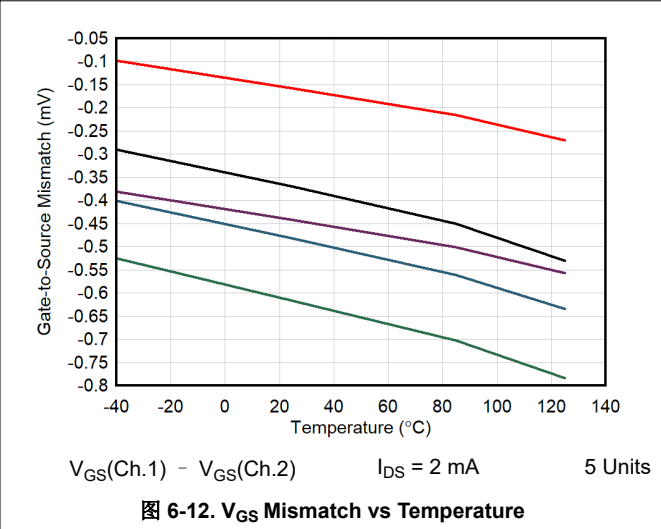
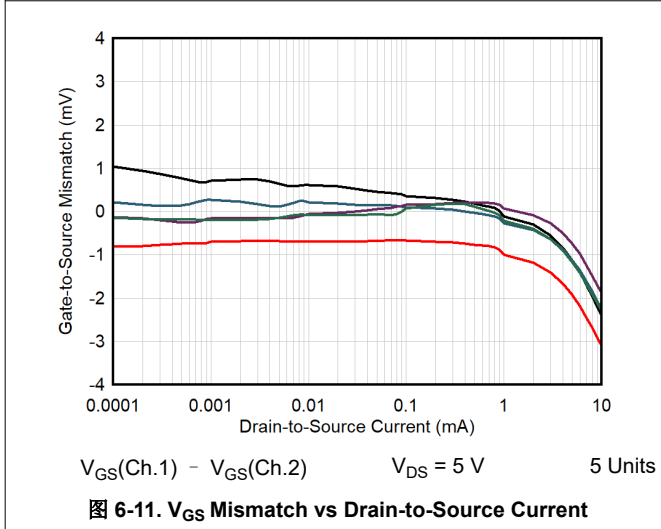
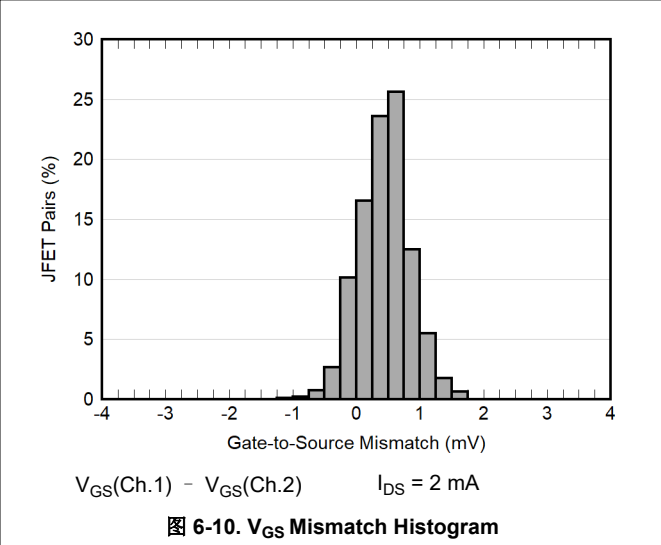
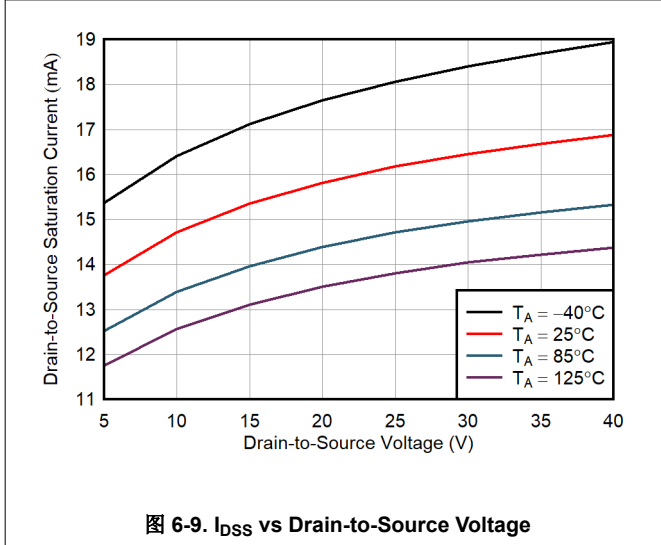
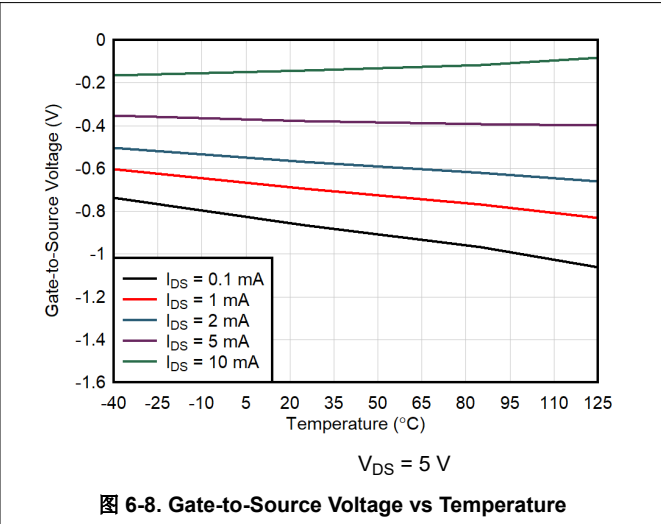
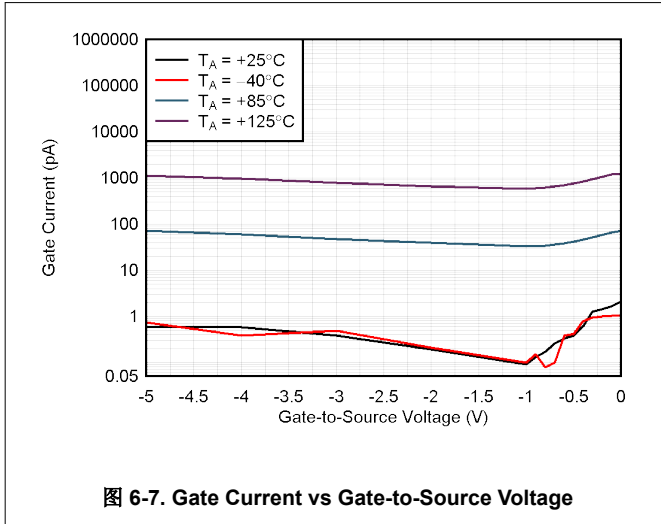


图 6-6. Gate Current vs Drain-to-Source Voltage

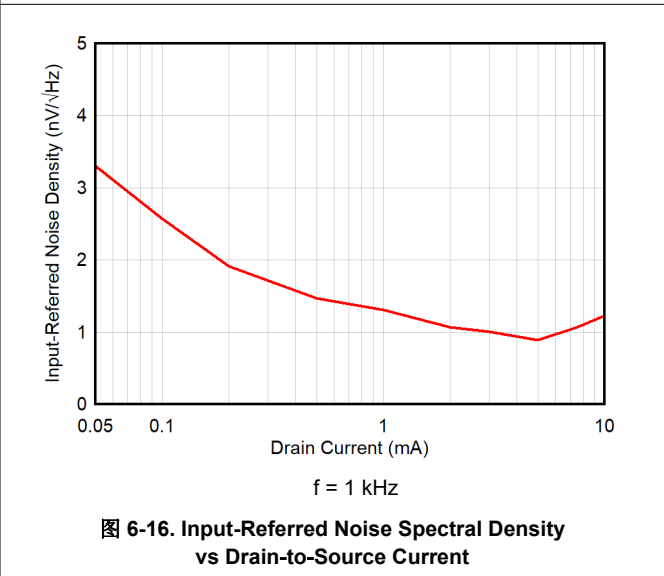
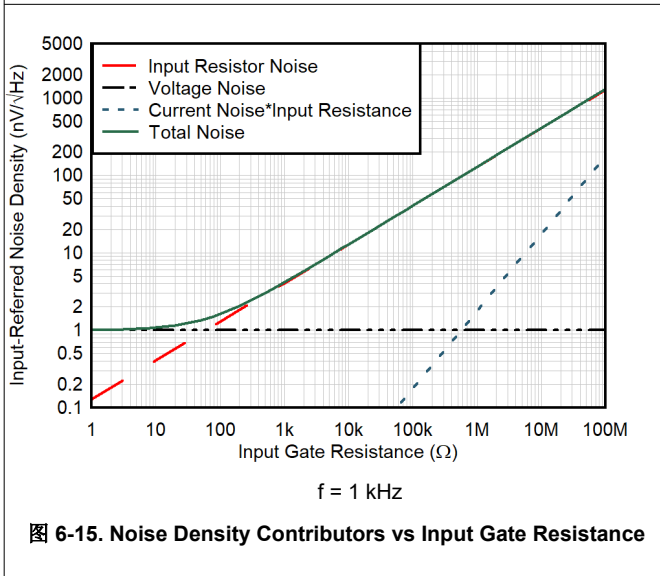
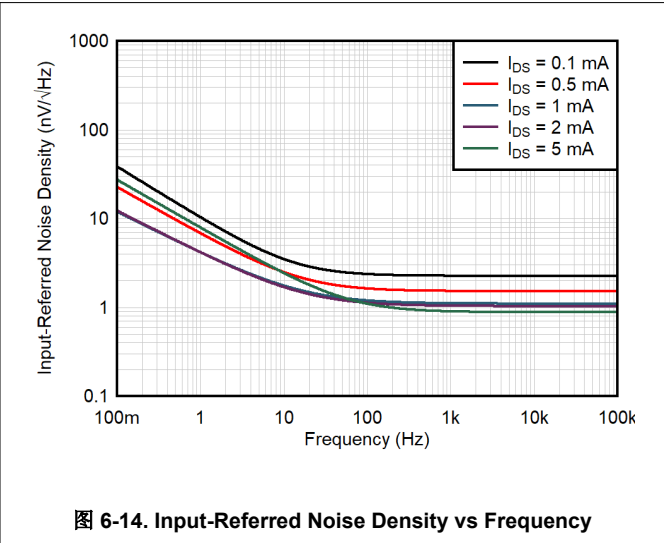
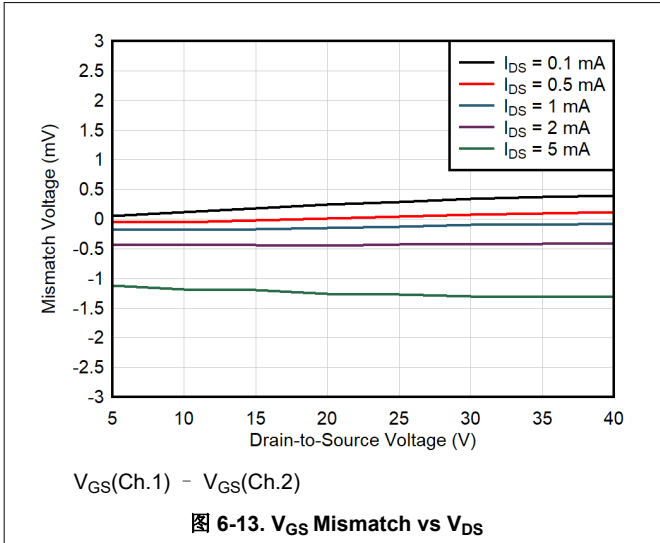
6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_{DS} = 2\text{ mA}$, common-source configuration, and $V_{DS} = 10\text{ V}$ (unless otherwise noted)



6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_{DS} = 2\text{ mA}$, common-source configuration, and $V_{DS} = 10\text{ V}$ (unless otherwise noted)



6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_{DS} = 2\text{ mA}$, common-source configuration, and $V_{DS} = 10\text{ V}$ (unless otherwise noted)

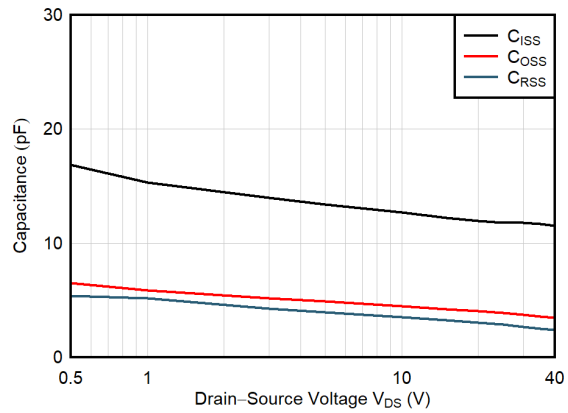


图 6-17. Input, Output, and Reverse Transfer Capacitance vs Drain-to-Source Voltage

7 Parameter Measurement Information

7.1 AC Measurement Configurations

The circuit configuration used for noise measurements is seen in [图 7-1](#). The nominal I_{DS} current is configured in the schematic by calibrating V^- . After I_{DS} is fixed, the V_{DS} voltage is set by calibrating V^+ . For input-referred noise data, the gain of the circuit is calibrated from V_{IN} to V_{OUT} and used for the input-referred gain calculation.

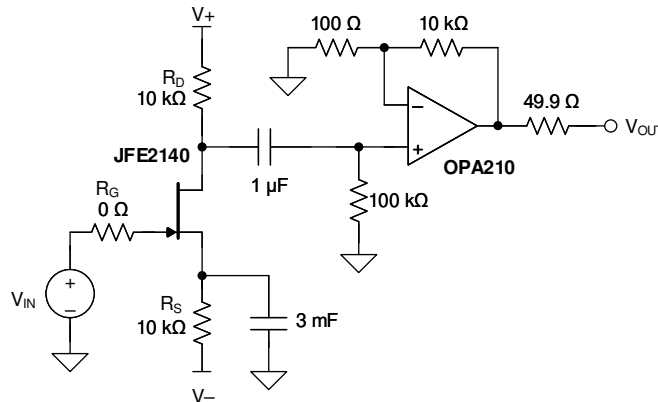


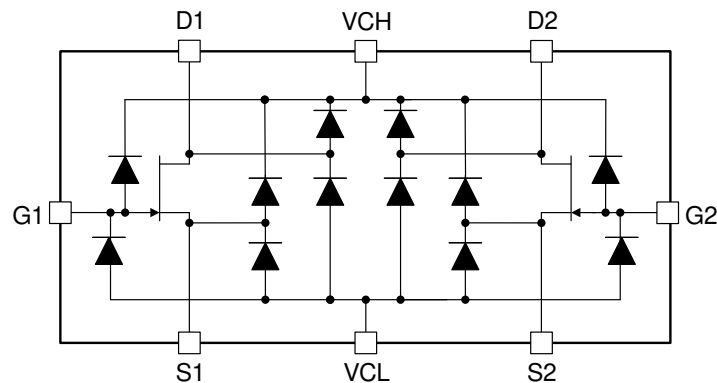
图 7-1. AC Measurement Reference Schematic

8 Detailed Description

8.1 Overview

The JFE2140 is a ultra-low noise, matched-input pair N-type JFET designed to create low-noise gain stages for very high output impedance sensors or microphones. Advanced, high precision processing technology gives the JFE2140 tight channel-to-channel matching, extremely low-noise performance, a high g_m/C_{ISS} ratio, and ultra-low gate-current performance. The integrated Input-protection diodes clamp high-voltage spurious input signals without the need for additional input diodes that can add leakage current or distortion-creating nonlinear capacitance. The JFE2140 provides a next-generation device to implement low-noise amplifiers for piezoelectric sensors, transducers, large-area condenser microphones, and hydrophones in small-package options.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Precision Matching

The JFE2140 features matched-pair, n-type JFET transistors fabricated on a high-precision analog process. Precision matching between opposite JFETs is required in differential-pair configurations, where any mismatch between input devices results in gain and common-mode rejection degradation. Precision matching also minimizes offset voltages that produce excessive error voltages in high-gain, dc-coupled composite amplifiers. Matching distribution for a production lot of units can be seen in [Figure 6-10](#).

8.3.2 Ultra-Low Noise

Junction field effect transistors (JFETs) are commonly used as an input stage in high-input-impedance, low-noise designs in audio, SONAR, vibration analysis, and other technologies. The JFE2140 is a new generation JFET device that offers very low noise performance at the lowest possible current consumption in high-input-impedance amplifier designs. The JFE2140 is manufactured on a high-performance analog process technology, giving tighter process parameter control than a standard JFET.

Designs that feature operational amplifiers (op amps) as the primary gain stage are common, but these designs are not able to achieve the lowest possible noise as a result of the inherent challenges and tradeoffs required from a full operational amplifier design. Noise in JFET designs can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or $1/f$ noise, is extremely important for systems that require signal gain at frequencies less than 100 Hz. The JFE2140 achieves extremely low $1/f$ noise in this range. Thermal noise is noise in the region greater than 1 kHz and depends on the gain, or g_m , of the circuit. The g_m is a function of the drain-to-source bias current; therefore, thermal noise is also a function of drain-to-source bias current. [Figure 6-14](#) shows both $1/f$ and thermal noise with multiple bias conditions measured using the circuit shown in [Figure 7-1](#).

Noise is typically modeled as a voltage source (voltage noise) and current source (current noise) on the input. The $1/f$ and thermal noise can be represented as voltage noise. Current noise is dominated by current flow into the gate, and is called *shot noise*. The JFE2140 features extremely low gate current, and therefore, extremely low current noise. [Figure 6-15](#) shows how source impedance on the input is the dominant noise source. In nearly all cases, noise created as a result of current noise is negligible.

8.3.3 Low Gate Current

The JFE2140 features a maximum gate current of 10 pA at room temperature, making the device an excellent choice for maximizing the gain and dynamic range from extremely high impedance sensors. Additionally, any noise contributions as a result of gate current are minimized because of the negligible shot noise at low current levels. As with all JFET devices, when the drain-to-source voltage increases, the gate current also increases. Keep the drain-to-source voltage to less than 5 V for the lowest gate input current operation.

8.3.4 Input Protection

The JFE2140 features input protection diodes that are used for surge clamping and ESD events. The diodes are rated to withstand high current surges for short times, steering current from the gate (G) pin to the VCH and VCL pins. The diodes also feature very low leakage, removing the need for external protection devices that may have high leakage currents or nonlinear capacitance that degrade the distortion performance.

8.4 Device Functional Modes

The JFE2140 functionality is identical to standard N-channel depletion JFET devices. The gate-to-source (V_{GS}) voltage, drain-to-source voltage (V_{DS}) and drain-to-source current (I_{DS}) determine the region of operation.

- For $V_{GS} < V_{GSC}$: JFE2140 conduction channel is closed; I_{DS} is only determined by junction leakage current.
- For $V_{GS} > V_{GSC}$: Two modes of operation can exist depending on V_{DS} . When V_{DS} is less than the linear (saturation) region threshold (see 图 8-1), the device operates in the linear region, meaning that the device behaves as a resistor connected from drain-to-source with minimal variation from any changes in V_{GS} . When V_{DS} is greater than the linear (saturation) region threshold, I_{DS} has a strong dependence on V_{GS} , where the relationship is described by the parameter g_m .

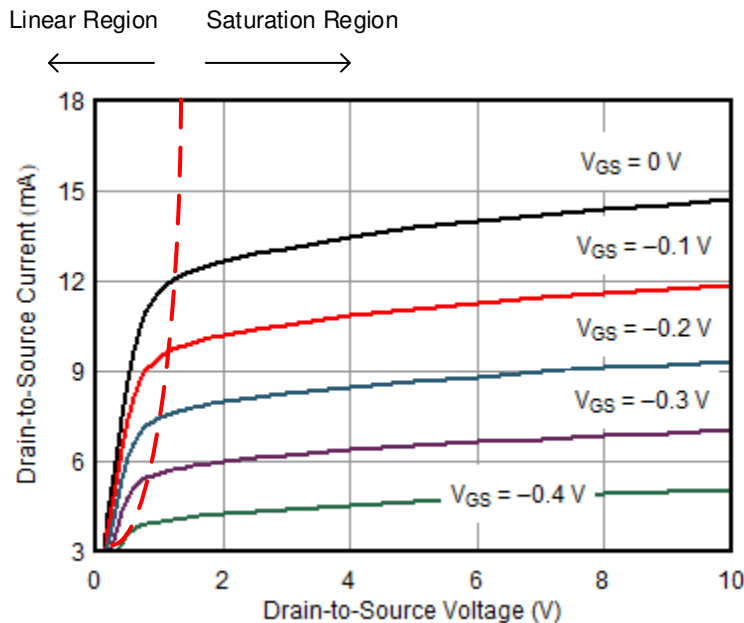


图 8-1. V_{DS} vs I_{DS}

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Protection Diodes

The JFE2140 features diodes that are used to help clamp voltage surges that can occur on the input sensor to the gate. The diodes are connected between the gates, sources, and drains of each JFET to two separate pins, VCL and VCH. The clamping mechanism works by *steering* current from the gate into the VCL or VCH nodes when the voltage at the gate, source or drain is less than VCL or greater than VCH. 图 9-1 shows an example of a microphone input circuit where a dc blocking capacitor operates with a large dc voltage. When the microphone input is dropped or shorted, the dc blocking capacitor discharges into the VCL or VCH nodes, thus helping eliminate large signal transient voltages on the gate. There are also clamping diodes from the drain and source to VCL and VCH, respectively. The clamping diodes can withstand high surge currents up to 200 mA for 50 ms; however, limit dc current to less than 20 mA.

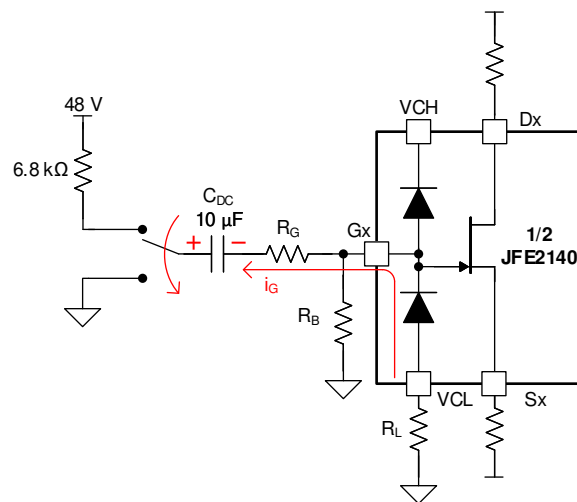


图 9-1. JFE2140 Clamping Diode Example

The example in 图 9-1 shows the diode clamp used to protect the JFET against overvoltage in a phantom-powered microphone circuit. Phantom power typically delivers 48 V through a 6.8-k Ω pullup resistor to a microphone or dynamic load. If the microphone is disconnected, dc blocking capacitor C_{DC} can be biased up to 48 V. If the input to the capacitor is then shorted to ground (shown by the switch in 图 9-1), the gate voltage can exceed the absolute maximum rating for V_{GS} . In this case, the blocking diode is used, along with current limiting resistors R_G and R_L , to clamp the gate voltage to a safe level. Be aware that the thermal noise of R_G couples directly into the gate input; therefore, make sure to minimize the resistance of R_G .

The clamping diodes are not required for operation. The V_{GS} voltage can withstand -40 V, so clamping is not required if the V_{GS} voltage is kept greater than this limit. If the diodes are not needed, leave the VCL and VCH nodes floating.

9.1.2 Cascode Configuration

The JFE2140 can be configured as a *cascoded* JFET front end. Cascode refers to using a second transistor in-series with the input transistor; see 图 9-2 for an example.

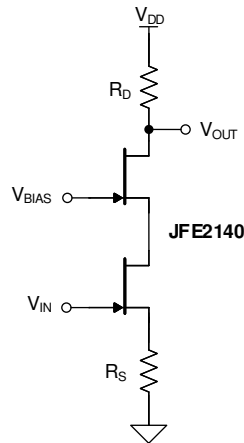


图 9-2. JFE2140 connected in Cascode Configuration

Using a cascode configuration, as shown in 图 9-2, increases the output impedance of the stage, resulting in higher gain, as well as buffers the input node from gate current that flows when the V_{DS} voltages are higher. The V_{BIAS} node must be forced to a voltage greater than what is required to allow both JFETs to remain in the saturated region. A JFET is not required to be used as the cascode device; the benefits of cascoding can be realized with other transistor types, while still maintaining the low-noise, high-impedance benefits of the JFE2140.

9.1.3 Common-Source Amplifier

The common-source amplifier is a commonly used open-loop gain stage for JFET amplifiers, the basic circuit is shown in 图 9-3.

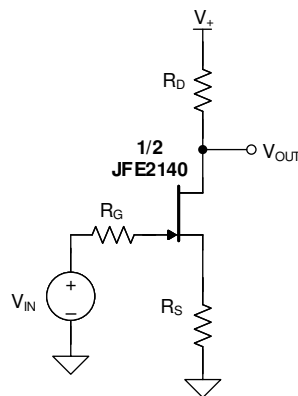


图 9-3. Common-Source Amplifier

The equation for gain of the circuit in 图 9-3 is shown in 方程式 1.

$$\frac{V_{OUT}}{V_{IN}} = - \frac{gm * R_D}{1 + gm * R_S} \quad (1)$$

Generally, higher gain results in improved noise performance. Gain increases as the bias current is increased as a result of increasing gm (see 图 6-4). As a result, the input-referred noise decreases as bias current is increased (see 图 6-14). Any JFET design must make a tradeoff between current consumption and noise performance. The JFE2140, however, delivers significantly lower noise performance than most operational

amplifiers at the same current consumption. The bias current (I_{DS}) is set by the value of the source resistor, R_S , and the threshold voltage, V_T , of the JFE2140. A graph showing nominal I_{DS} vs R_S is shown in 图 9-4.

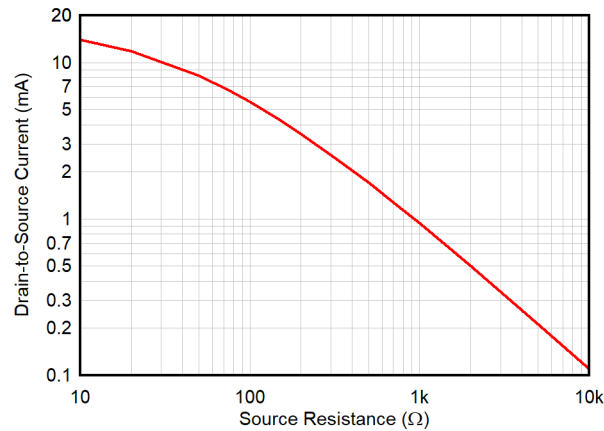


图 9-4. Drain-to-Source Current vs R_S , $V_{DS} = 5\text{ V}$

The bias current varies according to the resistor and threshold voltage tolerances. Additionally, thermal noise associated with R_S couples directly into the gain of the circuit, degrading the overall noise performance. To improve the circuit in 图 9-5, use a current-source biasing scheme. Current-source biasing removes the JFET threshold variation from the biasing scheme, and allows for lower-value filtering capacitance (C_S) for equivalent filtering due to the high output impedance of current sources.

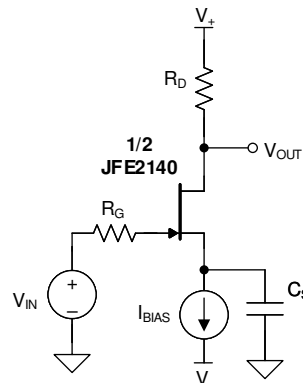


图 9-5. Common-Source Amplifier With Current-Source Biasing

9.1.4 Composite Amplifiers

The JFE2140 can be configured to provide a low-noise, high-input impedance front-end stage for a typical op amp. Open-loop transistor gain stages shown previously suffer from wide gain variations that are dependent on the forward transconductance of the JFE2140. When precision gain is required, the composite amplifier (JFET front-end + operational amplifier) achieves excellent results by allowing for a fixed gain determined by external resistors, and improving the noise and bandwidth of the operational amplifier. The JFE2140 gain stage provides a boost to the open-loop performance of the system, extending the bandwidth beyond what the operational amplifier alone can provide, and gives a high-input impedance, ultra-low noise input stage to interface with high source impedance microphones.

图 9-6 shows a generic schematic representation of a voltage-feedback composite amplifier. The component requirements and tradeoffs are listed in 表 9-1.

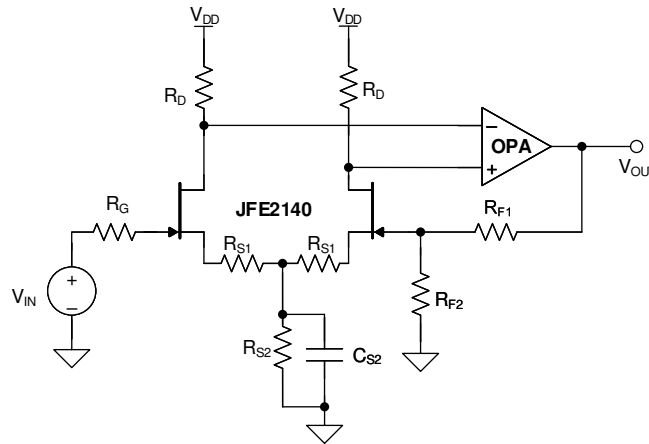


图 9-6. Low Noise, High Input Impedance Composite Amplifier

The gain of 图 9-6 can be calculated using the equation below.

$$A = 1 + \frac{R_{F1}}{R_{F2}} \quad (2)$$

表 9-1. Composite Amplifier Component List and Function

COMPONENT	DESCRIPTION
R _{S1}	Degeneration resistors. These resistors reduce the overall gain of the JFET stage, however, improve the linearity performance. Also, when used in differential configurations (see OPA1637 reference design) they will reduce CMRR errors that occur as a result of input mismatch voltages.
R _{S2}	Bias-current setting resistor. This resistor, along with R _{S1} , determine the bias current when using resistive biasing (see 图 9-4). Note both R _{S1} and R _{S2} resistance will directly impact noise performance.
R _G	Gate resistor. Can be used to help limit current flow into gate in overvoltage cases. For improved DC precision, match R _G to the equivalent parallel resistance of R _{S1} R _{S2} . Use the low resistance values to minimize the thermal noise impact on the circuit.
R _D	Drain resistor. Sets gain of JFET stage in common source biasing, along with g _m and R _{S1} + R _{S2} . Higher resistance will increase gain, however will lower the nominal V _{DS} voltage.
R _{F1}	Feedback resistor 1. Along with R _{F2} , sets the gain of the composite amplifier.
R _{F2}	Feedback resistor 2. Along with R _{F1} , sets the gain of the composite amplifier.
R _{S2}	Source resistor 2. Along with R _{S1} , sets the DC bias current where the JFET is nominally operated.
C _S	Source capacitor. Reduces the noise coupling from R _{S2} .

9.2 Typical Applications

9.2.1 Low-Noise, Low-Power, High-Input-Impedance Composite Amplifier

The JFE2140 can be configured to provide a low-noise, high-input impedance single-ended amplifier stage that can be optimized for ultra-low noise performance at low power levels. This configuration is designed for battery-powered audio applications such as guitar pedals, amplifiers and handheld recorders. The OPA1692, a low-power, dual audio amplifier, is used for the composite voltage-feedback amplifier, as well as a rail-splitting amplifier that centers the ground voltage between the battery positive and negative voltage.

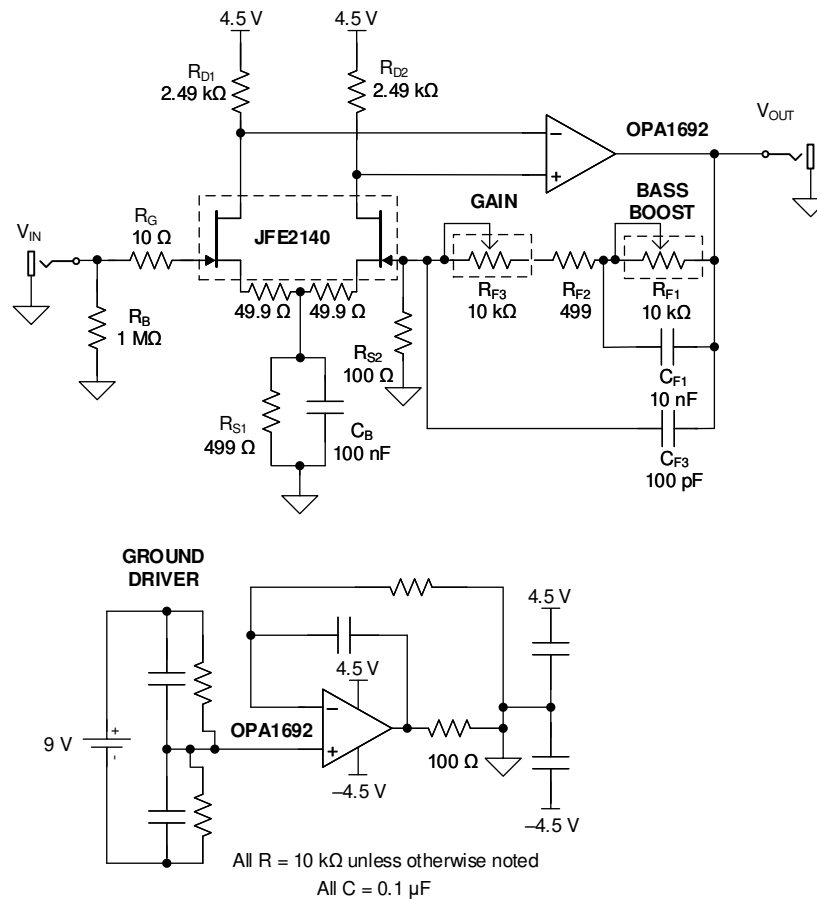


图 9-7. Low-Noise, Low-Power, High-Input-Impedance Composite Amplifier

9.2.1.1 Design Requirements

PARAMETER	DESIGN GOAL
Gain	15 dB to 40 dB nominal with low-frequency boost
Frequency response	1 Hz to 20 kHz
Noise	< 3 nV/√Hz at 1 kHz
Total current consumption	< 4 mA
Input current	< 100 pA

9.2.1.2 Detailed Design Procedure

This design provides single-ended, adjustable gain from 15 dB to 40 dB with extremely high input impedance at a very low frequency response. The power consumption is optimized for battery-powered audio applications.

- The JFE2140 is configured as a differential pair in a voltage-feedback composite amplifier. This configuration allows for low-frequency gain without large dc-blocking capacitors.
- The bias current is set by selecting the desired bias current and noise tradeoff (see [图 6-16](#)). To set the bias current point, adjust the source resistance according to [图 9-4](#).
- After the bias current is selected, set the JFET stage gain as high as possible. To avoid pushing the device into the linear region of operation, use the largest drain resistor ($R_{D1,2}$) possible while maintaining a minimum of 1 V across the drain-to-source nodes.
- The overall gain can be configured with the feedback resistors R_{F1} , R_{F2} and R_{F3} . Capacitor C_{F3} may be required depending on the gain configuration for amplifier stability; use amplifier stability best practices to maintain stability at both maximum and minimum gain configurations.

9.2.1.3 Application Curves

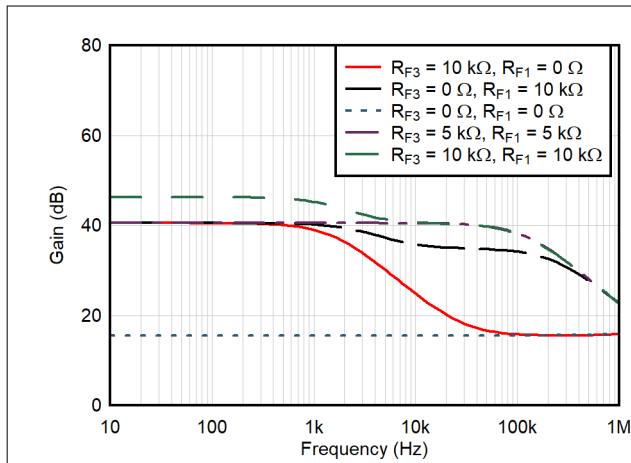


图 9-8. Gain/Phase

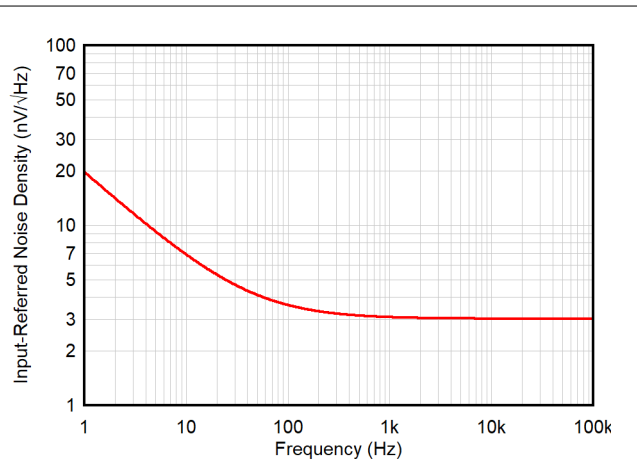


图 9-9. Input-Referred Noise Density

9.2.2 Differential Front-End Design

Differential pair architectures are useful for differential small signal amplification where high common-mode voltage rejection (CMRR) is required. In typical differential amplifiers or fully-differential amplifiers (FDA), the tolerance of the resistors alone dominates the CMRR performance. In addition, these amplifiers cannot be configured with high input impedance because of the requirement of input resistors. When used on the front-end of an FDA, the precision-matching on the JFE2140 removes the requirement of extremely low resistor matching (< 1%) by creating a matched-input gain stage. In addition, high input impedance significantly reduces the effects of source impedance mismatch on CMRR performance, creating a differential input designed for noisy environments that are common in professional audio.

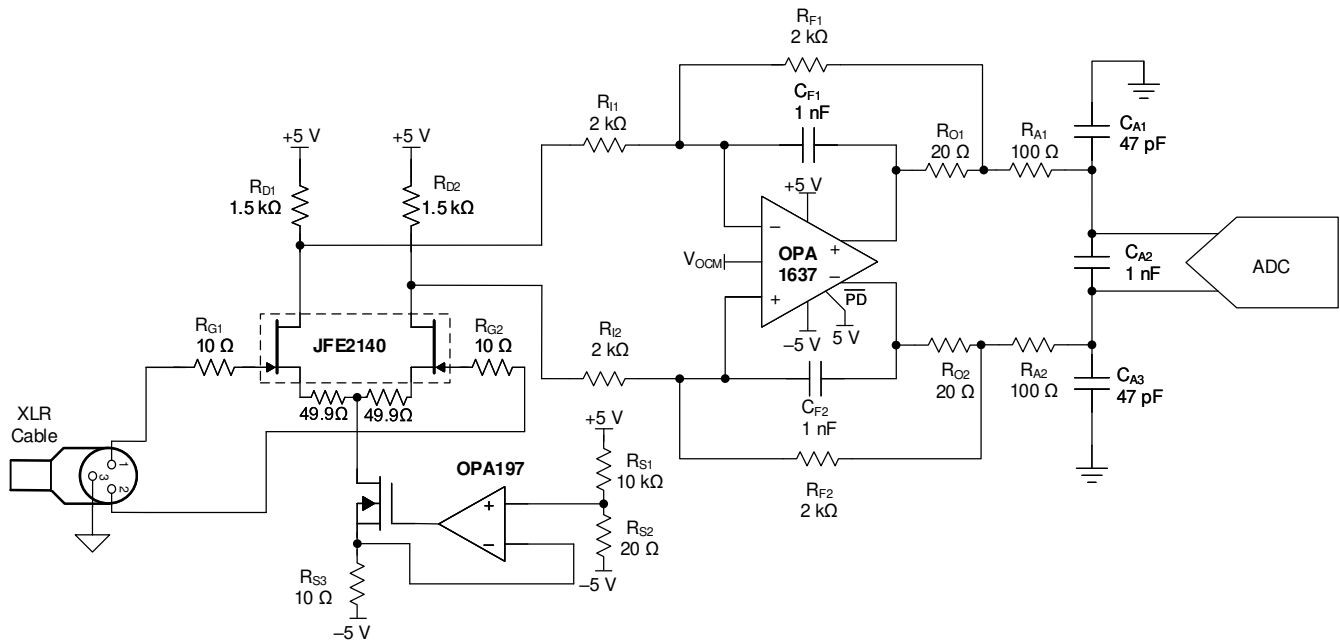


图 9-10. The JFE2140 as a High Input Impedance Front End for the OPA1637

9.2.2.1 Application Curves

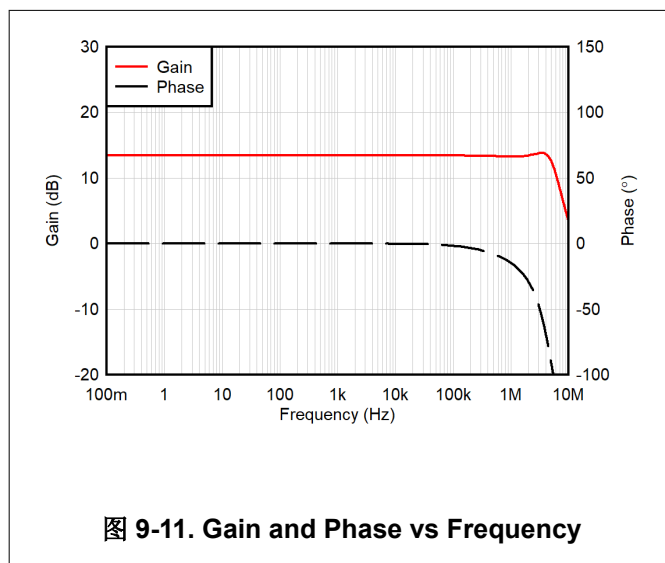


图 9-11. Gain and Phase vs Frequency

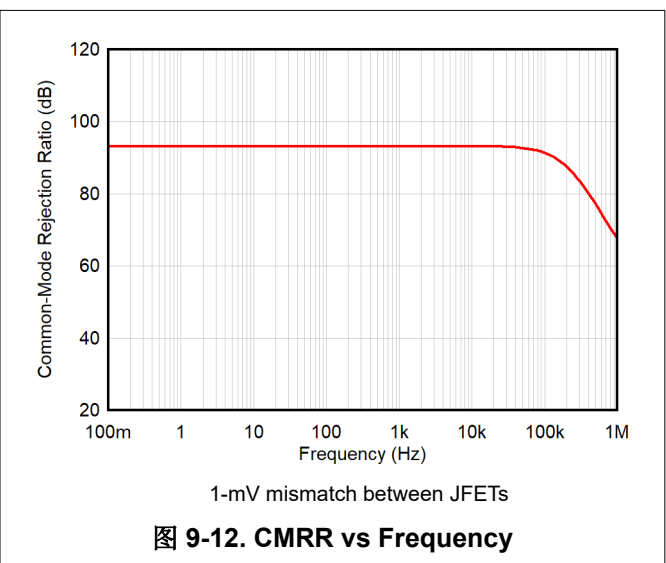


图 9-12. CMRR vs Frequency

10 Power Supply Recommendations

The JFE2140 is a dual, matched JFET transistor pair with clamping diodes. There are no specific power-supply connections; however, take care not to exceed any absolute maximum voltages on any of the pins if system supply voltages greater than or equal to 40 V are used.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Keep high impedance input signals away from noisy traces.
- Make sure supply voltages are adequately filtered.
- Minimize distance between source-connected and drain-connected components to the JFE2140.
- Consider a driven, low-impedance guard ring around the critical gate traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

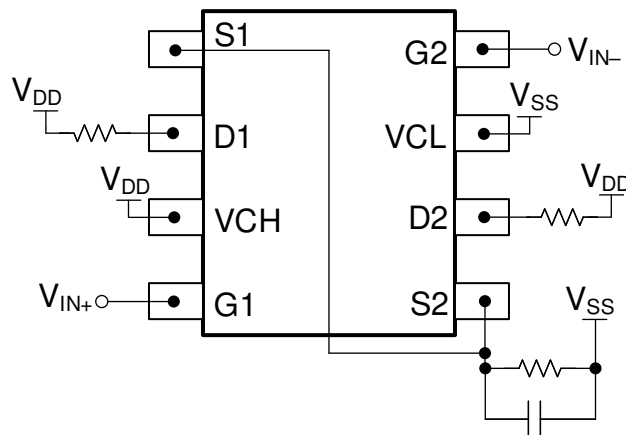


图 11-1. JFE2140 Layout Example: Differential Pair Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

12.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ simulation software is a free, fully functional version of the TINA software, preloaded with a library of macro models, in addition to a range of both passive and active models. TINA-TI software provides all the conventional dc, transient, and frequency domain analyses of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the WEBENCH® Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

12.1.1.3 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>.

12.1.1.4 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [OPAx202 Precision, Low-Noise, Heavy Capacitive Drive, 36-V Operational Amplifiers data sheet](#)
- Texas Instruments, [OPAx210 2.2-nV/√Hz Precision, Low-Power, 36-V Operational Amplifiers data sheet](#)
- Texas Instruments, [OPAx1692 Low-Power, Low-Noise and Low-Distortion SoundPlus™ Audio Operational Amplifiers data sheet](#)
- Texas Instruments, [OPAx197 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage Operational Amplifiers data sheet](#)

12.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

12.5 Trademarks

Burr-Brown™, TINA-TI™, and TI E2E™ are trademarks of Texas Instruments.

TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

WEBENCH® is a registered trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JFE2140DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	JF2140	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
JFE2140DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
JFE2140DR	SOIC	D	8	2500	356.0	356.0	35.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司