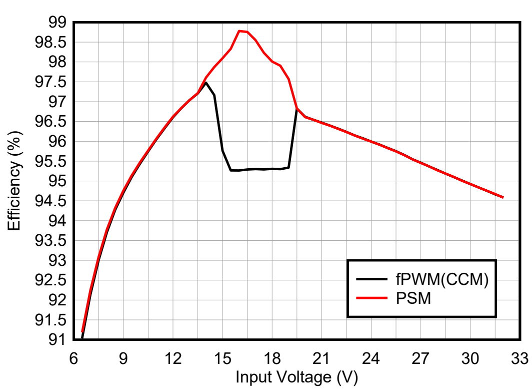
LM5177 80V 宽 V_{IN} 双向 4 开关降压/升压控制器

1 特性

- 宽输入电压范围（3.5V 至 78V，绝对最大值为 80V）
  - $V_{(BIAS)}$ > 3.5V 时，最小为 2.8V
- 输出电压范围为 3.3V 至 78V
- 低关断 I_Q (3 µA)
- 低工作 I_Q (60 µA)
- 3% 的反向电流限制精度可实现精确的充电电流
- 平均输入和输出电流监测器或限制器
- 对 PWM 或模拟输入信号进行输出电压动态跟踪
- 可选的省电模式 (PSM) 可实现高轻负载效率
- 两个集成式高压电源 LDO，支持自动选择
- 2A 峰值电流逻辑电平栅极驱动器
  - 集成式自举二极管
  - 自举过压和欠压保护
- 独立于工作模式（升压、降压/升压、降压）的固定频率
  - 可选的强制 PWM 模式
  - 开关频率高达 2MHz 可实现小解决方案和元件尺寸
  - 外部时钟同步
- 可选展频运行
- 可调节欠压和过压保护
- 断续模式过流保护



效率与输入电压间的关系 (I_O = 5A)

2 应用

- 非隔离式直流/直流电源（商用直流/直流、远程无线电单元、电机驱动控制）
- 备用电源系统（备用电池、消防安全）
- 工业 PC（单板计算机）
- 医疗 PSU（制氧机）
- 以太网供电（路由器）
- 太阳能电源（太阳能充电控制器）

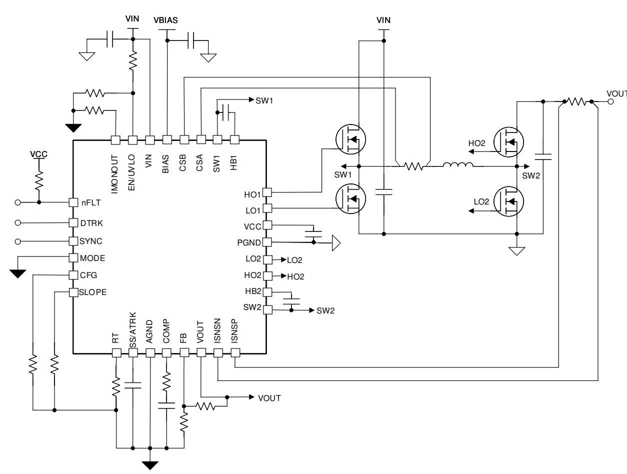
3 说明

LM5177 是一款四开关降压/升压控制器。无论输入电压是高于、等于还是低于调节后的输出电压，该器件均可提供稳定的输出电压。在省电模式下，该器件支持在整个输出电流范围内实现出色的效率。LM5177 以固定的开关频率运行，频率可通过 RT 或 SYNC 引脚进行设置。在降压、升压和降压/升压运行期间，开关频率保持不变。集成的可选平均电流监测器可帮助监测并限制 LM5177 的输入和输出电流。此功能还支持使用恒流 (CC) 和恒压 (CV) 模式为备用电源元件（如电池或电容器）充电。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
LM5177	DCP038	9.7mm × 4.4mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

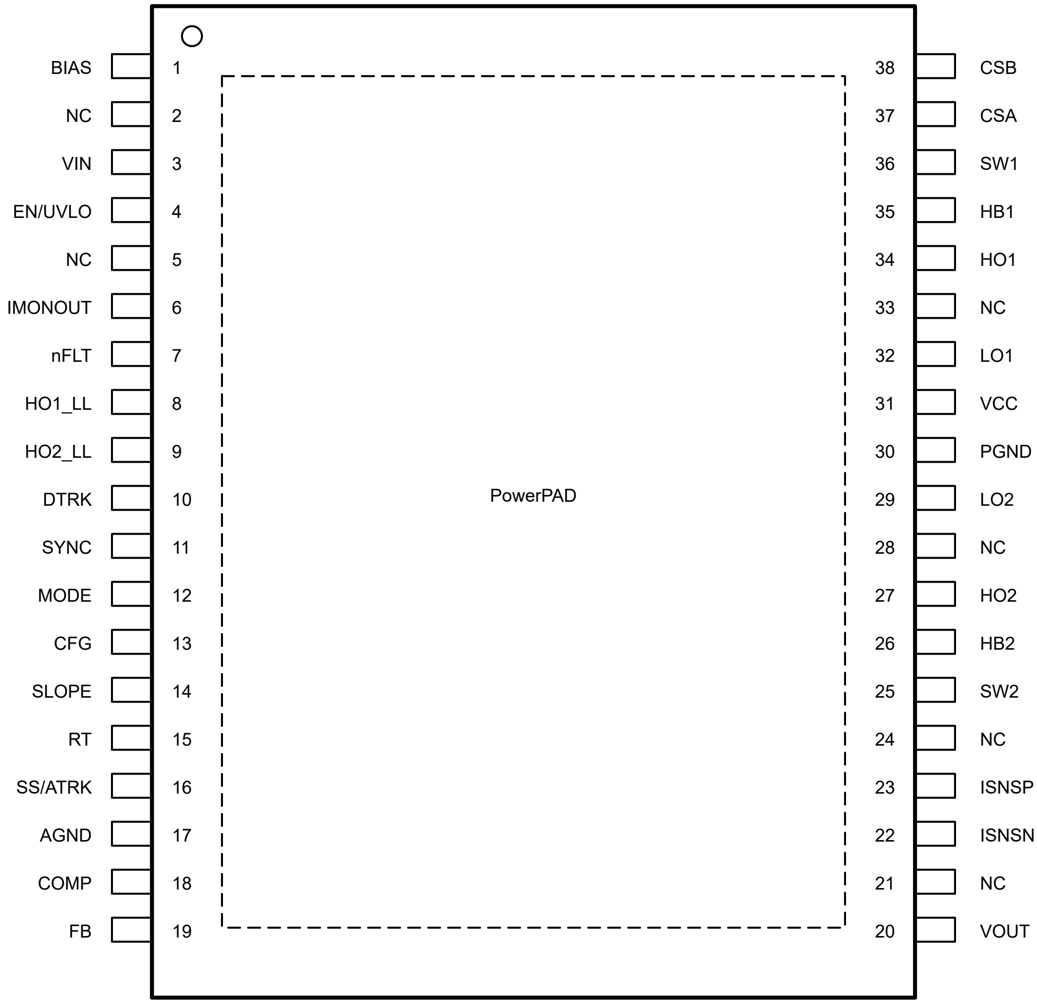
Changes from Revision A (October 2022) to Revision B (December 2022) — **Page**

- Added description for pin 8 and 9 and changed pin name to HO1_LL and HO2_LL ... 3
- Deleted fixed limitations with new material during product preview state. Changed top marking image. ... 6
- Add description for external gate driver connection ... 29
- Added description for the interaction of the different control loops during power backup ... 42

Changes from Revision * (June 2022) to Revision A (October 2022) — **Page**

- Added item number 7 for power save mode to known sample limitations list ... 6
- Changed equation for RT calculation ... 22
- Changed Functional Block Diagram of the Voltage and Peak Current Control Loop ... 23
- Changed description for negative current limit selection with SYNC-pin ... 27
- Changed equation for RT calculation ... 36
- Changed R_{C1} equation ... 40

5 Pin Configuration and Functions



Not to scale

图 5-1. 38-Pin DCP HTSSOP Pin Diagram

表 5-1. Pin Functions LM5177

Pin		Type[(1)]	Description
Name	No.		
AGND	17	G	Analog ground of the device
BIAS	1	I	Optional input to the VCC bias regulator. Powering VCC from an external supply instead of VIN can reduce power loss at high V_{IN}.
CFG	13	I/O	Device configuration pin. Connect a resistor between the CFG pin to select the device operation for spread spectrum (DRSS), short circuit protection (hiccup mode), current limit, or current monitor.
COMP	18	O	Output of the error amplifier. An external RC network connected between COMP and AGND compensates the regulator of the output voltage feedback loop.
CSA	37	I	Inductor peak current sensor positive input. Connect CSA to the positive side of the external current sense resistor using a low-current Kelvin connection.
CSB	38	I	Inductor peak current sense negative input. Connect CSB to the negative side of the external current sense resistor using a low-current Kelvin connection.
DTRK	10	I	Digital PWM input pin for the dynamical output voltage tracking. *Do not leave this pin floating.* If this function is not used, connect the pin to VCC or GND.

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表 5-1. Pin Functions LM5177 (continued)

Pin Name	Pin No.	Type(1)	Description
EN/UVLO	4	I	Enable pin. The pin enables or disables the device. If the pin is less than 0.6 V, the device shuts down. The pin must be raised above 0.65 V to enable the device. This pin is the enable pin for the device internal reference circuit and input voltage UVLO comparator input.
FB	19	I	Feedback pin for output voltage regulation. Connect a resistor divider network from the output of the converter to the FB pin. Connect the FB pin to VCC to operate at a fixed output voltage of 12 V.
HB1	35	P	Bootstrap supply pin for buck half-bridge. An external capacitor is required between the HB1 pin and the SW1 pin, respectively, to provide bias to the high-side MOSFET gate driver.
HO1	34	O	High-side gate driver output for the buck half-bridge
HO1_LL	8		Logic level output of the HO1 gate signal. Connect this ground reference PWM signal to an optional external gate-driver input. If the function is not used,make no external connection to this pin.
HB2	26	P	Bootstrap supply pin for boost half-bridge. An external capacitor is required between the HB2 pin and the SW2 pin, respectively, to provide bias to the high-side MOSFET gate driver.
HO2	27	O	High-side gate driver output for the boost half-bridge
HO2_LL	9		Logic level output of the HO2 gate signal. Connect this ground reference PWM signal to an optional external gate-driver input. If the function is not used ,make no external connection to this pin.
IMONOUT	6	O	Current monitor output pin. Output of the voltage-controlled current source of the optional current monitor. Connect the pin to a resistor to sense the voltage across. If the output or input current sense amplifier is configured as current limiter, an external RC network connected between IMONOUT and AGND compensates the regulator of the current feedback loop. Connect the IMONOUT pin to VCC to disable the block and reduce the quiescent current.
ISNSN	22	I	Positive sense input of the output or input current sense amplifier. An optional current sense resistor connected between ISNSN and ISNSP can be located either on the input side or on the output side of the power stage.
ISNSP	23	I	Negative sense input of the output or input current sense amplifier. An optional current sense resistor connected between ISNSN and ISNSP can be located either on the input side or on the output side of the power stage.
LO1	32	O	Low-side gate driver output for the buck half-bridge
LO2	29	O	Low-side gate driver output for the boost half-bridge
MODE	12	I	Digital input to select device operation mode. If the pin is pulled low, power save mode (PSM) is enabled. If the pin is pulled high, the forced PWM or CCM operation is enabled. The configuration can be changed dynamically during operation. *Do not leave this pin floating*. If this function is not used, connect the pin to VCC or GND.
NC	2	NC	No internal connection
NC	5	NC	No internal connection
NC	21	NC	No internal connection
NC	24	NC	No internal connection
NC	28	NC	No internal connection
NC	33	NC	No internal connection
nFLT	7	O	Open-drain output pin for fault indication or power good. This pin is pulled low when FB is outside a ±10% regulation window around the regulation window of the nominal output voltage.
PowerPAD	PAD	G	Connect the PowerPAD to the analog ground. Use thermal vias to connect to a PCB ground plane for improved power dissipation.
PGND	30	G	Power ground. This pin is the high current ground connection to the low-side gate drivers and for the internal VCC regulator.
RT	15	I/O	Switching frequency programming pin. An external resistor is connected to the RT pin and AGND to set the switching frequency.
SLOPE	14	I	A resistor connected between the SLOPE pin and AGND provides the slope compensation ramp for stable current mode operation in both buck and boost mode.

表 5-1. Pin Functions LM5177 (continued)

Pin		Type(1)	Description
Name	No.		
SS/ATRK	16	I/O	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start time. Analog output voltage tracking pin. The VOUT regulation target can be programmed by connecting the pin to variable voltage reference (for example, through a digital to analog converter). The internal circuit selects the lowest voltage applied to the pin.
SW1	36	P	Inductor switch node for the buck half-bridge
SW2	25	P	Inductor switch node for the buck half-bridge
SYNC	11	I	Synchronization clock input. The internal oscillator can be synchronized to an external clock during operation. If the output or input current sense amplifier is configured as a current limiter pulling, this pin is low during start-up, device switches the current limit direction to a negative polarity. *Do not leave this pin floating*. If this function is not used, connect the pin to VCC.
VCC	31	P	Internal linear bias regulator output. Connect a ceramic decoupling capacitor from VCC to PGND.
VIN	3	I	The input supply and sense input of the device. Connect VIN to the supply voltage of the power stage.
VOUT	20	I	VOUT sense input. Connect to the power stage output rail.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

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6 Specifications

Product Preview Samples

备注

The sample material during product preview state (see 图 6-1 for the package top marking) shows the following limitations which are identified during the silicon validation process:

1. If the μSleep mode is disabled, some devices can show an increased input quiescence current of about 2.5 mA, which affects the light load efficiency in power save mode (burst operation). TI recommends activating μSleep for best light load efficiency.
2. Under light load operation i.e. load currents in which the inductor current is very close the to the power save mode entry threshold (typ. 15% of Ipeak) it has been observed that the switching operation stops and the output voltage decays to zero volts. The converter will latch in this operation condition. To avoid this behavior or operate at such output current condition it is recommended to set the force PWM operation mode by pulling the MODE-pin high.

The previously mentioned limitations are intended to disappear in the final and qualified material.

For further information and inquiries about the previously mentioned descriptions, contact TI through e-mail at lm5177-support@list.ti.com.

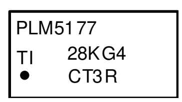

图 6-1. Samples Top Marking

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6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)[1]

		MIN	MAX	UNIT
Input	BIAS to AGND	–0.3	50	V
	VIN to AGND	–0.3	80	
	EN/UVLO to AGND	–0.3	$V_{(VIN)}$ + 0.3	
	SS/ATRK, DTRK, RT, SYNC, MODE, SLOPE, CFG, to AGND[2]	–0.3	5.8	
	FB to AGND	–0.3	5.8	
	CSA, CSB to AGND (DC)	–0.7	80	
	CSA, CSB to AGND (35-ns transient)	–5	80	
	SW1, SW2 to AGND (DC)	–0.7	80	
	SW1, SW2 to AGND (35-ns transient)	–5	80	
	HB1 to SW1, CSA, CSB	–0.3	5.5[5]	
		–0.3	7.8	
	HB2 to SW2, CSA, CSB	–0.3	5.5[5]	
		–0.3	7.8	
	SW1 to CSA, CSB	–0.3	0.3	
	PGND to AGND	–0.3	0.3	
Output	VCC to AGND	–0.3	5.5	V
	VOUT to AGND	–0.3	80	
	LO1, LO2, to AGND (DC)	–5	$V_{(VCC)}$ + 0.3	
	nFLT to AGND	–0.3	5.8	
	HO1, HO2, ISNSP, ISNSN, HB1, HB2 to AGND (DC)	–0.3	85	
	COMP, IMONOUT to AGND[3]	–0.3	5.8	
Storage temperature, T_{STG}		–55	150	°C
Operating junction temperature, T_J [4]		–40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) This pin is not specified to have an external voltage applied.
(3) This pin has an internal maximum voltage clamp which can handle up to 1.6 mA.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(5) Operating lifetime is de-rated for voltage bigger than the specified maximum.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002[2]	Corner pins	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

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6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)[(1)]

		MIN	NOM	MAX	UNIT
$V_{(VIN)}$	Input voltage sense	2.8		78	V
$V_{(VOUT)}$	Output voltage sense	3.3		78	V
$V_{(IMON)}$	ISNSP, ISNSN	2.8		78	V
$V_{(VCC)}$	VCC voltage	3.6		5.3	V
$C_{(VCC)}$	VCC regulator output capacitance	10			µF
V_{FB}	FB input	0		$V_{(VCC)}$ +0.3	V
V_{IL}	Logic pin low level			0.4	V
V_{IH}	Logic pin high level	1.3			V
f_{SW}	Typical switching frequency	100		2000	kHz
$f_{(SYNC)}$	Synchronization switching frequency limits	100		2000	kHz
	Synchronization frequency range relative to RT center frequency			±50%	
$f_{(DTRK)}$	Tracking input frequency range	TBD	500	TBD	kHz
	Tracking input minimum off time or on time	75			ns
	Differential voltage for ISNSN to ISNSP		50	55	mV
T_J	Operating junction temperature[(2)]	–40		125	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[(1)]		HTSSOP 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ = 12 V

PARAMETER					MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
	Shutdown current into VIN		$V_{(VIN)}$ = 12 V, $V_{(BIAS)}$ = 0 V, $V_{(EN)}$ = 0 V			2.8		μA
	Shutdown current into BIAS		$V_{(VIN)}$ = 0 V, $V_{(EN)}$ = 0 V			2.8		μA
	Stand-by current into VIN		$V_{(VIN)}$ = 78 V, $V_{(BIAS)}$ = 0 V, 0.7 V > $V_{(EN)}$ ≤ 1.25 V			45		μA
	Quiescent current into BIAS		$V_{(EN)}$ = 3.3 V, $V_{(FB)}$ > 1 V, μ Sleep enabled			60		μA
I_{IL}	Low-level input current	EN/UVLO	$V_{(EN/UVLO)}$ ≤ 0.55 V			±0.01		μA
VCC REGULATOR								
	VCC regulation		V_{BIAS} 12.0 V, $I_{(VCC)}$ = 20 mA			5		V
			V_{VIN} 12.0 V, $I_{(VCC)}$ = 20 mA			5		V
	BIAS LDO load regulation in dropout operation		V_{BIAS} = 3.5 V, $I_{(VCC)}$ = 50 mA			200		mV
	VCC line regulation		$I_{(VCC)}$ = 1 mA	$V_{(VIN)}$ = 3.5 V, $V_{(BIAS)}$ = 6.7 V to 42 V		±1%		
				$V_{(BIAS)}$ = 0 V, $V_{(VIN)}$ = 6.7 V to 78 V		±1%		
	BIAS LDO dropout load regulation		$V_{(BIAS)}$ = 6.7 V, $V_{(VIN)}$ = 3.5 V	$I_{(VCC)}$ = 1 mA to 200 mA		7		mV
	VIN LDO dropout load regulation		$V_{(BIAS)}$ = 0 V, $V_{(VIN)}$ = 6.7 V	$I_{(VCC)}$ = 1 mA to 175 mA		7		mV
	VCC UVLO delay		VCC rising			6		μs
	VCC sourcing current limit		VCC = 3.7 V, T_J = 25°C to 150°C	$V_{(BIAS)}$ = 0 V, $V_{(VIN)}$ = 6.7 V,	200			mA
				$V_{(BIAS)}$ = 6.7 V, $V_{(VIN)}$ = 3.5 V	200			mA
$V_{T+(VCC)}$	Positive-going threshold		V(VCC) rising			3.45		V
$V_{T-(VCC)}$	Negative-going threshold		V(VCC) falling			3.25		V
$V_{T+(VCC,SUP)}$	Positive-going threshold for LDO switch-over					6.5		V
ENABLE								
$V_{T+(EN)}$	Enable positive-going threshold		EN rising			0.63		V
$V_{T-(EN)}$	Enable negative-going threshold		EN falling			0.6		V
$V_{hyst(EN)}$	Enable threshold hysteresis		EN falling			20		mV
$t_{d(EN)}$	Shutdown delay time					20		μs
UVLO								
$V_{T+(UVLO)}$	UVLO positive-going threshold		$V_{(EN/UVLO)}$ rising			1.28		V
$V_{T-(UVLO)}$	UVLO negative-going threshold		$V_{(EN/UVLO)}$ falling			1.23		V
$V_{hyst(UVLO)}$	UVLO threshold hysteresis		$V_{(EN/UVLO)}$ falling			50		mV
I_{UVLO}	UVLO hystereses sinking current		0.7 V ≤ $V_{(EN/UVLO)}$ < 1.24 V			5		μA
	Enable time to start switching		VCC = 5 V, $V_{T+(UVLO)}$ > 1.3 V			45		μs
$t_{d(UVLO)}$	UVLO detection delay time		$V_{(EN/UVLO)}$ falling; $V_{(VDET)}$ falling			30		μs
SYNC								
$V_{T+(SYNC)}$	Sync input positive-going threshold						1.19	V
$V_{T-(SYNC)}$	Sync input negative-going threshold				0.41			V

ADVANCE INFORMATION

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ = 12 V

PARAMETER				MIN	TYP	MAX	UNIT
$t_{d(Det,Sync)}$	Sync activity detection delay	Referred to $f_{(SYNC)}$				3	cycles
SOFT START							
$I_{(SS)}$	Soft-start current				10		µA
	SS pulldown switch, $R_{DS(on)}$	$V_{(SS)}$ = 1 V			23		Ω
$t_{d(DISCH;SS)}$	SS pin discharge time	Time from internal SS discharge until the soft-start current can charge the pin again			500		µs
$V_{(SS,clamp)}$	Clamp voltage for the SS pin				4.1		V
PULSE WIDTH MODULATION							
	Switching frequency	R_{RT} = 14.7 kΩ		1845	2050	2255	kHz
	Switching frequency	R_{RT} = 316 kΩ		90	100	110	kHz
	Minimum controllable on time	FPWM, R_{RT} = 14.7 kΩ	Boost mode		58		ns
			Buck mode		98		ns
	Minimum controllable off time		Boost mode		97		ns
			Buck mode		92		ns
	RT regulation voltage				0.75		V
SPREAD SPECTRUM							
	Switching frequency modulation range	Upper limit			7.8%		
		Lower limit			–7.8%		
VOUT TRACKING							
$V_{T+(DTRK)}$	DTRK positive-going threshold	$V_{(DTRK)}$ rising				1.19	V
$V_{T-(DTRK)}$	DTRK negative-going threshold	$V_{(DTRK)}$ falling		0.41			V
	DTRK activity detection frequency				135		kHz
$t_{d(Det,DTRK)}$	DTRK activity detection delay	Referred to $f_{(DTRK)}$				3	cycles
fc(LPF)	Corner frequency of internal low pass				35		kHz
MODE SELECTION							
$V_{T+(MODE)}$	Mode input positive-going threshold					1.19	V
$V_{T-(MODE)}$	Mode input negative-going threshold			0.41			V
CURRENT SENSE							
	Positive peak current limit threshold			45	50	55	mV
	Negative peak current limit threshold			–55	–50	–45	mV
	PSM entry threshold	PSM_ENTRY_THRESHOLD = 0b01			5		mV
CURRENT MONITOR AND LIMITER							
	Current sense amplifier transconductance	IMON_LIMITER_EN = 0b0	0 mV ≤ $\Delta V_{(ISNS)}$ ≤ 50 mV		1		mS
	Offset voltage[1]	IMON_LIMITER_EN = 0b0	T_J= 25℃		±1		mV
	Current sense amplifier bandwidth	IMON_LIMITER_EN = 0b0			2		MHz
	Output current IMONOUT		$\Delta V_{(IMON)}$ = 45 mV		45		µA
			$\Delta V_{(IMON)}$ = 5 mV		5		µA
	Current sense amplifier transconductance	IMON_LIMITER_EN = 0b1			200		µS

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ = 12 V

PARAMETER					MIN	TYP	MAX	UNIT
$\Delta V_{(ISNS)}$	Current sense offset and threshold voltage		IMON_LIMITER_EN = 0b1	T_J = 25℃		50		mV
	ISNS pin input bias currents		ISNSP = ISNSN = 12 V			80		µA
$V_{T+(DIS,IMON)}$	Positive-going threshold to disable IMON		Referred to VCC			65%		
HICCUP MODE PROTECTION								
	Hiccup mode on time					1		ms
	Hiccup mode off time					24		ms
ERROR AMPLIFIER								
V_{REF}	FB reference voltage	FB reference			0.99	1	1.01	V
	FB pin leakage current		$V_{(FB)}$ = 1 V			60		nA
	Internal FB divider ratio		$V_{(FB)}$ > 3.1 V			20		V/V
	Transconductance					600		µS
	Output resistance					96		MΩ
	COMP sourcing current					100		uA
	COMP sinking current					100		uA
	COMP clamp voltage		$V_{(FB)}$ = 990 mV			1.25		V
	COMP clamp voltage		$V_{(FB)}$ = 1.01 V			0.24		V
	Unity gain bandwidth					4.5		MHz
$V_{T+(SEL,iFB)}$	Positive going threshold to select internal FB operation		$V_{(FB)}$ rising			2.5		V
OVP								
VT+(OVP)	Overvoltage rising threshold		FB rising reference to V_{REF}			110%		
VT-(OVP)	Overvoltage falling threshold		FB falling reference to V_{REF}			105%		
	Overvoltage de-glitch time					10		µs
VT+(OVP2)	Overvoltage 2 rising threshold		$V_{(VOUT)}$ rising			83.5		V
nFLT								
	nFLT pulldown switch on resistance		1-mA sinking			90		Ω
	Power-good positive-going threshold		FB rising (reference to V_{REF})			95%		
	Power-good negative-going threshold		FB falling (reference to V_{REF})			90%		
	nFLT off-state leakage		$V_{(nFLT)}$ = 5 V				100	nA
$t_{d(nFLT\text{-}PIN)}$	nFLT pin reaction time		Measured from a fault event until nFLT goes low				37	µs
MOSFET DRIVER								
t_r	Rise time	HG1, HG2, LG1, LG2	C_G = 3.3 nF			12		ns
t_f	Fall time	HG1, HG2, LG1, LG2	C_G = 3.3 nF			12		ns

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Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ = 12 V

PARAMETER					MIN	TYP	MAX	UNIT
t_t	Transition (dead) time	HOx from high to low and LOx from low to high	C_G = 3.3 nF	$R_{(RT)}$ = 14.7 kΩ		17		ns
		HOx from low to high and LOx from high to low				22		ns
		HOx from high to low and LOx from low to high		$R_{(RT)}$ = 316 k Ω		55		ns
		HOx from low to high and LOx from high to low				60		ns
	Gate driver low-side PMOS on-resistance	LO1, LO2	$I_{(test)}$ = 200 mA			1.12		Ω
	Gate driver high-side PMOS on-resistance	HO1, HO2	$I_{(test)}$ = 200 mA			1.16		Ω
	Gate driver low-side NMOS on-resistance	LO1, LO2	$I_{(test)}$ = 200 mA			0.5		Ω
	Gate driver low-side NMOS on-resistance	HO1, HO2	$I_{(test)}$ = 200 mA			0.51		Ω
V_{TH-} (BST_UV)	Negative-going bootstrap UVLO2 threshold		V(HBx) – V(SWx) falling			2.75		V
V_{TH+} (BST_UV)	Positive-going bootstrap UVLO2 threshold		V(HBx) – V(SWx) rising			2.95		V
V_{TH+} (BST_OV)	Positive-going bootstrap over-voltage threshold		V(HBx) – V(SWx) rising, I_HBx = 10 mA			6		V
V_{TH} (GATEOUT)	Low-side and high-side gate driver output switching detection		Referenced to VCC			37%		
			Referenced to V(HBx) – V(SWx)			37%		
THERMAL SHUTDOWN								
T_{T+J}	Thermal shutdown threshold		T_J rising			164		°C
	Thermal shutdown hysteresis					15		°C
R2D INTERFACE								
	Internal reference resistor					33		kΩ

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ = 12 V

PARAMETER				MIN	TYP	MAX	UNIT
R_{CFG}	External selection resistor resistance	R2D setting #0			0		kΩ
		R2D setting #1			0.511		kΩ
		R2D setting #2			1.15		kΩ
		R2D setting #3			1.87		kΩ
		R2D setting #4			2.74		kΩ
		R2D setting #5			3.83		kΩ
		R2D setting #6			5.11		kΩ
		R2D setting #7			6.49		kΩ
		R2D setting #8			8.25		kΩ
		R2D setting #9			10.5		kΩ
		R2D setting #10			13.3		kΩ
		R2D setting #11			16.2		kΩ
		R2D setting #12			20.5		kΩ
		R2D setting #13			24.9		kΩ
		R2D setting #14			30.1		kΩ
		R2D setting #15			36.5		kΩ

(1) Zero offset is determined by interpolation

6.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
OVERALL DEVICE FEATURES						
	Minimum time low EN toggle	time measured from EN toggle from H to L and from L to H	TBD			μs

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6.7 Typical Characteristics

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC)}$ = 5 V

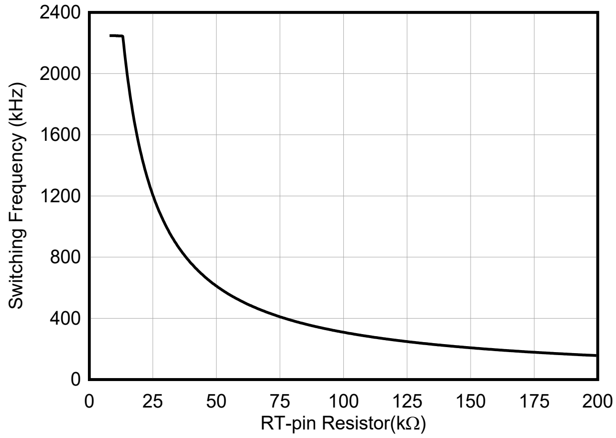

图 **6-2. Switching Frequency Versus RT Resistance**

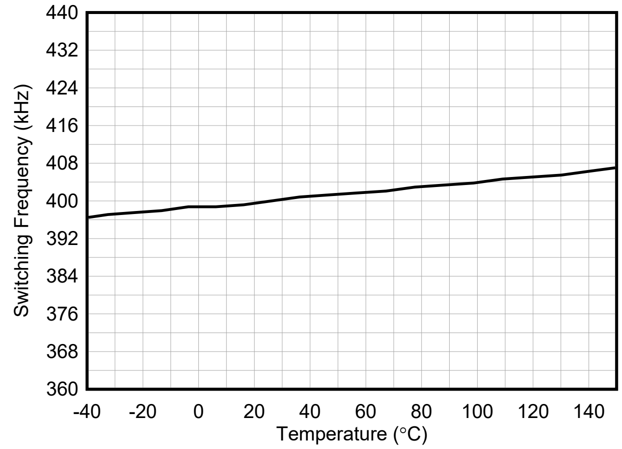

图 **6-3. Switching Frequency Versus Temperature**

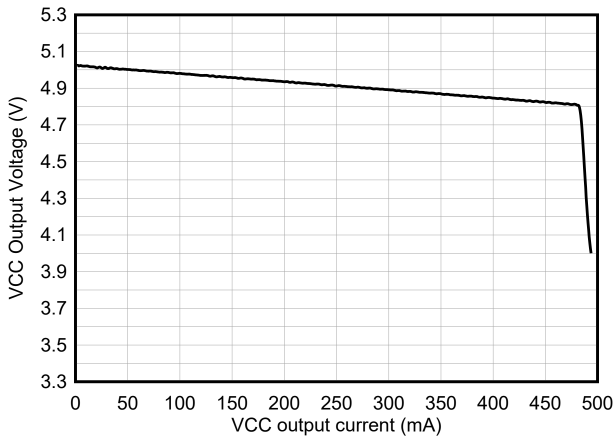

图 **6-4. $V_{(VCC)}$ Versus I_{VCC} Supplied Through BIAS**

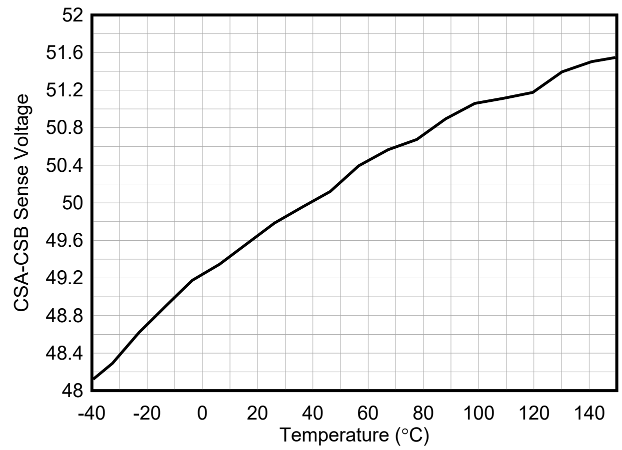

图 **6-5. Current Limit Threshold Versus Temperature**

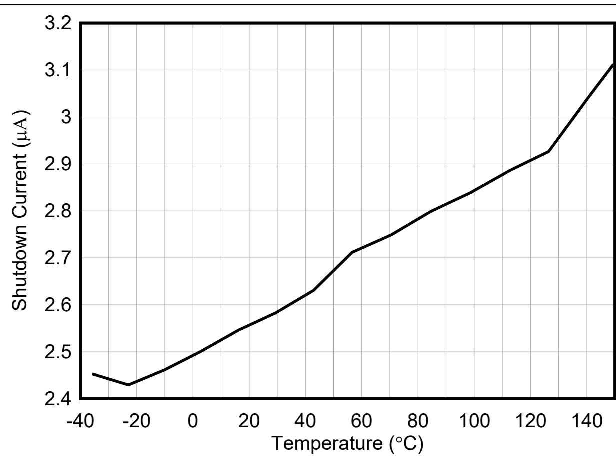

图 **6-6. Shutdown Current in Shutdown Versus Temperature, $V_{(VIN)}$ = 12 V**

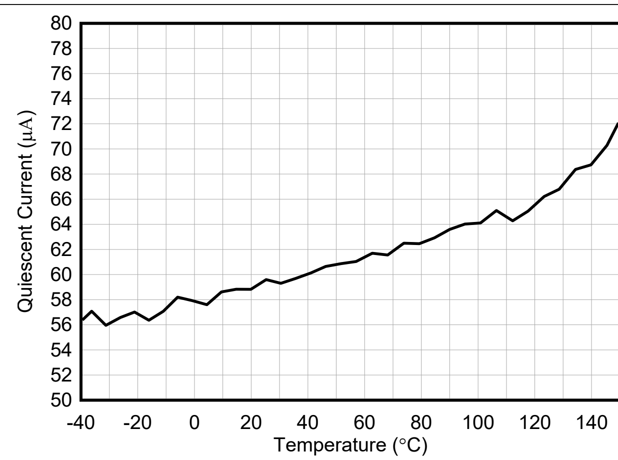

图 **6-7. Quiescent Current Versus Temperature**

6.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC)}$ = 5 V

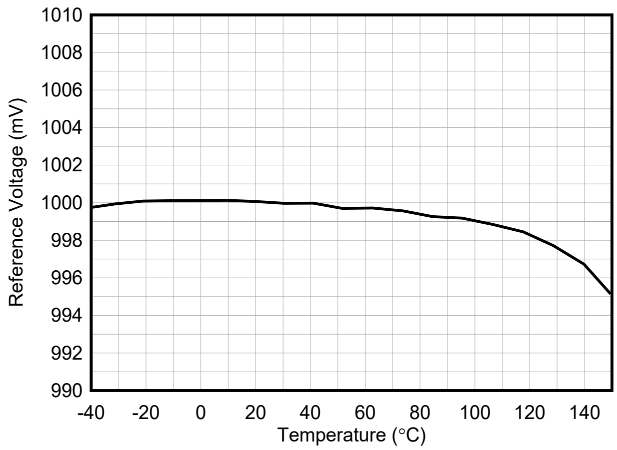

图 6-8. FB Pin Reference Voltage Versus Temperature

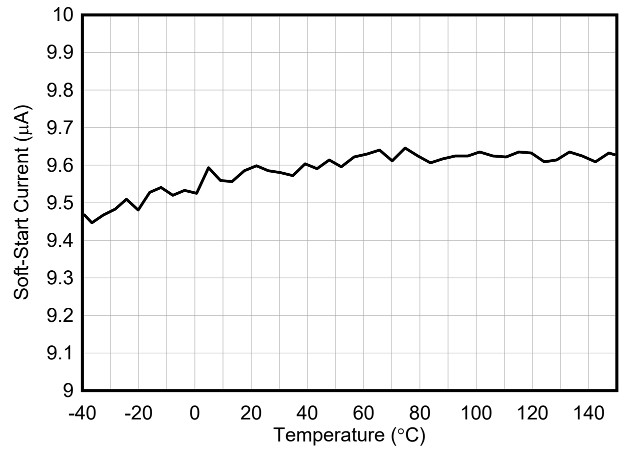

图 6-9. Soft-Start Current Versus Temperature

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7 Parameter Measurement Information

7.1 Gate Driver Rise Time and Fall Time

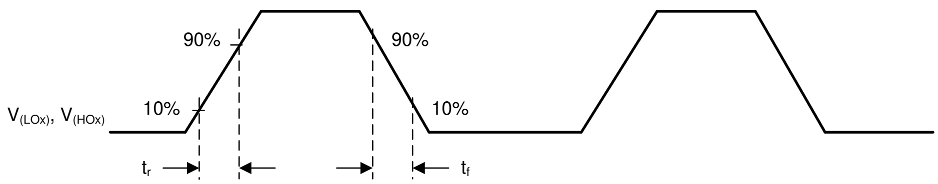

图 7-1. Timing Diagram Gate Driver, t_r, t_f

7.2 Gate Driver Dead (Transition) Time

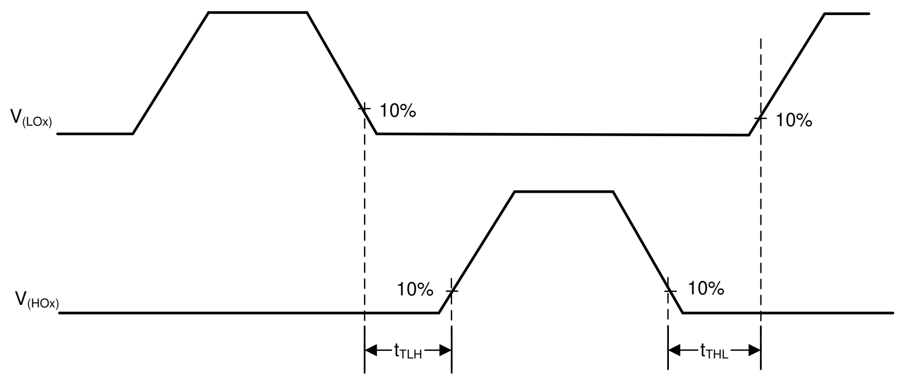

图 7-2. Timing Diagram Gate Driver, t_t

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8 Detailed Description

8.1 Overview

The LM5177 is a four switch buck-boost controller. The device provides a regulated output voltage if the input voltage is higher, equal, or lower than the adjusted output voltage.

In power safe mode, the LM5177 supports superb efficiency over the full rage of the output current. The operation modes are on-the-fly pin-selectable during operation. The proprietary buck-boost modulation scheme also runs at a fixed switching frequency, which can be set through the RT/SYNC pin. The switching frequency remains constant during buck, boost, and buck-boost operation. The device maintains small mode transition ripple over all operating modes. Through the activation of the dual random spread spectrum operation, EMI mitigation is achievable at any time of the design process.

The integrated and optional average current monitor can help monitor and limit input and output current of the LM5177. This feature also supports charging backup power elements, like batteries or capacitors, with constant current (CC) and constant voltage (CV).

The output voltage of the LM5177 can be dynamically adjusted during operation (dynamic voltage scaling and envelope tracking). The adjustment is either possible by changing the analog reference voltage of the SS/ATRK pin or it can be done directly with a PWM input signal on the DTRK pin.

The internal wide input LDOs ensure a robust supply of the device functionality under different input and output voltage conditions. Due to the high drive capability and the automatic and headroom depended voltages selection, the power losses are kept at a minimum at high switching frequency operation. The separate bias pin can be connected to the input, output, or an external supply to further reduce power losses in the device. At all times, the internal supply voltage is monitored to avoid undefined failure handling.

The LM5177 integrates a full bridge N-channel MOSFET driver. The gate driver circuit has a high driving capability to ensure high efficiency targets over the wide range of the supported application. The gate driver features an integrated high voltage low dropout bootstrap diode. The internal bootstrap circuit has a protection against an overvoltage that can be injected by negative spikes and an undervoltage lockout protection to avoid a linear operation of the external power FET. The bootstrap circuit ensures 100% duty cycle operation in pure boost or buck mode.

The resistor-to-digital (R2D) interface offers the user a simple and robust selection of all the device functionality where the analog settings of the soft start minimize the inrush current. Additionally, the control loop and slope compensation ensure a best-in-class output performance for the wide range of supported application cases.

The devices built-in protection features ensure a safe operation under different fault conditions. There is a V_{IN} undervoltage lockout protection to avoid brownout situations. Because the input UVLO threshold and hysteresis can be configured through an external feedback divider, the brownout is avoided under the different designs. The device has an output overvoltage protection and an input overvoltage protection for negative current operation. The selectable hiccup overcurrent protection avoids excessive short circuit currents by using the internal cycle-by-cycle peak current protection. Due to the integrated thermal shutdown, the device is protected against thermal damage caused by an overload condition of the internal VCC regulators. All output-related fault events are monitored and indicated at the open-drain nFLT pin of the device.

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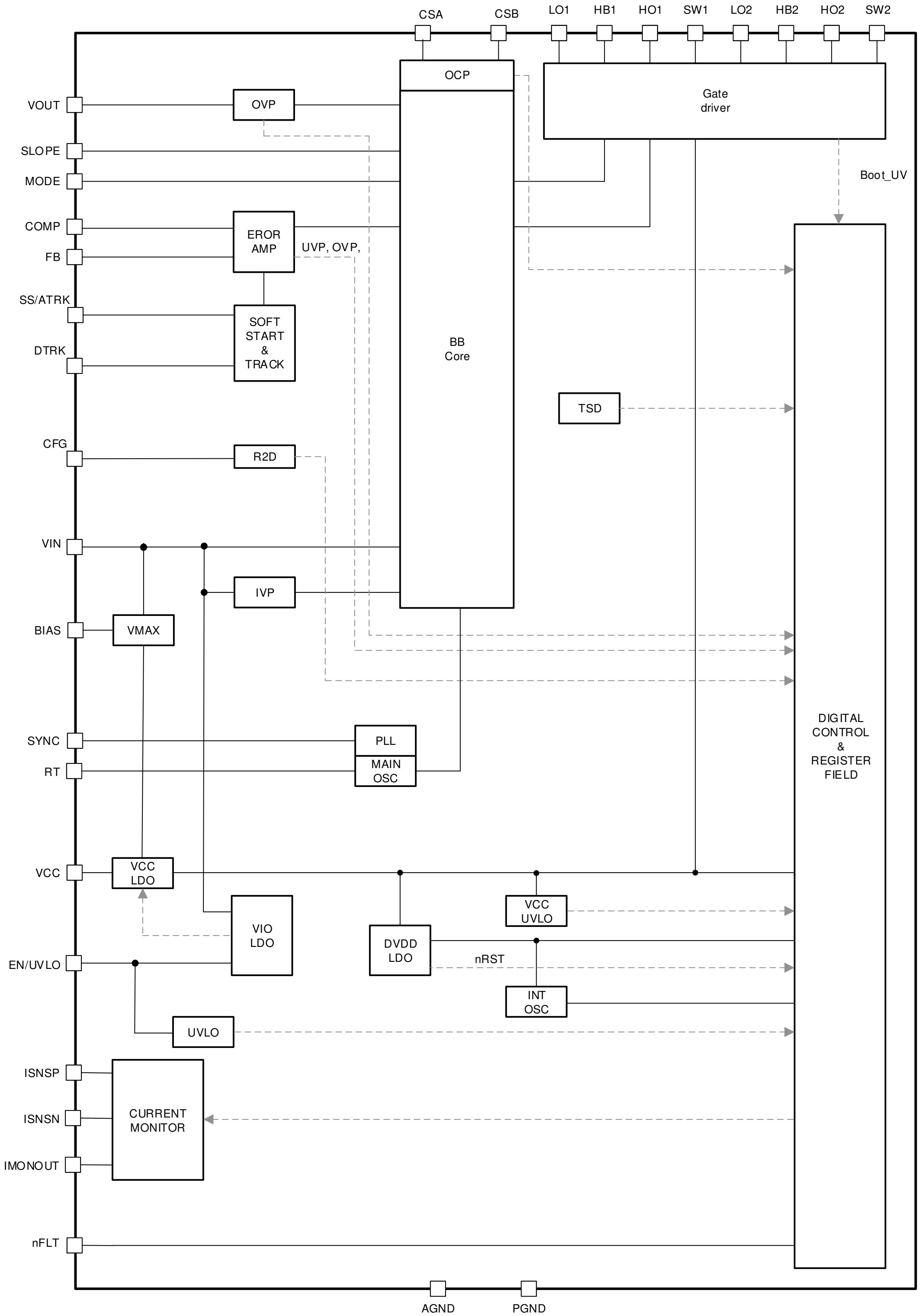
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Buck-Boost Control Scheme

The LM5177 buck-boost control algorithm makes sure there is a seamless transition between the different operation modes, the fixed frequency operation, and the power stage protection features. The internal state machines controls the flowing three active switching states:

State I: Transistor Q1 and Q3 are conducting. Q2 and Q4 are not conducting (boost mode magnetization state).

State II: Transistor Q1 and Q4 are conducting. Q2 and Q3 are not conducting (boost demagnetization or buck magnetization state).

State III: Transistor Q2 and Q4 are conducting. Q1 and Q3 are not conducting (buck demagnetization state).

Switch	State I	State II	State III
Q1	ON	ON	OFF
Q2	OFF	OFF	ON
Q3	ON	OFF	OFF
Q4	OFF	ON	ON

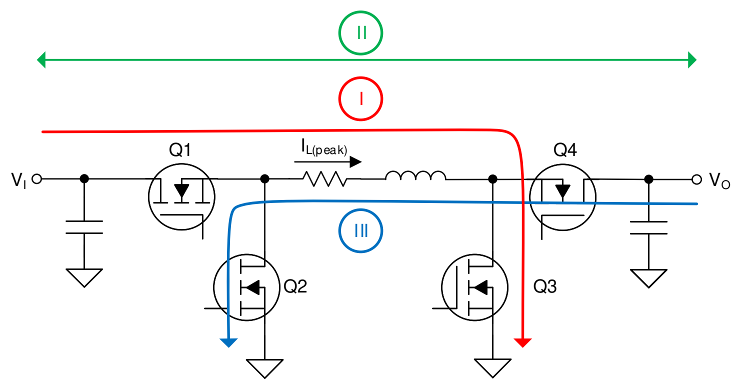


图 8-1. Buck-Boost Active Switching States

8.3.1.1 Boost Mode

In boost mode operation, the converter starts a boost magnetization cycle (switching state I) with the internal clock signal. After it samples the inductor current, the device transitions to switching state II, which is the boost demagnetization state. The maximum duty cycle in boost mode is limited by the minimum boost on time and the selected switching frequency.

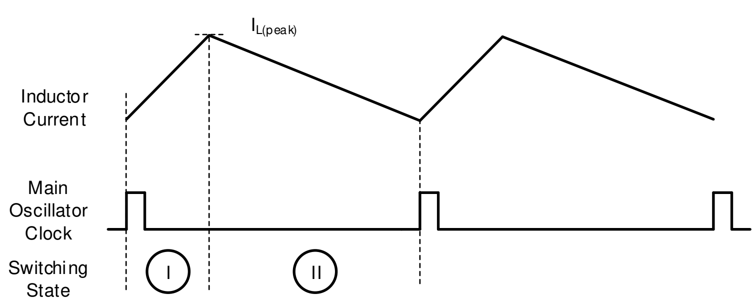


图 8-2. Inductor Current in Continuous Current Boost Operation

8.3.1.2 Buck Mode

In buck mode operation, the converter starts a buck magnetization cycle (state II) with the internal clock signal. When the inductor reaches its peak current, the converter proceeds to the buck demagnetization state III. With the next clock signal, the converter changes back to a buck magnetization cycle and starts a new switching cycle

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with sampling the peak current. As long as the duty cycle does not reach the minimum off time, the current control remains in buck operating mode.

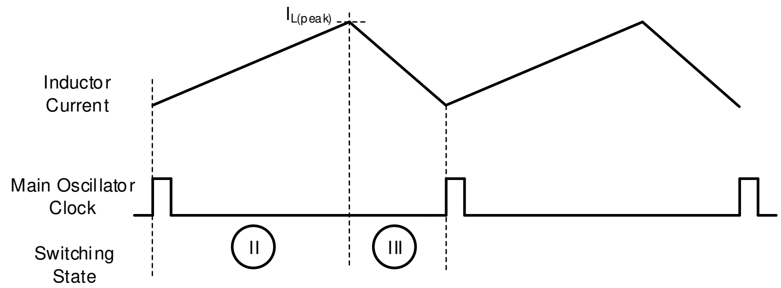

图 8-3. Inductor Current in Continuous Current Boost Operation

8.3.1.3 Buck-Boost Mode

As soon as the on time in buck mode operation exceeds the minimum on time or the off time in boost mode exceeds the minimum off time, the control transits to the buck boost operation. In the continuous current buck-boost mode, the control adds a boost magnetization (state I) switching cycle before the peak current is reached. Therefore, buck-boost operation mode always consists of all three switching cycles state I, state II, and state III. The peak current detection in this mode happens during switching state I.

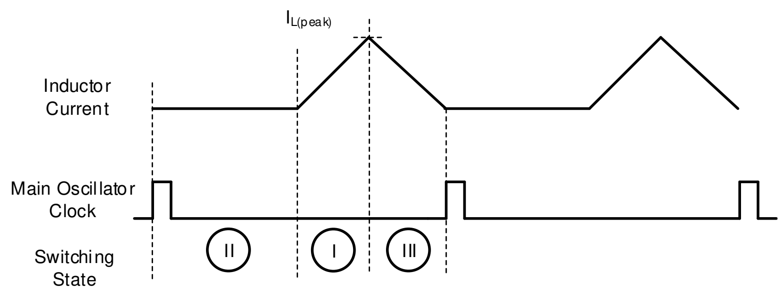

图 8-4. Inductor Current in Continuous Buck-Boost Operation

8.3.2 Power Save Mode

With the MODE pin low, power save mode is active. In this operating mode, the switching activity is reduced and efficiency is maximized. If the mode pin is high, power save mode is disabled. The converter operates in continuous conduction mode.

In boost or in buck mode, the converter is operating up to the duty cycles with the respective minimum off times or on times. If the timing limits are reached, the output voltage increases. As soon as this happens, the voltage regulation loop detects the increase and turns the device into a TI proprietary sleep mode as the energy consumed by the load is less than what the converter generates during switching. In this mode, both low sides are turned on to ensure the high-side gate voltage supply voltage for HB1 and HB2 are charged. Other internal circuits are partially turned off to reduce the current consumption of the converter to a minimum possible. In case the output voltage reaches the nominal output voltage set point, the switching activity starts again.

To avoid subharmonic frequencies due to repetitive entry and exit of the power save operation, the entry point is randomized between the nominal voltage and the maximum entry detection threshold of 1% above the nominal voltage.

In the buck-boost area where larger or smaller duty cycles is necessary, switching pulses are skipped. When necessary, the control initiates switching activities with a minimum time of state I or state III to maintain the inductor current as required by the voltage regulation loop.

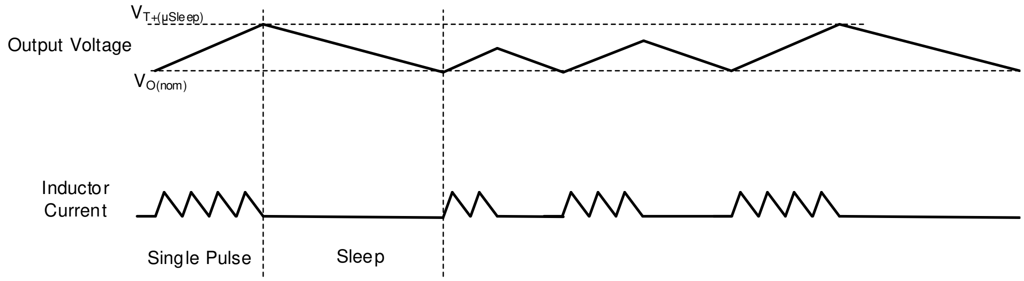

图 8-5. Timing Diagram for the Power Save Mode

8.3.3 Power-On Reset (POR System)

The integrated power-on reset system provides power to all internal functional circuits other than the gate drivers and handles the supervision for the internal logic. The low quiescent current design of this block enables an extremely low shutdown current of the whole system. There is a power ORing between the VIN and BIAS pin for the POR system to ensure LM5177 functionality even under extreme operation conditions, like an output or input short.

Once the voltage on VIN or BIAS rises above the POR threshold, the device logic starts the initialization process and is continuously monitoring the EN/UVLO pin to start the converter operation. To avoid any brownout, the POR system contains a voltage detection (VDET) for the VIN pin. This function additionally supervises the input voltage and ensures the power stage operation is blocked outside.

8.3.4 Supply Voltage Selection – VMAX Switch

There are two pins to supply the LM5177 internal voltage regulators. Due to the internal supply voltage selection circuit, the device can reduce the power dissipation by ensuring a seamless operation at low input or output voltages as well as in transient operating conditions like an output short. The VMAX switch selects the pin with the lower voltage from the VIN or BIAS pin once the voltage on both is above the switch-over threshold ($V_{T(VCC, SUP)}$). If one pin voltage is lower than the threshold, the other supply pin is selected. And if both pins are lower than the switch-over threshold, the higher voltage of VIN or BIAS is selected as supply. The following are common configurations for the supply pins:

- The VIN pin is connected to the supply voltage. The BIAS pin is connected to VO. During start-up, that is as long as the output voltage is not higher than the supply switch-over threshold, the VIN supplies the internal regulators. Once V_O is high enough, the supply current comes from the BIAS pin.
- Both the VIN pin and the BIAS pin are connected together to the input supply voltage. This configuration is often used in applications where the input supply voltage is usually lower or equal than the output voltage. As the BIAS pin is connected to the input voltage, the device has the full current capability of the internal regulators at low input voltages for start-up.
- The VIN is connected to the input supply voltage and the BIAS pin is connected to an auxiliary supply (for example, an existing 12-V DC/DC converter). This configuration is commonly used at high voltage applications on the input and output voltages where the power dissipation over the integrated linear regulators must be further minimized.

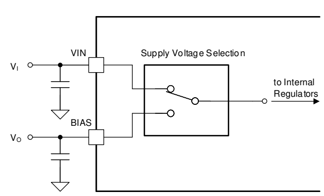

图 8-6. VMAX Supply Scenario 1

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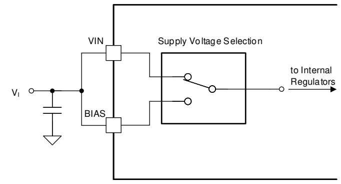

图 8-7. VMAX Supply Scenario 2

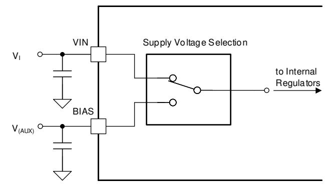

图 8-8. VMAX Supply Scenario 3

8.3.5 Enable and Undervoltage Lockout

The LM5177 has a dual function enable and undervoltage lockout (UVLO) pin. The internal device logic and reference system powers up once the pin voltage is above the $V_{T+(EN)}$ threshold. Once this condition is met, the device is in standby mode. If the EN/UVLO pin voltage is below the $V_{T-(EN)}$ threshold, the device is in shutdown mode to save quiescent current. Find the device operation modes description in 节 8.4.

The UVLO function of the device can detect an low input voltage condition for the power stage to avoid a brownout condition. The detection threshold as well as the required hysteresis are adjustable with an external voltage divider on the EN/UVLO pin.

If the EN/UVLO pin voltage is above the $V_{T+(EN)}$ threshold, the internal current source for the UVLO hysteresis is active. If the EN/UVLO pin voltage is above the $V_{T+(UVLO)}$ threshold, the internal current source for the UVLO hysteresis is off.

The UVLO features an internal delay time ($t_{d(UVLO)}$) for the shutdown to avoid any undesired converter shutdown due to input noise on the UVLO detection pin. The voltage on the EN/UVLO pin must be below the $V_{T-(UVLO)}$ threshold for the delay time, $t_{d(UVLO)}$. Once these conditions are met, the device logic immediately stops the converter operation.

The UVLO threshold is typically set by a resistor divider from VIN to AGND. The effective turn-on threshold is calculated using 方程式 1. The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor and the internal hysteresis current.

$$V_{(VIN,IT+,UVLO)} = V_{IT+(UVLO)} \times \left(1 + \frac{R_{UVLO,top}}{R_{UVLO,bot}}\right) + R_{UVLO,top} \times I_{(UVLO,hyst)} \quad (1)$$

where

- $R_{(UVLO,top)}$ is the upper resistor.
- $R_{(UVLO,bot)}$ is the lower resistor in the divider.

8.3.6 Oscillator Frequency Selection

The LM5177 has a low tolerance internal trimmed oscillator. With the RT pin left open, the oscillator frequency is 75 kHz. With the RT pin grounded, the switching frequency is at the maximum of 2.5 MHz. The oscillator frequency can be programmed up or down by connecting a resistor from the RT pin to ground. To calculate the RT resistor for a specific oscillator frequency, use 方程式 2.

$$R_{(RT)} = \left(\frac{1}{f_{(sw)}} - 20ns\right) \times 30.3\frac{G\Omega}{s} \quad (2)$$

The RT pin is regulated to 0.75 V by an internal voltage source when the device is in active mode. Therefore, the switching frequency can be dynamically changed during operation by changing the current flowing through the resistor. 图 8-9 and 图 8-10 show two examples for changing the frequency by the switching the resistor value or applying a external voltage source through a resistor. It is not recommended to connect any additional capacitance directly to the RT pin.

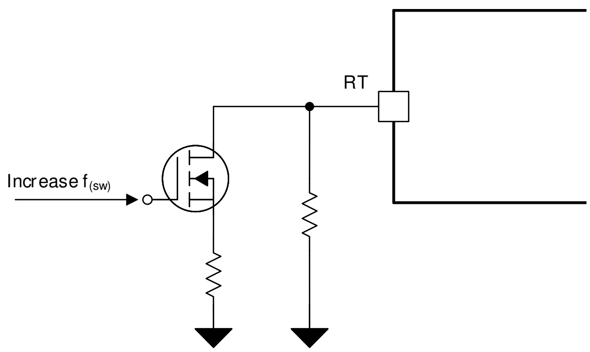

图 8-9. Frequency Hopping Example

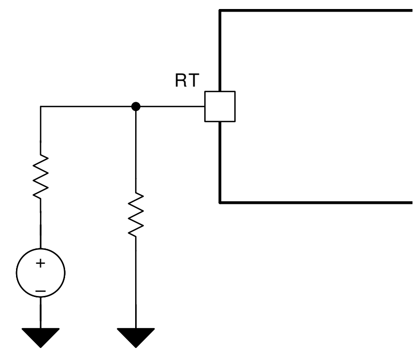

图 8-10. Dynamic Frequency Changing Example

8.3.7 Voltage Regulation Loop

The LM5177 features an internal error amplifier (EA) to regulate the output voltage. The output voltage gets sensed on the FB pin through external resistors, which determine the target or nominal output voltage. The reference for the EA builds the soft-start and analog output voltage tracking pin (SS/ATRK). The COMP pin is the output of the internal gm-stage and gets connected to the external compensation network. The voltage over the compensation network is the nominal value for the inner peak current control loop of the device.

By connecting the FB pin to a voltage higher the internal feedback selection threshold (for example, $V_{(VCC)}$), the device latches this configuration during start-up and operates with a fixed output voltage.

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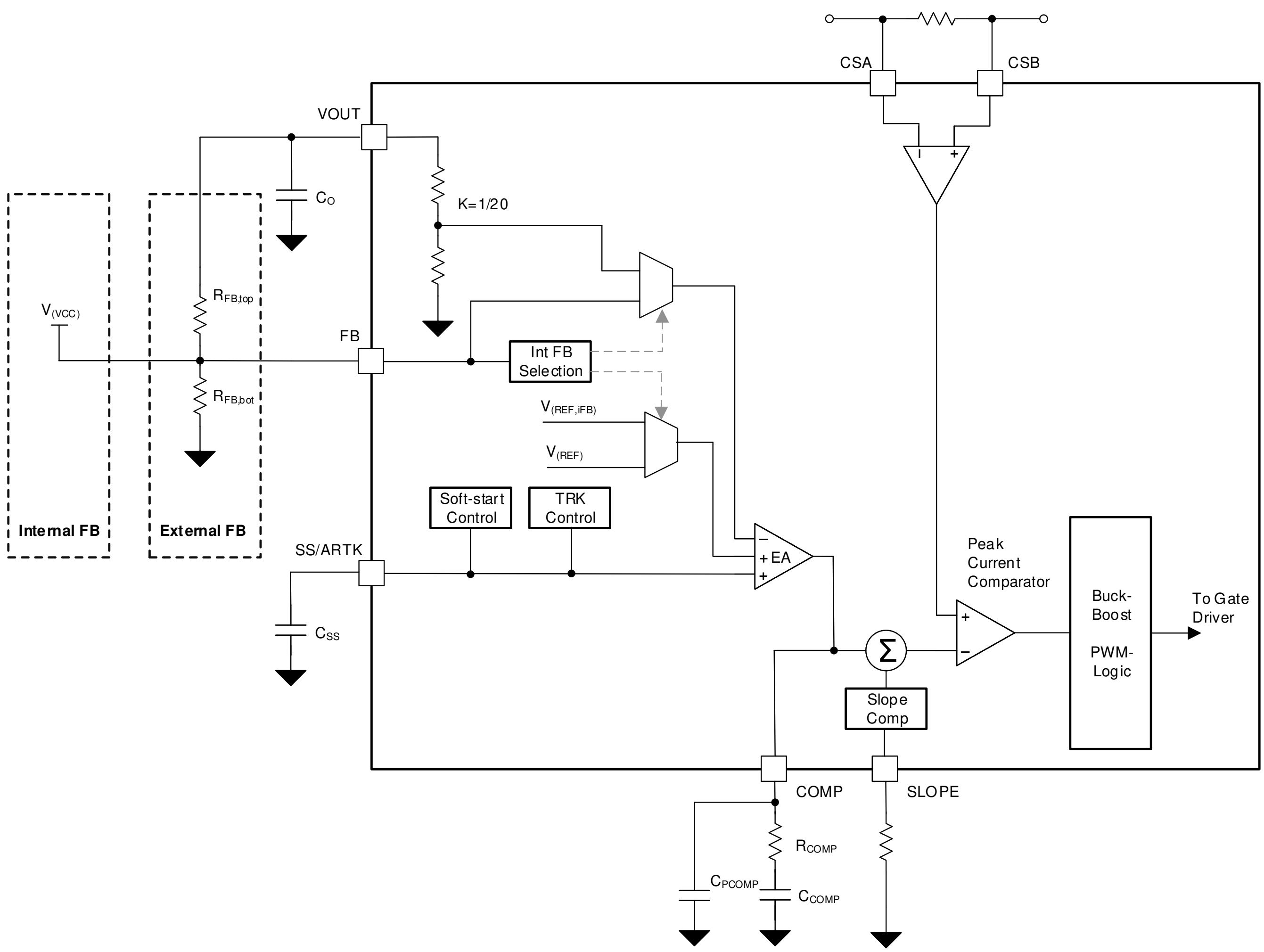

图 8-11. Functional Block Diagram of the Voltage and Peak Current Control Loop

Use the following equations to calculate the external components:

External Feedback:

$$R_{(COMP)} = \frac{2\pi \times f_{(BW)}}{gm_{(ea)}} \times \frac{R_{(FB,bot)} + R_{(FB,top)}}{R_{(FB,bot)}} \times \frac{10 \times R_{(SNS1)} \times C_O}{1 - d_{max}} \tag{3}$$

Internal Feedback:

$$R_{(COMP)} = \frac{2\pi \times f_{(BW)}}{gm_{(ea)}} \times 20 \times \frac{10 \times R_{(SNS1)} \times C_O}{1 - d_{max}} \tag{4}$$

Common for Internal and External Feedback:

$$C_{(COMP)} = \frac{1}{2\pi \times f_{(CZ)} \times R_{(COMP)}} \tag{5}$$

$$C_{(PCOMP)} = \frac{1}{2\pi \times 10 \times f_{(BW)} \times R_{(COMP)}} \tag{6}$$

For most applications, TI recommends the following guidelines for bandwidth selection of the compensation. The hard limit of the bandwidth ($f_{(BW)}$) is the right half plane zero of the boost operation:

$$f_{RHPZ} = \frac{1}{2\pi} \times \frac{V(VOUT) \times \left(1 - d_{max}\right)^2}{I_{o,max} \times L} \tag{7}$$

The maximum recommended bandwidth must be within the following boundaries:

$$f_{(BW)} < \frac{1}{3} \times f_{RHPZ} \tag{8}$$

$$f_{(BW)} < \frac{1}{10} \times \left(1 - d_{max}\right) \times f_{(SW)} \tag{9}$$

The compensation zero (f_{CZ}) must be places in relation to the dominating pole of the boost.

$$f_{CZ} = 1.5 \times f_{pole,boost} \tag{10}$$

$$f_{pole,boost} = \frac{1}{2\pi} \times \frac{2 \times I_{o,max}}{V(VOUT) \times C_O} \tag{11}$$

Due to the precise implementation of the error amplifier, the voltage on the LM5177 COMP pin is accurately reflecting the nominal peak current value of the inductor. 图 8-12 shows the control V/I-characteristics of error amplifier in FPWM mode. Use this as a guidance for applicative designs where you need to manipulate the inner current loop regulation.

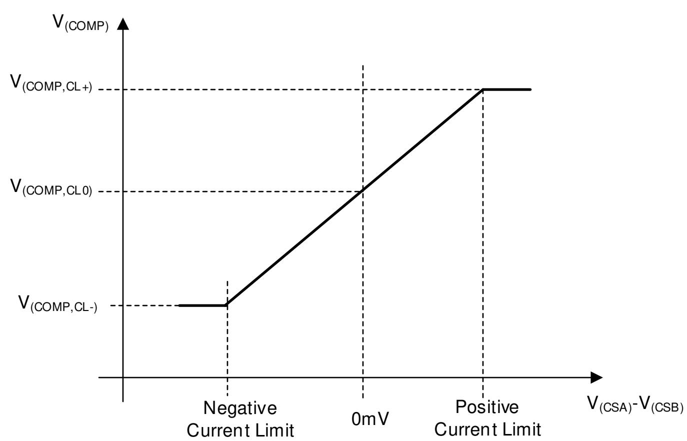

图 8-12. Control Function for the Peak Current Sense Voltage Versus V_{COMP}

8.3.8 Output Voltage Tracking

There are two kinds of output voltage tracking features integrated in the device.

- Analog voltage tracking function through the SS/ATRK pin
- Digital voltage tracking function through the DTRK pin

Analog Voltage Tracking

For the analog output voltage tracking, an external applied voltage overwrites the reference voltage for the output regulation loop. Although it is possible, it is not recommend to apply this voltage before the soft start is finished because the soft-start ramp time and, therefore, the input current during the start-up is changed.

As the internal error amplifier is designed to use the lowest reference input voltage, the applied voltage on the SS/ATRK pin is only effective for voltages lower than the V_{ref} of the feedback pin. Hence, the maximum voltage for the output is determined by the resistor network on the FB pin.

Digital Voltage Tracking

The DTRK input of the LM5177 directly modulates the internal reference voltage. This function activates if the voltage on the DTRK pin is higher than the rising threshold of $V_{T(DTRK)}$ and a PWM signal in the recommended frequency is applied to the pin.

The maximum output voltage during digital tracking cannot exceed the nominal reference voltage for the FB resistor divider. The applied PWM signal reduces the internal reference voltage in relation with the duty cycle on the DTRK pin. A small duty cycle means less output voltage and a high duty cycle of the PWM input represents a high output voltage. For example, a duty cycle of 30% causes a output voltage of 30% of the selected voltage by the FB divider resistors.

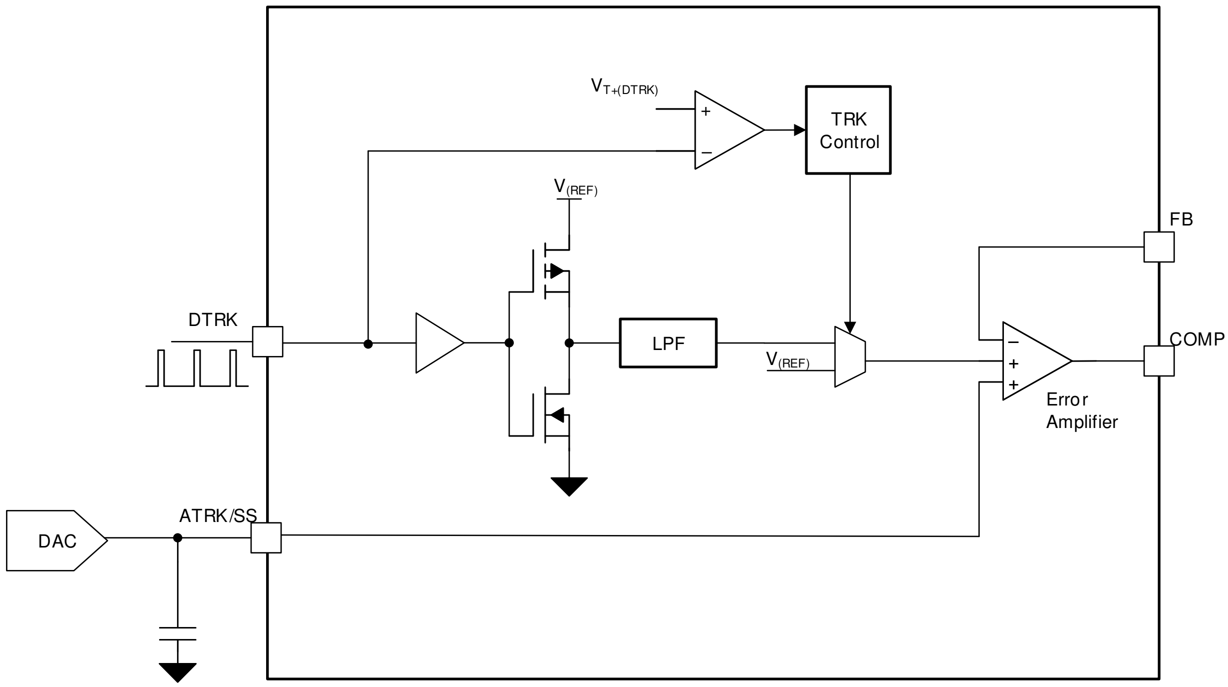

图 8-13. Output Voltage Tracking Functional Block Diagram

8.3.9 Slope Compensation

The LM5177 provides a slope compensation pin to ensure stable operation and the best transient performance over a wide operating range. According to peak current mode control theory, slope compensation is required at operation with duty cycle greater than 50%. The value for the resistor on the SLOPE pin is calculated with 方程式 12.

$$R_{(SLOPE)} = \frac{L}{R_{(SNS1)}} \times 50 \times 10^6 \frac{V}{As} \tag{12}$$

During the design process, consider the following guidelines for the slope compensation:

1. The quotient of peak current sense resistor, $R_{(SNS1)}$, and the main inductor, L, need to be smaller than the factor given by 方程式 13.

$$\frac{R_{(SNS1)}}{L} < \frac{1V \times f_{(sw)}}{V_O \times 10} \tag{13}$$

where

- V_O is the maximum output voltage of a system with dynamic voltage changes.

2. The quotient is within the limits given by 方程式 14.

$$100\ Hz < \frac{R_{(SNS1)}}{L} < 8000\ Hz \tag{14}$$

8.3.10 Configurable Soft Start

The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

The LM5177 features an adjustable soft start that determines the charging time of the output or outputs. The soft-start feature limits inrush current as a result of high output capacitance to avoid an overcurrent condition.

At the beginning of the soft-start sequence, the SS voltage is 0 V. If the SS pin voltage is below the feedback reference voltage, V_{REF}, the soft-start pin controls the regulated FB voltage and the internal soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the output voltage and FB pin. Once the voltage on the SS exceeds the internal reference voltage, the soft-start interval is complete and the error amplifier is referenced to $V_{(REF)}$.

The soft-start time ($t_{(ss)}$) is given by:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{Ref}} \tag{15}$$

The soft-start capacitor is internally discharged when the converter is disabled because of the following:

- EN/UVLO falling below the operating threshold
- VCC falling below the VCC UV threshold
- The device is in hiccup mode current limiting.
- The device is in thermal shutdown.

8.3.11 Current Monitoring and Current Limit Control Loop

The LM5177 features two high voltage current sensors. The first one maintains the peak current sensing between the CSA and CSB pins. The second current sensor inputs are connected to the ISNSP and ISNSN pins.

This optional current sensing provides the capability to monitor or to limit either the input or the output current of the DC/DC converter If the optional current sense amplifier is not used, the user can disable it to reduce the bias current consumption of the whole device by connecting the IMONOUT pin to VCC. Do not do this dynamical during the operation of the device because the configuration gets latched at start-up of the converter. Use the CFG pin to select one of the following desired operation modes.

Current Monitor Operation:

In case the current sense amplifier is configured as a monitor, the output voltage on the IMONOUT pin is a linear relation between the sense voltage between ISNSP and ISNSP pins and the IMON sense amplifier transcendence and the resistor placed on the IMONOUT pin.

$$V_{(IMONOUT)} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm \times R_{(IMONOUT)} \tag{16}$$

The output voltage of the IMONOUT pin is clamped to the values given in 节 6.5.

If the user intends to reduce the bandwidth of the current monitor, the user can place an optional capacitor in parallel to the IMONOUT pin like it is indicated in 图 8-14.

Current Limit Operation:

In this configuration, the current sense gm amplifier monitors the voltage across the sense resistor and compares it with an internal reference voltage. If the drop across the sense resistor is greater than the reference threshold the gm amplifier gradually reduces the peak current capability of the DC/DC converter until the differential voltage is equal the reference voltage. This function of the LM5177 can be used to do the following:

- Regulate the current into the load from the power stage
- Regulate the current from the output into the power stage
- Regulated the current from the input supply to the power stage
- Regulated the current into the device input from the power stage

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To select a negative current limit direction, the SYNC pin needs to be pulled low for the time when EN/UVLO goes above the EN rising threshold until the soft-start ramp starts the converter operation. The configuration gets latched and the SYNC pin can be used for the synchronization afterward. If the synchronization function is not used it can be pulled low continuously. For a positive current limit protection the SYNC pin can be pulled high or connected to a valid synchronization signal during the time when EN/UVLO goes above the EN rising threshold until the soft-start ramp starts the converter operation

Once the current limit operation mode is selected, a RC compensation network must be placed on the IMONOUT pin. For most applications, a compensation bandwidth with a factor of 3× to 5× faster than the compensation of the output voltage loop has given good results.

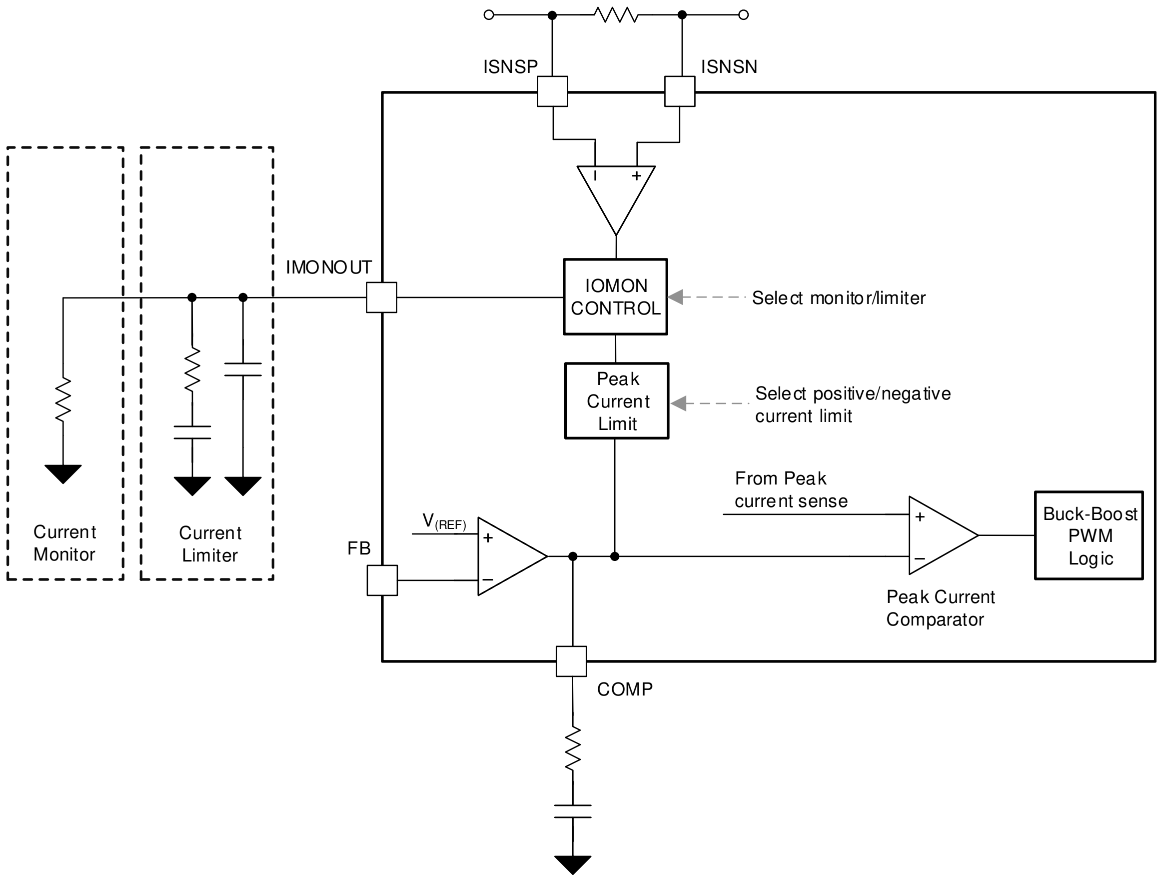

图 8-14. Current Monitor Functional Block Diagram

8.3.12 Device Configuration Pin

The resistor selection on the CFG pin is read and latched during the power-up sequence of the device. The selection cannot be changed until the voltage on the EN or UVLO reaches the falling threshold or VCC voltage drops below the $V_{CCT\text{-}(UVLO)}$ threshold. 表 8-1 shows the possible device configurations versus the different resistor values on the CFG pin.

表 8-1. CFG Pin Configuration Overview

#	$R_{(CFG)}$ / kΩ	DRSS	SCP – Hiccup Mode	µ SLEEP	Current Limit
1	0	DISABLED	DISABLED	DISABLED	DISABLED
2	0.511	ENABLED	DISABLED		
3	1.3	DISABLED	ENABLED		
4	1.9	ENABLED	ENABLED		

表 8-1. CFG Pin Configuration Overview (continued)

#	$R_{(CFG)}$ / kΩ	DRSS	SCP – Hiccup Mode	μ SLEEP	Current Limit
5	2.7	DISABLED	DISABLED	DISABLED	ENABLED
6	3.8	ENABLED	DISABLED		
7	5.1	DISABLED	ENABLED		
8	6.5	ENABLED	ENABLED		
9	8.3	DISABLED	DISABLED	ENABLED	DISABLED
10	10.5	ENABLED	DISABLED		
11	13.3	DISABLED	ENABLED		
12	16.2	ENABLED	ENABLED		
13	20.5	DISABLED	DISABLED	ENABLED	ENABLED
14	24.9	ENABLED	DISABLED		
15	30.1	DISABLED	ENABLED		
16	36.5	ENABLED	ENABLED		

8.3.13 Dual Random Spread Spectrum – DRSS

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. This function is enabled by the CFG pin. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When an external synchronization clock is applied to the SYNC pin, the internal spread spectrum is disabled. DRSS combines a low frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in lower radio frequency bands (for example, AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example, FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

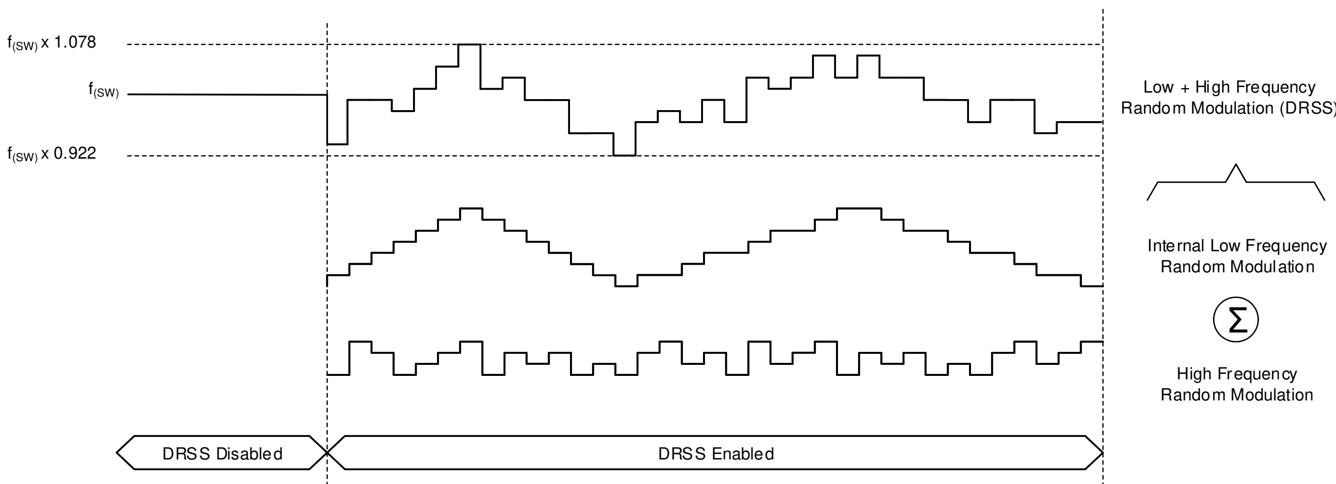

图 8-15. Dual Random Spread Spectrum

8.3.14 Gate Driver

The LM5177 features four internal logic-level nMOS gate drivers. The drivers maintain the high frequency switching of both half bridges needed for a buck-boost operation. If the device is in boost or buck mode, the other half bridge high-side switch needs to be permanent. The internal gate drivers support this by sharing the current from the other half bridge, which is switching. Therefore, a minimum of quiescent current can be assured as no additional char pump is needed. Due to the high drive current, it can support a wide range of external power FETs as well as a parallel operation of them.

The LO and HO outputs are protected with a shoot-through protection, which ensures that both outputs are not turned on at the same time. If the PWM modulation logic of the buck-boost turns the LOx pin off, the HOx pin is not turned on until the following are true:

1. A minimum internal transition time ($t_{t(dead)}$) is reached.
2. The voltage on the LOx pin drops below the detection threshold $V_{TH(GATEOUT)}$.

This behavior is maintained and vice versa if the HOx pin turns off first.

The high-side supply voltage for the gate driver are monitored by an additional bootstrap UVLO comparator. This comparator monitors the differential voltage between SWx and HBx. If the voltage drops below the threshold the buck-boost converter operation turns off. The device restarts automatically once the positive going threshold is reached with the a soft-start scheme.

Additionally, the LM5177 monitors to the upper voltage between SWx and HBx. If this voltage exceeds the threshold voltage of the clamping circuit, it activates a internal current source to pull the voltage down.

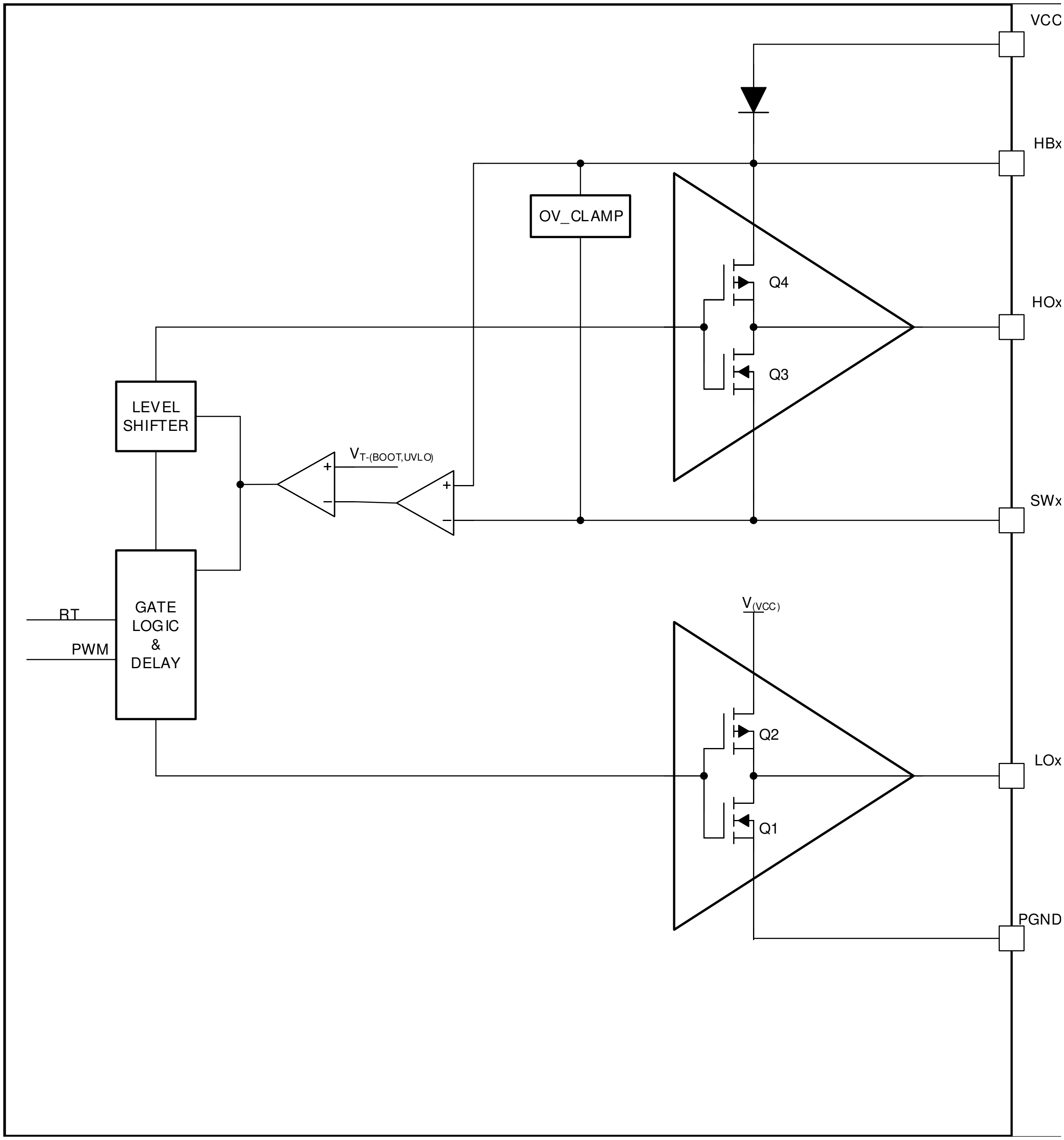

图 8-16. Functional Block Diagram Gate Driver

External Gate Driver Support

The LM5177 supports external gate driver by the HOx_LL pins. These pins provide the two high-side gate drive signals referenced to ground. By connecting the HOx_LL and LOx signals to a external gate driver the external power FETs can be controlled by the external gate driver. This feature for example is helpful in case no logic level FET is available and the application need to drive gate voltages higher the one the integrated gate drive supports.

The external bootstrap capacitors on HBx still needs to be placed in the schematic as the internal current sense amplifier is still supplied trough this pins. The HOx pin can be left floating. Make sure the supply voltage $V_{(extGD)}$

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for each external gate driver maintains the necessary requirements for a 4-switch Buck-Boost such as 100% duty cycle and the isolation between each side of the full-bridge. Below Simplified Schematic External Gate Driver support show a functional block diagram of the

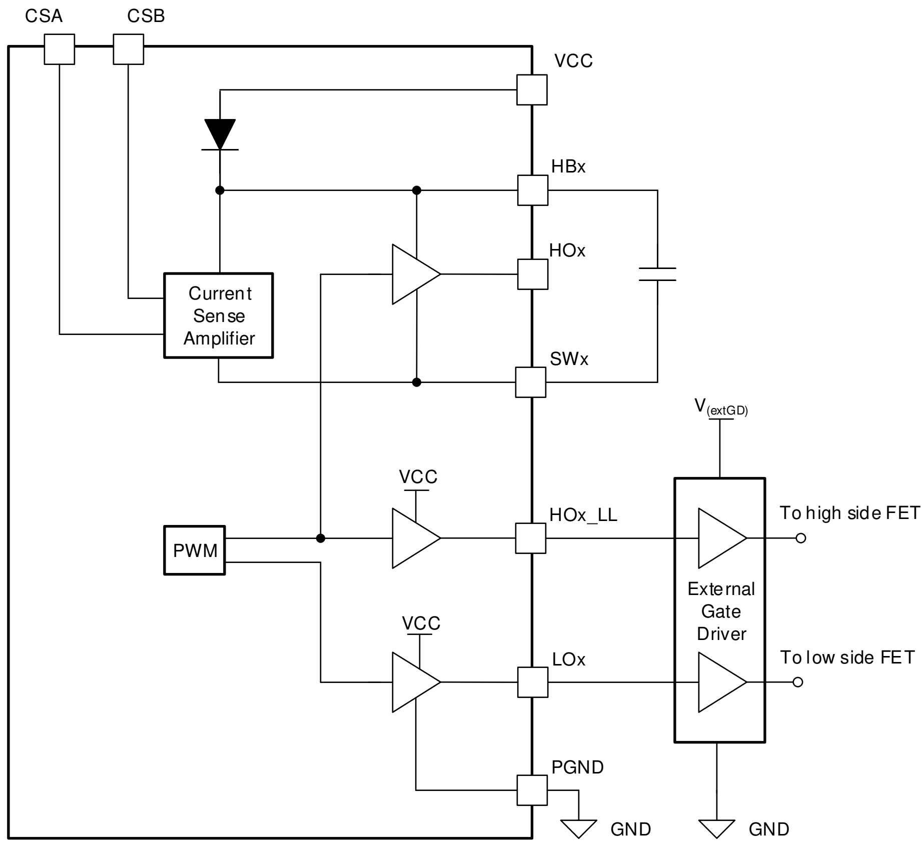

图 8-17. Simplified Schematic External Gate Driver support

8.3.15 Frequency Synchronization

The device features an internal phase looked loop (PLL), which is designed to transition the switching frequency seamlessly between the frequency set by the RT pin and the external frequency synchronization signal. If no external frequency is provided, the RT pin sets the center frequency of the PLL. The external synchronization signal can change the switching frequency ±50%. To ensure low quiescence current, the input buffer of the SYNC pin is disabled if no valid sync frequency, that is a frequency signal outside the recommended synchronization range is applied.

The $f_{(SW)}$ synchronization stops if the device enters power save mode or µSleep operation, if enabled. Once the converter enters the PWM operation again, the device re-syncs to a pin signal. The synchronization timings are given in 图 8-19.

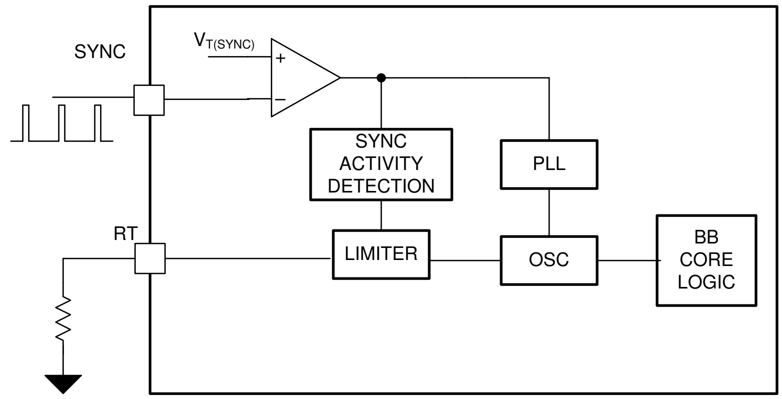

图 8-18. Main Oscillator Functional Block Diagram

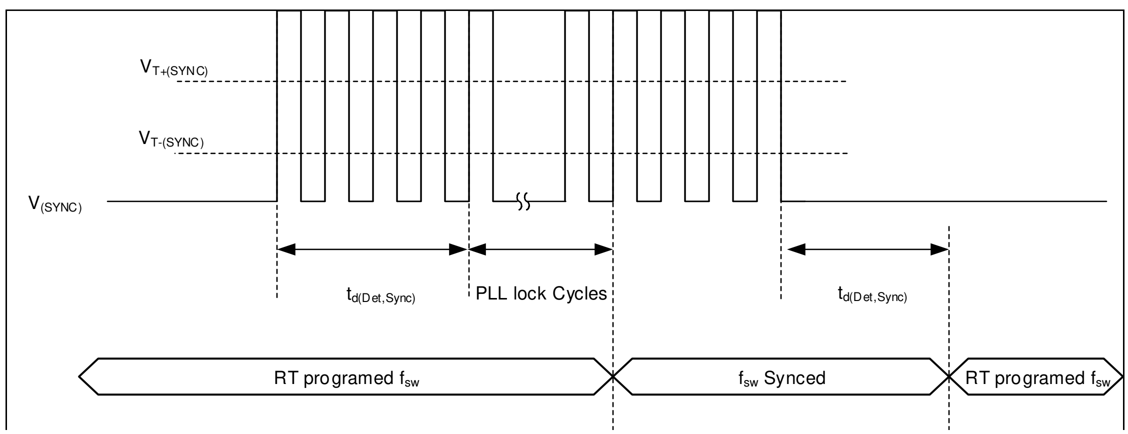

图 8-19. Timing Diagram SYNC Function

The sync pin has a dual function to configure the current limit direction.

8.4 Device Functional Modes

图 8-20 describes the functional behavior of the internal device logic.

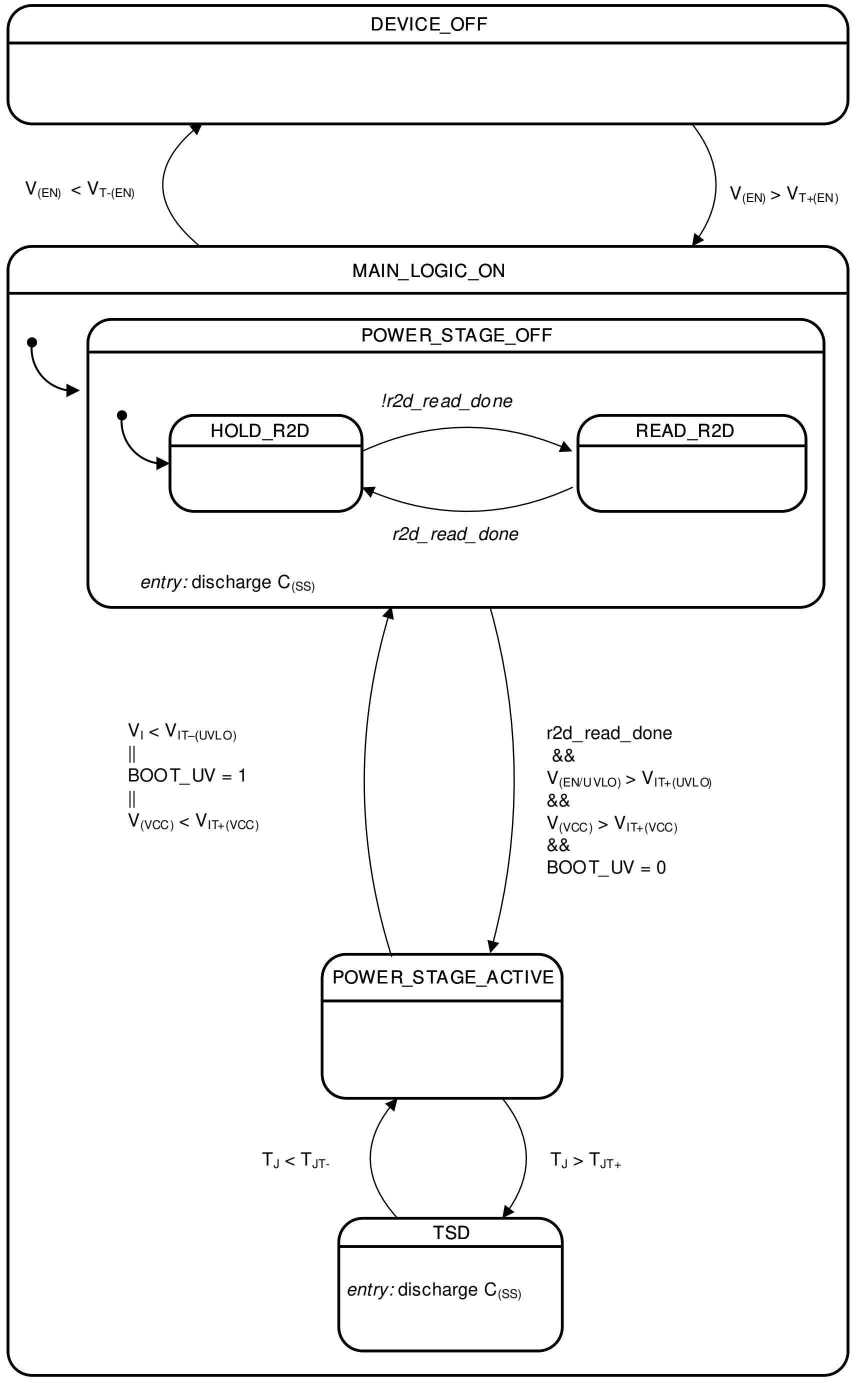

图 8-20. Functional State Diagram

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LM5177 is a wide input voltage, synchronous, non-inverting buck-boost controller, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage. To expedite and streamline the process of designing the external circuits and select the components, a comprehensive quickstart calculator is available for download to assist the designer with component selection for a given application.

9.2 Typical Application

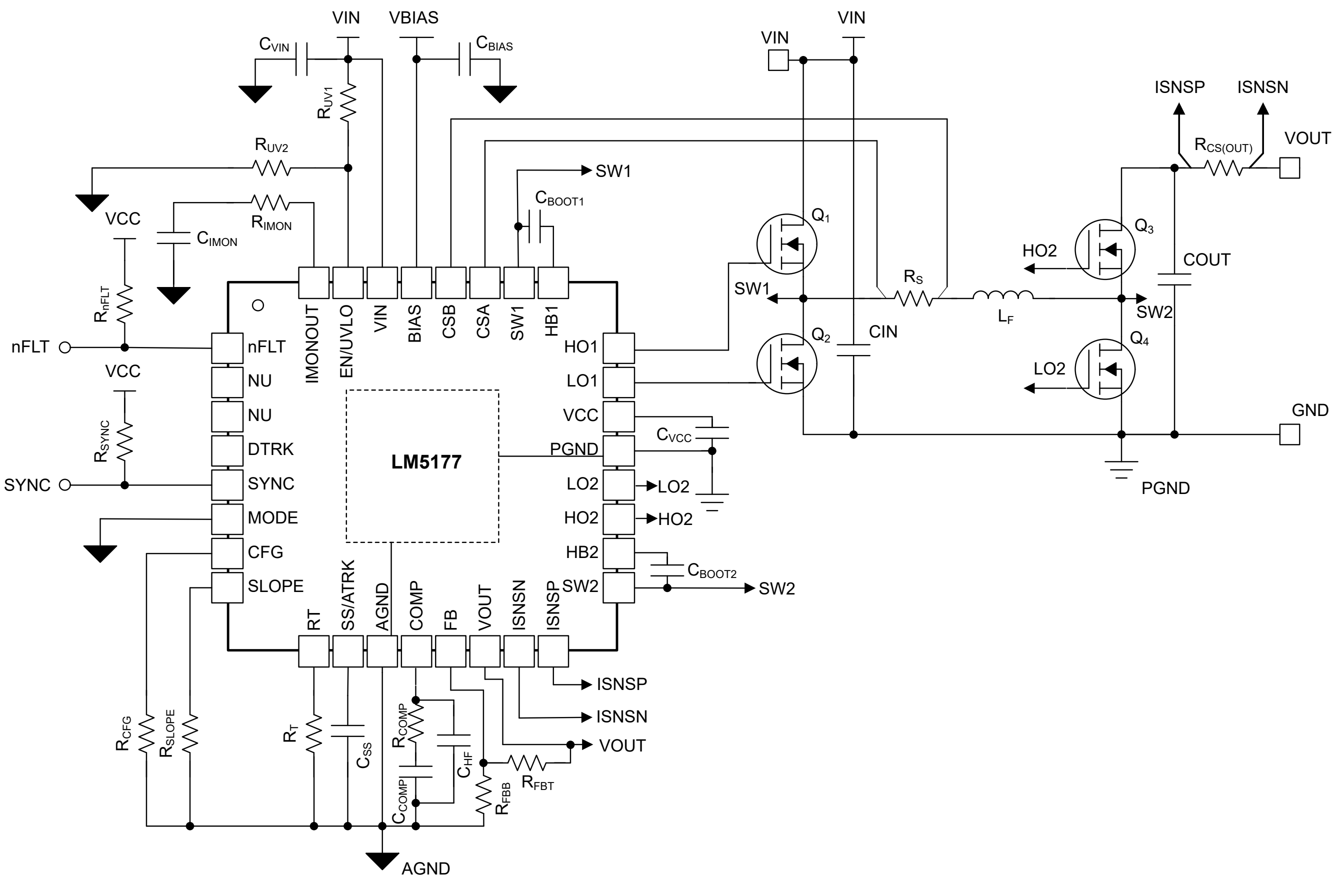

图 9-1. Simplified Schematic of a Typical Application

9.2.1 Design Requirements

表 9-1 shows the intended input, output, and performance parameters for a typical design example.

表 9-1. Design Parameters

Parameter	Value
V_I minimum	4 V
V_I typical = V_I start-up	13.5 V
V_I maximum	36 V

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表 9-1. Design Parameters (continued)

Parameter	Value
V_O nominal	16 V
P_O maximum	150 W

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM5177 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

9.2.2.2 Frequency

The switching frequency of LM5177 is set by an R_T resistor connected from the RT/SYNC pin to AGND. The R_T resistor required to set the desired frequency is calculated using 方程式 17 or 图 6-3. A 1% standard resistor of 78.7 kΩ is selected for f_{SW} = 400 kHz.

$$R_{(RT)} = \left(\frac{1}{f_{sw}} - 20\text{ns}\right) \times 30.3\ \frac{\text{G}\Omega}{\text{s}} \tag{17}$$

9.2.2.3 Feedback Divider

The feedback voltage divider is found with 方程式 18:

$$R_{FB,top} = \left(V_{(VOUT)} - V_{(REF)}\right) \times R_{FB,bot} \tag{18}$$

For the 16-V output, an upper resistor of 71.5 kΩ and a lower resistor of 4.7 kΩ have been selected.

表 9-2 shows an overview of a possible selection for the feedback divider resistors over common output voltages.

表 9-2. FB Pin Resistor Divider Examples with $R_{FB,bot}$ = 5.62 kΩ

V_O – Target	$R_{FB,top}$ – Calculation	$R_{FB,top}$ – E48 Series	V_O Nominal	Error from FB Resistor
5 V	22.5 kΩ	22.6 kΩ	5.02 V	0.4%
9 V	45 kΩ	44.2 kΩ	8.86 V	– 1.5%
12 V	61.8 kΩ	61.9 kΩ	12.01 V	0.1%
16 V	84.3 kΩ	86.6 kΩ	16.41 V	2.5%
24 V	129.3 kΩ	127 kΩ	23.6 V	– 1.7%
28 V	151.7 kΩ	154 kΩ	28.4 V	1.4%
36 V	196.7 kΩ	196 kΩ	35.88 V	– 0.3%
42 V	230.4 kΩ	226 kΩ	41.21 V	– 1.9%
48 V	264.1 kΩ	261 kΩ	47.44 V	– 1.2%
60 V	331.6 kΩ	332 kΩ	60.07 V	0.1%

9.2.2.4 Inductor Selection

The inductor selection is based on consideration of both buck and boost modes of operation. For buck mode, inductor selection is based on limiting the peak-to-peak current ripple, ΔI_L, to approximately 40% of the maximum inductor current at the maximum input voltage. The target inductance for buck mode is:

$$L_{BUCK} = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \times V_{OUT}}{0.4 \times I_{OUT(MAX)} \times f_{SW} \times V_{IN(MAX)}} = 5.91\ \mu H \tag{19}$$

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple, ΔI_L, to approximately 30% of the maximum inductor current at the minimum input voltage. The target inductance for boost mode is:

$$L_{BOOST} = \frac{V_{IN(MIN)}^2 \times \left(V_{OUT} - V_{IN(MIN)}\right)}{0.3 \times I_{OUT(MAX)} \times f_{SW} \times V_{OUT}^2} = 0.665\ \mu H \tag{20}$$

For this application, an inductor with 3.3 µH was selected.

The peak inductor current occurs at minimum input voltage and is given by:

$$I_{L(PEAK)} = I_{L(MAX)} + \frac{V_{IN(MIN)} \times \left(V_{OUT} - V_{IN(MIN)}\right)}{2 \times L \times f_{SW} \times V_{OUT}} = 38.74\ A \tag{21}$$

To ensure sufficient output current, the current limit threshold must be set to allow the maximum load current in boost operation. The inductor peak current during overload depends on the current limit resistor, R_{SENSE} (refer to the subsection on selecting R_{SENSE}). The peak inductor current in current limit when in boost mode is given by:

$$I_{L(PEAK,\ ILIMIT,\ BOOST)} = \frac{50mV}{R_{SENSE}} = 37.6\ A \tag{22}$$

The peak inductor current in current limit when in buck mode happens at high input voltage and is given by:

$$I_{L(PEAK,\ ILIMIT,\ BUCK)} = \frac{50mV}{R_{SENSE}} + \frac{V_{IN(MAX)} - V_{OUT}}{L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} = 44.33\ A \tag{23}$$

The peak inductor current in current limit is 37.6 A and 44.33 A in boost mode and buck mode, respectively. The inductor must be selected to handle this current.

9.2.2.5 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by 方程式 24 where the minimum V_{IN} corresponds to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \tag{24}$$

In this example, the maximum output ripple RMS current is $I_{COUT(RMS)}$ = 16.3 A. A 2-mΩ output capacitor ESR causes an output ripple voltage of 75 mV as given by:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(MIN)}} \times ESR \tag{25}$$

A 130-µF output capacitor causes a capacitive ripple voltage of 136 mV as given by:

$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \tag{26}$$

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Typically, a combination of ceramic and bulk capacitors is needed to provide low ESR and high ripple current capacity. 图 9-1 shows a good starting point for C_{OUT} for typical applications.

9.2.2.6 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)} \tag{27}$$

The maximum RMS current occurs at D = 0.5, which gives $I_{CIN(RMS)} = I_{OUT} / 2 = 4.7$ A. A combination of ceramic and bulk capacitors must be used to provide a short path for high di/dt current and to reduce the output voltage ripple. 图 9-1 is a good starting point for C_{IN} for typical applications.

9.2.2.7 Main Current Sensor

The current sense resistor between the CS and CSG pins must be selected to ensure that current limit is set high enough for both buck and boost modes of operation. The current limit resistor is given by:

$$I_{CL} = \frac{V_{(VOUT,\,max)}}{V_{(VIN,\,min)}} \times 1.43 \times I_o \tag{28}$$

$$R_{SNS1} = \frac{50\ mV}{I_{CL}} \tag{29}$$

The closest standard value of R_{SENSE} = 1.33 mΩ is selected based on the boost mode operation.

The maximum power dissipation in R_{SENSE} happens at $V_{IN(MIN)}$:

$$P_{R_{SENSE(MAX)}} = \left(\frac{50\ mV}{R_{SENSE}}\right)^2 \times R_{SENSE} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right) = 1.41\ W \tag{30}$$

Therefore, a sense resistor with 2-W power rating is sufficient for this application.

For some application circuits, it can be required to add a filter network to attenuate noise in the CS and CSG sense lines. The filter resistance must not exceed 100 Ω.

9.2.2.8 Slope Compensation

For stable current loop operation and to avoid subharmonic oscillations, the slope resistor must be selected based on 方程式 31:

$$R_{SLOPE} = \frac{L_1}{R_{SNS1}} \times 50\ \frac{MV}{As} \tag{31}$$

This slope compensation results in “dead-beat” operation, in which the current loop disturbances die out in one switching cycle. Theoretically, a current mode loop is stable with half the “dead-beat” slope (considered already in the calculated slope resistor value in 方程式 31). A smaller slope capacitor results in larger slope signal, which is better for noise immunity in the transition region (V_{IN} is approximately equal to V_{OUT}). A larger slope signal, however, restricts the achievable input voltage range for a given output voltage, switching frequency, and inductor. For this design, R_{SLOPE} = 137 kΩ is selected for better transition region behavior while still providing the required V_{IN} range. This selection of slope capacitor, inductor, switching frequency, and inductor satisfies the COMP range limitation.

9.2.2.9 UVLO Divider

The UVLO resistor divider must be designed for turn-on below 4.1 V. Selecting $R_{UVLO,top}$ = 75 kΩ gives a UVLO hysteresis of 0.375 V based on 方程式 32. The lower UVLO resistor is selected using:

$$V_{(VIN,IT+,UVLO)} = V_{IT+(UVLO)} \times \left(1 + \frac{R_{UVLO,top}}{R_{UVLO,bot}}\right) + R_{UVLO,top} \times I_{(UVLO,hyst)} \quad (32)$$

A standard value of 39.0 kΩ is selected for $R_{UVLO,bot}$.

When programming the UVLO threshold for lower input voltage operation, it is important to choose MOSFETs with gate (Miller) plateau voltage lower than the minimum V_{IN}.

9.2.2.10 Soft-Start Capacitor

The soft-start time is programmed using the soft-start capacitor. The relationship between C_{SS} and the soft-start time is given by:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{Ref}} = 18\ \mathrm{nF} \quad (33)$$

C_{SS} = 18 nF gives a soft-start time of 1.8 ms.

9.2.2.11 MOSFETs QH1 and QL1

The input side MOSFETs QH1 and QL1 need to withstand the maximum input voltage of 36 V. In addition, they must withstand the transient spikes at SW1 during switching. Therefore, QH1 and QL1 must be rated for 50 V or higher. The gate plateau voltages of the MOSFETs must be smaller than the minimum input voltage of the converter, otherwise, the MOSFETs may not fully enhance during start-up or overload conditions.

The power loss in QH1 in boost mode is approximated by:

$$P_{COND(QH1)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QH1)} \quad (34)$$

The power loss in QH1 in buck mode consists of both conduction and switching loss components given by 方程式 35 and 方程式 36, respectively:

$$P_{COND(QH1)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QH1)} \quad (35)$$

$$P_{SW(QH1)} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW} \quad (36)$$

The rise (t_r) and the fall (t_f) times are based on the MOSFET data sheet information or measured in the lab. Typically, a MOSFET with smaller R_{DSON} (smaller conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QL1 in the buck mode of operation is shown in 方程式 37:

$$P_{COND(QL1)} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT}^2 \times R_{DS,On(QL1)} \quad (37)$$

9.2.2.12 MOSFETs QH2 and QL2

The output side MOSFETs QH2 and QL2 see the output voltage of 16 V and additional transient spikes at SW2 during switching. Therefore, QH2 and QL2 must be rated for 25 V or more. The gate plateau voltages of the MOSFETs must be smaller than the minimum input voltage of the converter, otherwise, the MOSFETs may not fully enhance during start-up or overload conditions.

The power loss in QH2 in buck mode of operation is approximated by:

$$P_{COND(QH2)} = I_{OUT}^2 \times R_{DS,On(QH2)} \quad (38)$$

The power loss in QL2 in the boost mode of operation consists of both conduction and switching loss components given by 方程式 39 and 方程式 40, respectively:

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$$P_{COND(QL2)} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QL2)} \tag{39}$$

$$P_{SW(QL2)} = \frac{1}{2} \times V_{OUT} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right) \times (t_r + t_f) \times f_{SW} \tag{40}$$

The rise (t_r) and the fall (t_f) times can be based on the MOSFET data sheet information or measured in the lab. Typically, a MOSFET with smaller R_{DSON} (lower conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QH2 in the boost mode of operation is shown in 方程式 41:

$$P_{COND(QH2)} = \frac{V_{IN}}{V_{OUT}} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QH2)} \tag{41}$$

9.2.2.13 Frequency Compensation

This section presents the control loop compensation design procedure for the LM5177 buck-boost controller. The LM5177 operates mainly in buck or boost modes, separated by a transition region, and therefore, the control loop design is done for both buck and boost operating modes. Then, a final selection of compensation is made based on the mode that is more restrictive from a loop stability point of view. Typically, for a converter designed to go deep into both buck and boost operating regions, the boost compensation design is more restrictive due to the presence of a right half plane zero (RHPZ) in boost mode.

The boost power stage output pole location is given by:

$$f_{p1(boost)} = \frac{1}{2\pi}\left(\frac{2}{R_{OUT} \times C_{OUT}}\right) = 1.44\ \text{kHz} \tag{42}$$

where

- R_{OUT} = 1.7 Ω corresponds to the maximum load of 9.4 A.

The boost power stage ESR zero location is given by:

$$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR} \times C_{OUT}}\right) = 265\ \text{kHz} \tag{43}$$

The boost power stage RHP zero location is given by:

$$f_{RHP} = \frac{1}{2\pi}\left(\frac{R_{OUT} \times (1 - D_{MAX})^2}{L_1}\right) = 4.72\ \text{kHz} \tag{44}$$

where

- D_{MAX} is the maximum duty cycle at the minimum V_{IN}.

The buck power stage output pole location is given by:

$$f_{p1(buck)} = \frac{1}{2\pi}\left(\frac{1}{R_{OUT} \times C_{OUT}}\right) = 720\ \text{Hz} \tag{45}$$

The buck power stage ESR zero location is the same as the boost power stage ESR zero.

It is clear from 方程式 46 that RHP zero is the main factor limiting the achievable bandwidth. For a robust design, the crossover frequency must be less than 1/3 of the RHP zero frequency. Given the position of the RHP zero, a reasonable target bandwidth in boost operation is around 1 kHz:

$$f_{bw} = 1\ \text{kHz} \tag{46}$$

For some power stages, the boost RHP zero may not be as restrictive, which happens when the boost maximum duty cycle (D_{MAX}) is small, or when a really small inductor is used. In those cases, compare the limits posed by the RHP zero (f_{RHP} / 3) with 1/20 of the switching frequency and use the smaller of the two values as the achievable bandwidth.

The compensation zero can be placed at 1.5 times the boost output pole frequency. Keep in mind that this locates the zero at three times the buck output pole frequency, which results in approximately 30 degrees of phase loss before crossover of the buck loop and 15 degrees of phase loss at intermediate frequencies for the boost loop:

$$f_{ZC} = 2.16\,\mathrm{kHz} \tag{47}$$

If the crossover frequency is well below the RHP zero and the compensation zero is placed well below the crossover, the compensation gain resistor, R_{c1}, is calculated using the approximation:

$$R_{C1} = \frac{2\pi \times f_{bw}}{gm_{EA}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times \frac{A_{CS} \times R_{SENSE} \times C_{OUT}}{1 - D_{MAX}} \times \frac{1}{\sqrt{1 + \left(\frac{f_{bw}}{f_{RHP}}\right)^2}} = 1.1\,\mathrm{k\Omega} \tag{48}$$

where

- D_{MAX} is the maximum duty cycle at the minimum V_{IN} in boost mode.
- A_{CS} is the current sense amplifier gain.

The compensation capacitor, C_{c1}, is then calculated from:

$$C_{C1} = \frac{1}{2\pi \times f_{ZC} \times R_{c1}} = 97\mathrm{nF} \tag{49}$$

The standard values of compensation components are selected to be R_{c1} = 768 Ω and C_{c1} = 100 nF.

A high frequency pole (f_{pc2}) is placed using a capacitor (C_{c2}) in parallel with R_{c1} and C_{c1}. Set the frequency of this pole at seven to ten times of f_{bw} to provide attenuation of switching ripple and noise on COMP while avoiding excessive phase loss at the crossover frequency. For a target f_{pc2} = 10 kHz, C_{c2} is calculated using 方程式 50:

$$C_{C2} = \frac{1}{2\pi \times f_{pc2} \times R_{c1}} = 20.9\,\mathrm{nF} \tag{50}$$

Select a standard value of 22 nF for C_{c2}. These values provide a good starting point for the compensation design. Each design must be tuned in the lab to achieve the desired balance between stability margin across the operating range and transient response time.

ADVANCE INFORMATION

9.2.3 Application Curves

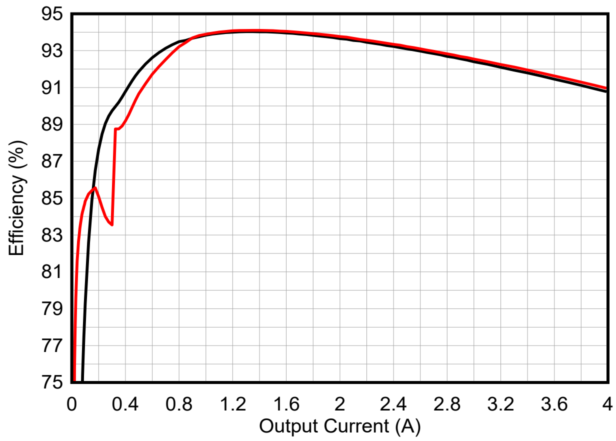

图 9-2. Efficiency Versus I_O in Boost Mode (V_{IN} = 5 V)

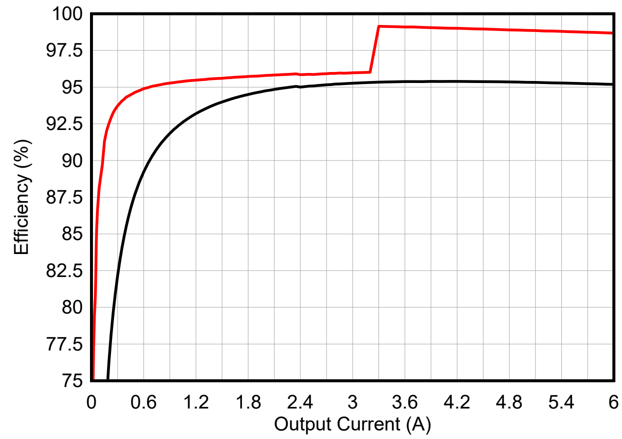

图 9-3. Efficiency Versus I_O in Buck-Boost Mode (V_{IN} = 16 V)

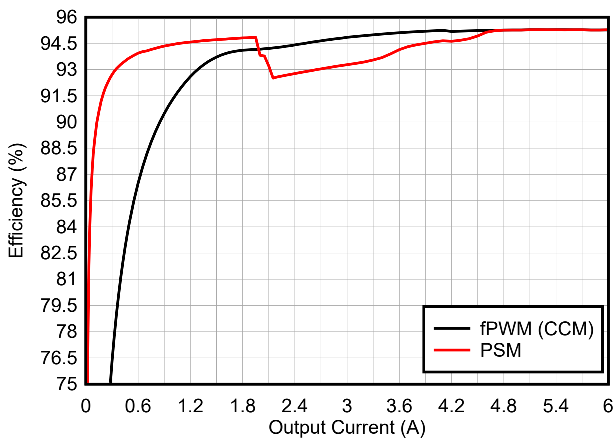

图 9-4. Efficiency Versus I_O in Buck Mode (V_{IN} = 32 V)

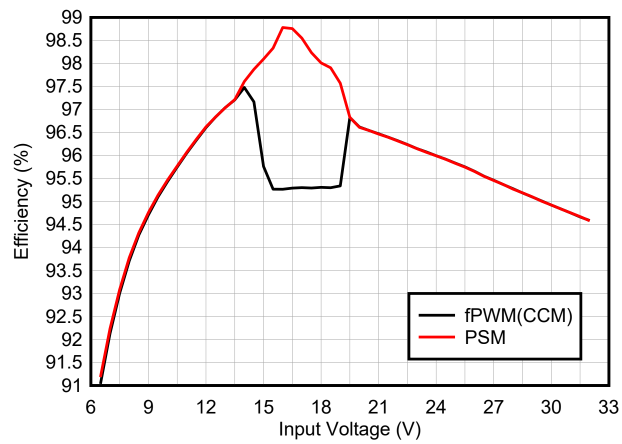

图 9-5. Efficiency Versus V_{IN} (I_O = 5 A)

9.3 System Examples

9.3.1 Bi-Directional Power Backup

The precise reverse current limits of the device enables the LM5177 to charge a storage element on the input of the power stage. Once the integrated average current limitation circuit of the LM5177 is enabled on the input, the third regulation loop maintains a constant current operation to charge the storage on the input for example a battery or super-capacitor array. The end of charge voltage for the input can be regulated by a simple hysteric regulation approach or by using an linear approach with an external operational amplifier as well as an equivalent digital regulation scheme.

Once the system power supply is interrupted or has a malfunction the LM5177 imitatively supplies the connected system as the selected transition voltage threshold triggers. The seamless transition is maintained by the buck-boost voltage control loop, which stays in regulation during charging and ensures a minimum of voltage drop for the connected system during backup.

Benefits:

- Seamless and automatic transition from main system supply to the power backup
- Combination of energy storage charging control and backup regulator with a single chip solution
- Single inductor solution, that is one power stage for charging and backup operation
- Constant current constant voltage operation possible to realize with

- Adjustable on-the-fly transition voltage using the output feedback divider
- Scalable solution for multiple systems. Power levels are adjusted with the BOM. Topologies and architecture qualification maintains the same.

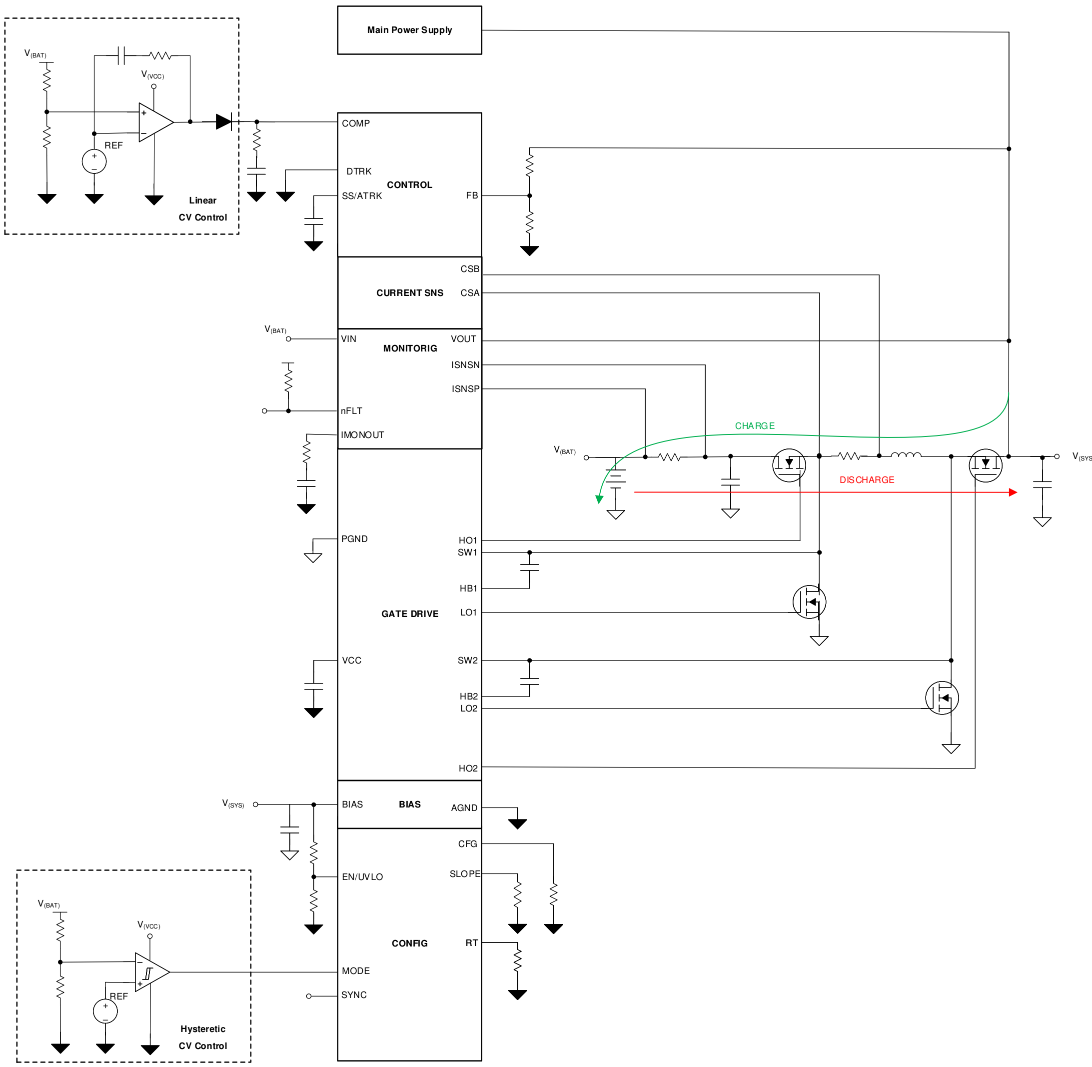

图 9-6. Simplified Schematic of a Bi-Directional Operation

Below you find a overview for the control loop interacting together in the DC/DC Backup application. The central point for the interaction is the COMP pin which defines the peak current target for the underlying bi directional peak current control loop

1. Internal peak current loop. The control input signal from the COMP pin sets the bi-directional (positive and negative pack current) for the PWM logic.
2. The internal output voltage loop is controlling the V_O or system voltage once the system supply voltage is not there any more and V_O drops below the selected voltage by the FB-PIN
3. The internal constant current loop limits and regulates the peak current in the selected direction. For most power backup cases the negative (charging) current is selected. By activating the constant current limit the peak current gets clamped and can not reach his full value which enables a lower charging current that the forward discharging current as the forward direction don’t get limited if the negative direction of the constant current loop is selected.
4. The input voltage (V_{BAT}) constant voltage regulation can be added externally with a linear regulator in the COMP-pin. Once the battery voltage reaches the desired voltage target the regulator pull-sup the peak current set-point that the charging operation stops.

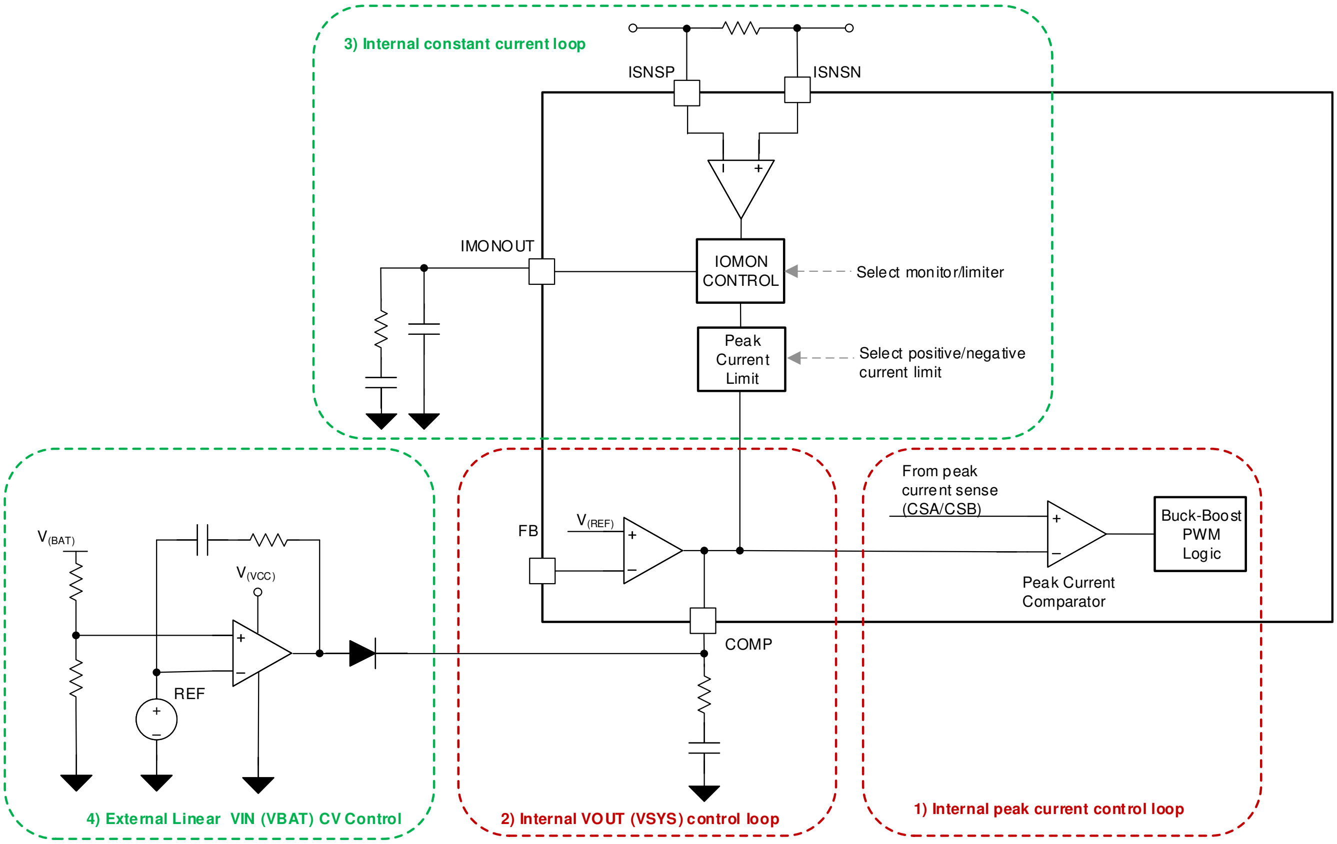

图 9-7. Overview of the Control loops for DC/DC Backup application

10 Power Supply Recommendations

The LM5177 is designed to operate over a wide input voltage range. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use 方程式 51 to estimate the average input current.

$$I_I = \frac{P_O}{V_I \eta} \tag{51}$$

where

- η the efficiency.

One way to get a value for the efficiency is the data from the efficiency graphs in 节 9.2.3 in the worst case operation mode. For most applications, the boost operation is the region of highest input current.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. One way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. An EMI input filter is often used in front of the controller power stage. Unless carefully designed, it can lead to instability as well as some of the previously mentioned affects.

11 Layout

A proper PCB design and layout is important in high-current, fast-switching circuits (with high current and voltage slew rates) to achieve a robust and reliable design. As expected, certain topics must be considered for the design of the PCB layout for the LM5177.

11.1 Layout Guidelines

11.1.1 Power Stage Layout

Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of the buck-boost regulator and are typically placed on the top side of the PCB. The benefits of convective heat transfer are maximized when leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side. Insert at least one inner plane, connected to ground, to shield, and isolate the small-signal traces from noisy power traces.

The DC/DC regulator has several high-current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.

- The most important loop areas to minimize are the path from the input capacitors through the buck high-side and low-side MOSFETs, and back to the ground connection of the input capacitor and the path from the output capacitors through the boost high-side and low-side MOSFETs, and back to the ground connection of the output capacitor. Connect the negative terminal of the capacitor close to the source of the low-side MOSFETs (at ground). Similarly, connect the positive terminal of the capacitor or capacitors close to the drain of the high-side MOSFETs of both loops.
- In addition to these recommendation, follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.

11.1.2 Gate Driver Layout

The LM5177 high-side and low-side gate drivers incorporate short propagation delays, frequency depended dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the external power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths are not well controlled. Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, and thereby increasing MOSFET switching times.

Connections from the gate driver outputs, HO1 and HO2, to the respective gates of the high-side MOSFETs must be as short as possible to reduce series parasitic inductance. Route HO1 and HO2 and SW1 and SW2 gate traces as a differential pair from the device pin to the high-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Connections from gate driver outputs, LO1 and LO2, to the respective gates of the low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Route LO1 and LO2, and PGND traces as a differential pair from the device pin to the low-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Minimize the current loop path from the VCC, HB1, and HB2 pins through their respective capacitors as these provide the high instantaneous current.

11.1.3 Controller Layout

With the provision to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP, FB, SLOPE, SS/ATRK, and RT away from high-voltage switching nodes such as the following to avoid mutual coupling:
  - SW1

- SW2
- HO1
- HO2
- LO1
- LO2
- HB1
- HB2
- Use an internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
- Route the CSA and CSB and ISNSP and ISNSN traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor.
- Locate the upper and lower feedback resistors close to the FB pins, keeping the FB traces as short as possible. Route the trace from the upper feedback resistor or resistors to the output voltage sense point.
- Use a common ground node for power ground and a different one for analog ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.
- The HTSSOP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate (ground) of the device. This connection allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem.

11.2 Layout Example

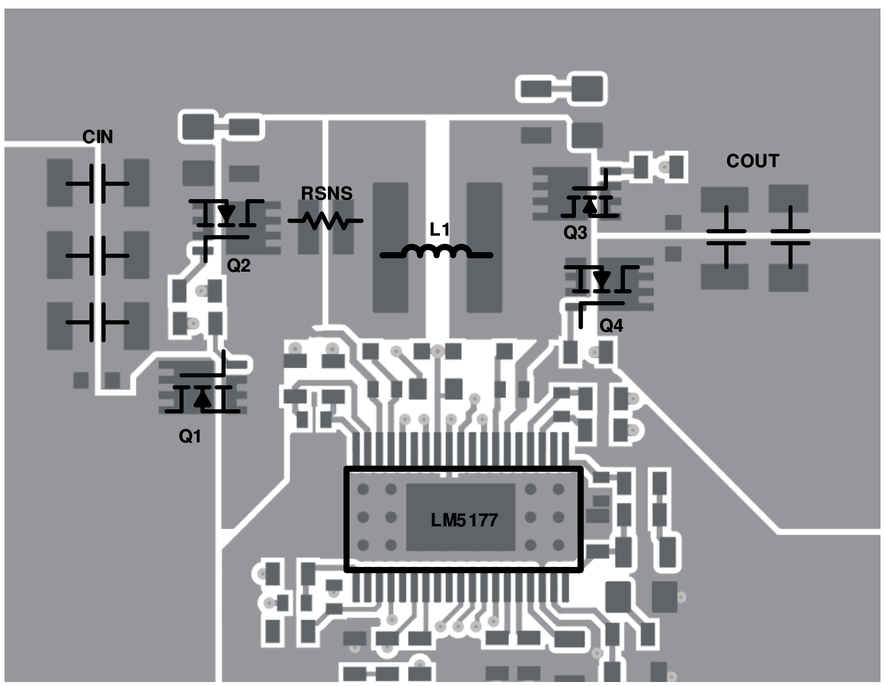

图 11-1. LM5177 Top Layer Routing Example

ADVANCE INFORMATION

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Device Support

12.1.1 第三方产品免责声明

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12.1.2 Development Support

12.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM5177 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

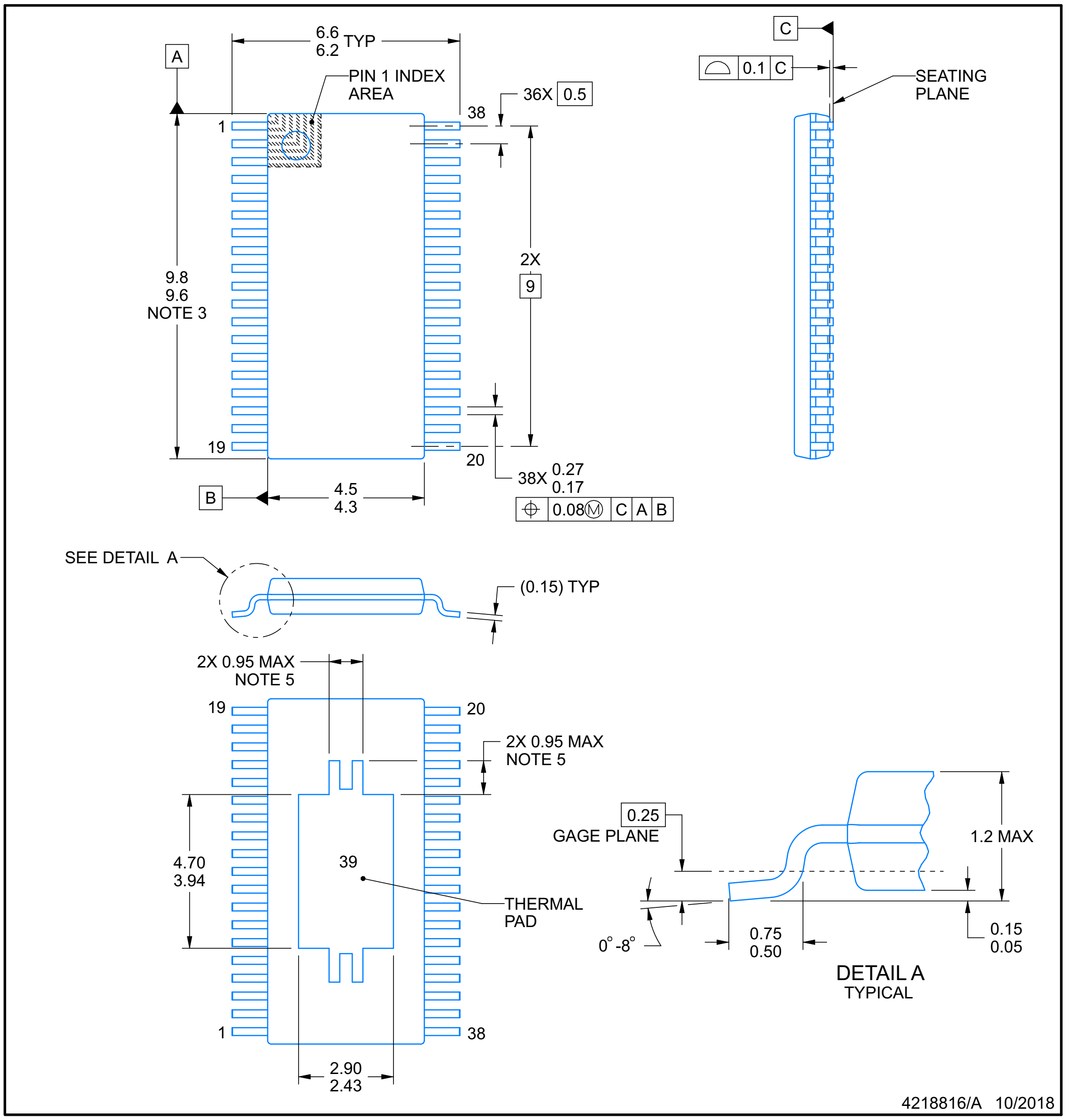
ADVANCE INFORMATION

PACKAGE OUTLINE

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

TEXAS INSTRUMENTS
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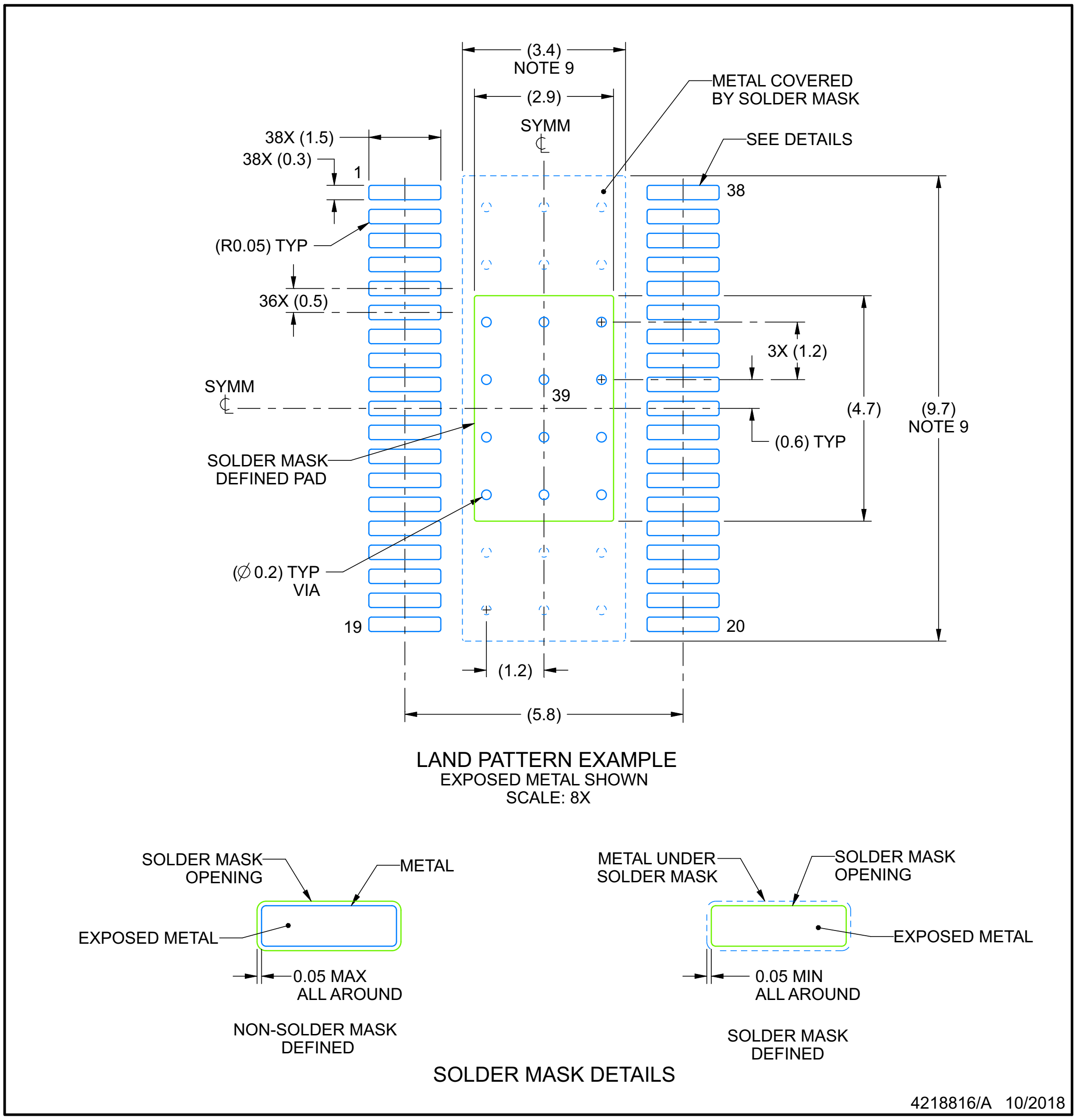
EXAMPLE BOARD LAYOUT

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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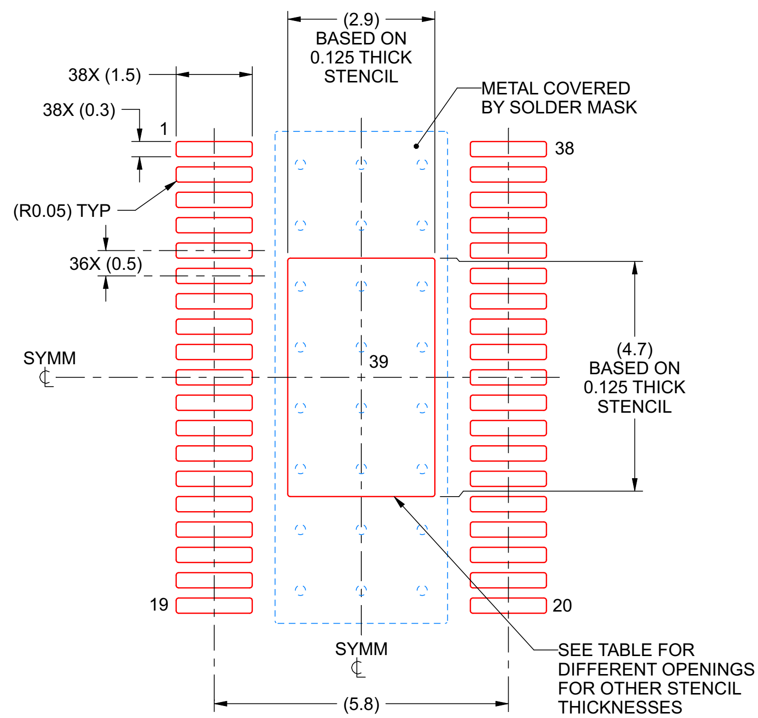
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

4218816/A 10/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLM5177DCPR	ACTIVE	HTSSOP	DCP	38	2500	TBD	Call TI	Call TI	-40 to 150		Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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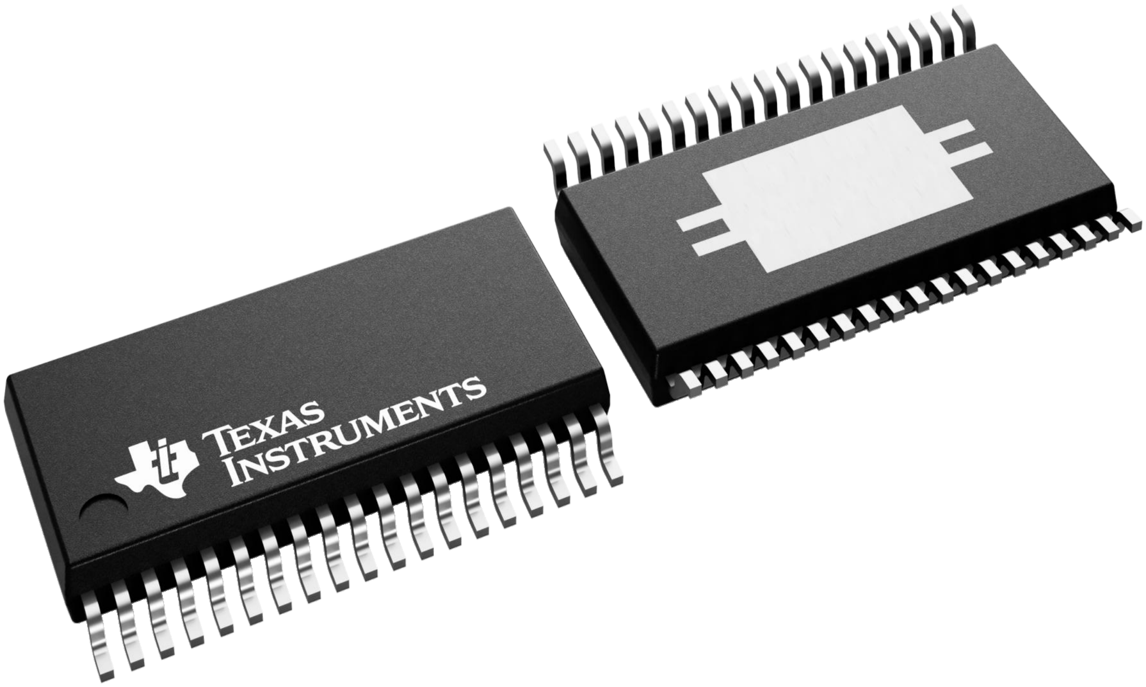
GENERIC PACKAGE VIEW

DCP 38 — PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch — SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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