V 类 2x2 交叉点交换机

查询样片: **SN55LVCP22-SP**

特性

- 针对 **DS90CP22 2x2** 低压差分信号 **(LVDS)** 交叉点交换机的高速 **(>1000Mbps)** 升级
- 低抖动完全差分数据路径
- **50ps**（典型值）的峰值到峰值抖动，此时伪随机二进制序列 **(PRBS) =** 2^{23}**-1** 样式
- 总功率耗散少于 **200mW**（典型值），**300mW**（最大值）
- 输出（通道到通道）偏斜为 **80ps**（典型值）
- 可配置为 **2:1** 复用，**1:2** 去复用，集线器或者 **1:2** 信号分配器
- 输入可接受 **LVDS**，低电压正射极耦合逻辑 **(LVPECL)**，电路模式逻辑 **(CML)** 信号
- **1.7ns**（典型值）的快速交换时间
- **0.65ns**（典型值）的快速传播延迟
- 采用 **16** 引脚陶瓷扁平 **(CFP)** 封装
- 与 **TIA/EIA-644-A LVDS** 标准互操作
- 军用温度范围：**-55°C** 至 **125°C**

应用范围

- 基站
- 分插复用器
- 针对串行背板的保护开关
- 网络交换机/路由器
- 光网络线路卡/交换机
- 时钟分配
- 可提供工程评估 **(/EM)** 样品 (1)

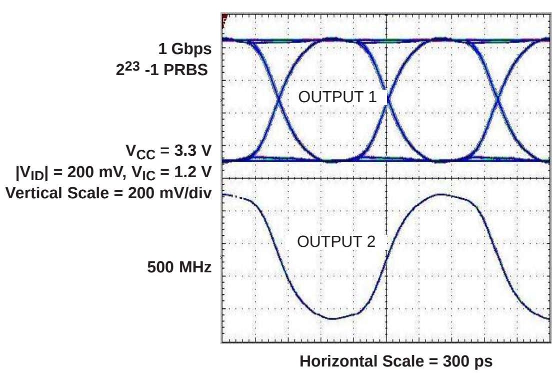
(1) 这些部件只用于工程评估。 它们的加工工艺为非兼容流程 (例如，无预烧过程等) ，并且只在 25°C 的温度额定值下测试。 这些部件不适合于品质检定、生产、辐射测试或飞行使用。 不担保完全军用额定温度 -55°C 至 125°C 范围内或使用寿命内的部件性能。

说明

SN55LVCP22 是一款 2x2 交叉点交换机，此交换机为每个路径提供速度大于 1000Mbps 的运行。 双通道组装有宽共模（0V 至 4V）接收器，从而实现对 LVDS，LVPECL，和 CML 信号的接收。 此双输出为 LVDS 驱动器以提供低功耗、低电磁干扰 (EMI)、高速运转。 SN55LVCP22 提供一个支持 2:2 缓冲（复示），1:2 分配，2:1 复用，2x2 交换的单一器件，以及每个通道上的 LVPECL/CML 到 LVDS 电平转换。 SN55LVCP22 的灵活操作提供了一个单一器件支持光网络、无限基础设施、和数据通信系统中常见的容错系统对于冗余串行总线传输的需求（运转和保护交换卡）。 TI 在 SN65LVDS100 和 SN65LVDS122 中提供了额外的千兆比特集线器/转换器以及交叉点产品。

SN55LVCP22 使用一个完全差分数据路径来确保低噪声生成、快速交换时间、低脉宽失真、和低抖动。 80ps（典型值）的输出通道到通道偏斜确保所有应用中输出的准确校准。 提供了小外形尺寸集成电路 (SOIC) 和薄型小尺寸 (TSSOP) 封装选项可实现对现有解决方案的轻松升级，并且当电路板空间有限时节省其空间。

OUTPUTS OPERATING SIMULTANEOUSLY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

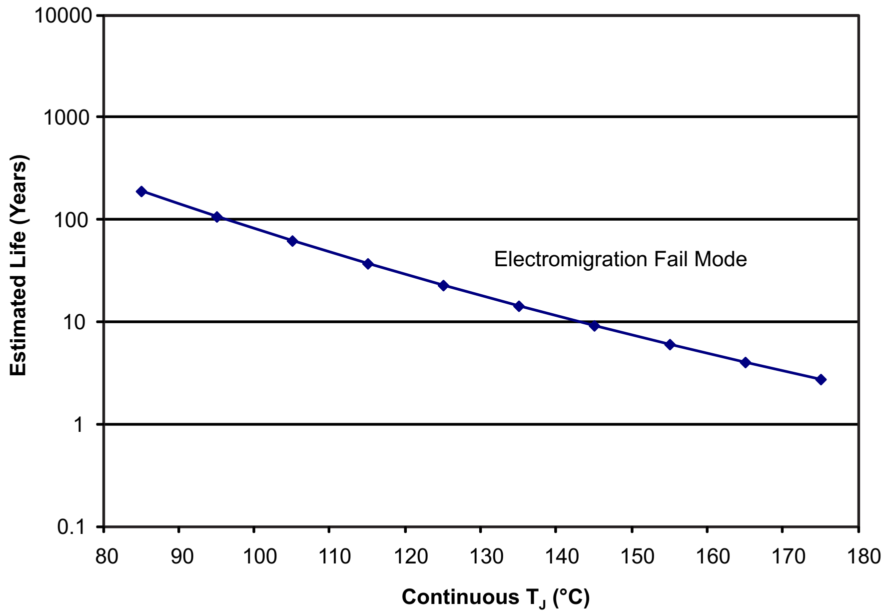
English Data Sheet: SLLSE43

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

THERMAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS	VALUE	UNITS
θ_{JA}	Junction-to-ambient thermal resistance			82.5	°C/W
θ_{JC}	Junction-to-case thermal resistance			7.5	°C/W
P_D	Device power dissipation	Typical	V_{CC} = 3.3 V, T_A = 25°C, 1 Gbps	198	mW
		Maximum	V_{CC} = 3.6 V, T_A = 125°C, 1 Gbps	313	



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

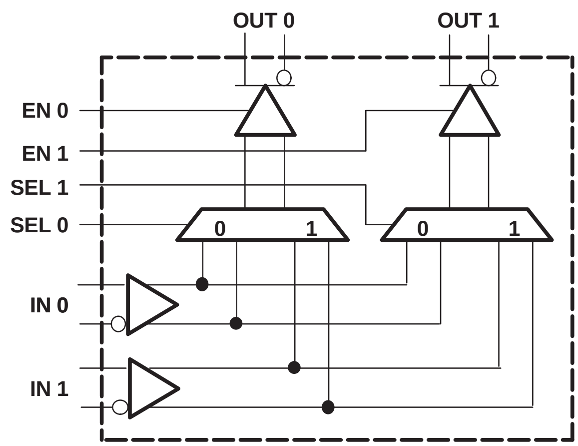
C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 1. SN55LVCP22-SP Operating Life Derating Chart

Table 1. FUNCTION TABLE

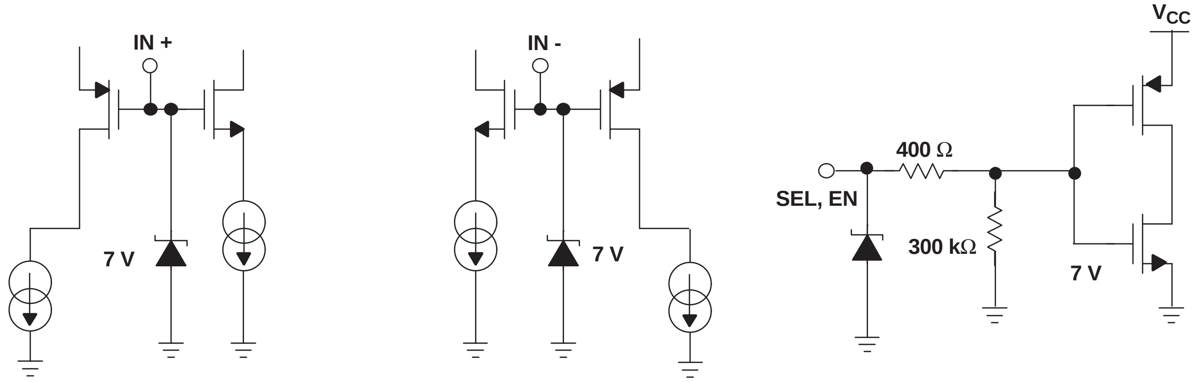
SEL0	SEL1	OUT0	OUT1	FUNCTION
0	0	IN0	IN0	1:2 Splitter
0	1	IN0	IN1	Repeater
1	0	IN1	IN0	Switch
1	1	IN1	IN1	1:2 Splitter

FUNCTIONAL BLOCK DIAGRAM

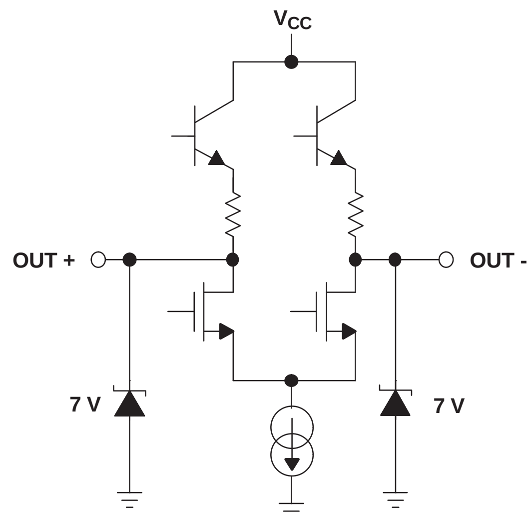


EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUTS



OUTPUTS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

			UNITS
Supply voltage[2] range, V_{CC}			–0.5 V to 4 V
CMOS/TTL input voltage (ENO, EN1, SEL0, SEL1)			–0.5 V to 4 V
LVDS receiver input voltage (IN+, IN–)			–0.7 V to 4.3 V
LVDS driver output voltage (OUT+, OUT–)			–0.5 V to 4 V
LVDS output short circuit current			Continuous
Storage temperature range			–65°C to 125°C
Maximum Junction temperature			150°C
Electrostatic discharge	Human body model[3]	All pins	±5 kV
	Charged-device mode[4]	All pins	±500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminals.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	0		4	V
Operating Case Ttemperature range, T_C (1)	–55		125	°C
Magnitude of differential input voltage $\|V_{ID}\|$	0.1		3	V

(1) Maximum case temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS (EN0, EN1, SEL0, SEL1)						
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.8	V
I_{IH}	High-level input current	V_{IN} = 3.6 V or 2.0 V, V_{CC} = 3.6 V	-25	±3	25	µA
I_{IL}	Low-level input current	V_{IN} = 0.0 V or 0.8 V, V_{CC} = 3.6 V	-15	±1	15	µA
V_{CL}	Input clamp voltage	I_{CL} = –18 mA		-0.8	-1.5	V
LVDS OUTPUT SPECIFICATIONS (OUT0, OUT1)						
$\|V_{OD}\|$	Differential output voltage	R_L = 75 Ω, See Figure 3	255	365	475	mV
		R_L = 75 Ω, V_{CC} = 3.3 V, T_A = 25°C, See Figure 3	285	365	440	
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	V_{ID} = ±100 mV, See Figure 3	–25		25	mV
V_{OS}	Steady-state offset voltage	See Figure 4	1	1.2	1.45	V
ΔV_{OS}	Change in steady-state offset voltage between logic states	See Figure 4	–25		25	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 4		50		mV
I_{OZ}	High-impedance output current	V_{OUT} = GND or V_{CC}	-15		15	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V, 1.5 V; V_{OUT} = 3.6 V or GND	-15		15	µA
I_{OS}	Output short-circuit current	V_{OUT+} or V_{OUT-} = 0 V			-8	mA
I_{OSB}	Both outputs short-circuit current	V_{OUT+} and V_{OUT-} = 0 V	–8		8	mA
C_O	Differential output capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		3		pF
LVDS RECEIVER DC SPECIFICATIONS (IN0, IN1)						
V_{TH}	Positive-going differential input voltage threshold	See Figure 2 and Table 2			100	mV
V_{TL}	Negative-going differential input voltage threshold	See Figure 2 and Table 2	–100			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis			25	150	mV
V_{CMR}	Common-mode voltage range	V_{ID} = 100 mV, V_{CC} = 3.0 V to 3.6 V	0.05		3.95	V
I_{IN}	Input current	V_{IN} = 4 V, V_{CC} = 3.6 V or 0.0	-18	±1	18	µA
		V_{IN} = 0 V, V_{CC} = 3.6V or 0.0	-18	±1	18	
C_{IN}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
SUPPLY CURRENT						
I_{CCQ}	Quiescent supply current	R_L = 75 Ω, EN0=EN1=High		60	87	mA
I_{CCD}	Total supply current	R_L = 75 Ω, C_L = 5 pF, 500 MHz (1000 Mbps), EN0=EN1=High		63	87	mA
I_{CCZ}	3-state supply current	EN0 = EN1 = Low		25	35	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

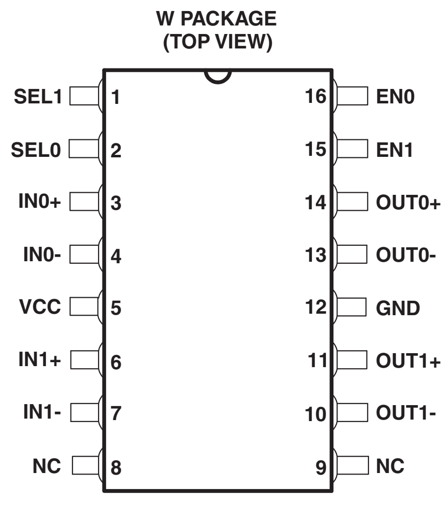
SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

parameter		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Input to SEL setup time	See Figure 7	2.2	0.8		ns
t_{HOLD}	Input to SEL hold time	See Figure 7	2.2	1.0		ns
t_{SWITCH}	SEL to switched output	See Figure 7		1.7	2.6	ns
t_{PHZ}	Disable time, high-level-to-high-impedance	See Figure 6		2	8	ns
t_{PLZ}	Disable time, low-level-to-high-impedance	See Figure 6		2	8	ns
t_{PZH}	Enable time, high-impedance -to-high-level output	See Figure 6		2	8	ns
t_{PZL}	Enable time, high-impedance-to-low-level output	See Figure 6		2	8	ns
t_{LHT}	Differential output signal rise time (20%-80%)(1)	C_L = 5 pF, See Figure 5		280	620	ps
t_{HLT}	Differential output signal fall time (20%-80%)(1)	C_L = 5 pF, See Figure 5		280	620	ps
t_{JIT}	Added peak-to-peak jitter	V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 50 MHz, C_L = 5 pF		13.7	22.2	ps
		V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 240 MHz, C_L = 5 pF		13.4	24.5	
		V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 500 MHz, C_L = 5 pF		14.4	35.7	
		V_{ID} = 200 mV, PRBS = 2^{15}-1 data pattern, V_{CM} = 1.2 V, 240 Mbps, C_L = 5 pF		68.3	204	ps
		V_{ID} = 200 mV, PRBS = 2^{15}-1 data pattern, V_{CM} = 1.2 V, 1000 Mbps, C_L = 5 pF		73.2	282	
t_{Jrms}	Added random jitter (rms)	V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 50 MHz, C_L = 5 pF		0.97	1.5	ps_{RMS}
		V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 240 MHz, C_L = 5 pF		0.85	1.53	
		V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 500 MHz, C_L = 5 pF		0.86	1.79	
t_{PLHD}	Propagation delay time, low-to-high-level output(1)		200	650	2350	ps
t_{PHLD}	Propagation delay time, high-to-low-level output(1)		200	650	2350	ps
t_{skew}(2)	Pulse skew ($\|t_{PLHD} - t_{PHLD}\|$)(3)	C_L = 5 pF, See Figure 5		45	160	ps
t_{CCS}	Output channel-to-channel skew, splitter mode	C_L = 5 pF, See Figure 5		80		ps
f_{MAX}(2)	Maximum operating frequency(4)		1			GHz

(1) Input: V_{IC} = 1.2 V, V_{ID} = 200 mV, 50% duty cycle, 1 MHz, t_r/t_f = 500 ps
(2) t_{skew} and f_{MAX} parameters are guaranteed by characterization, but not production tested.
(3) t_{skew} is the magnitude of the time difference between the t_{PLHD} and t_{PHLD} of any output of a single device.
(4) Signal generator conditions: 50% duty cycle, t_r or t_f ≤ 100 ps (10% to 90%), transmitter output criteria: duty cycle = 45% to 55% V_{OD} ≥ 300 mV.

PIN ASSIGNMENTS



NC - No internal connection

PARAMETER MEASUREMENT INFORMATION

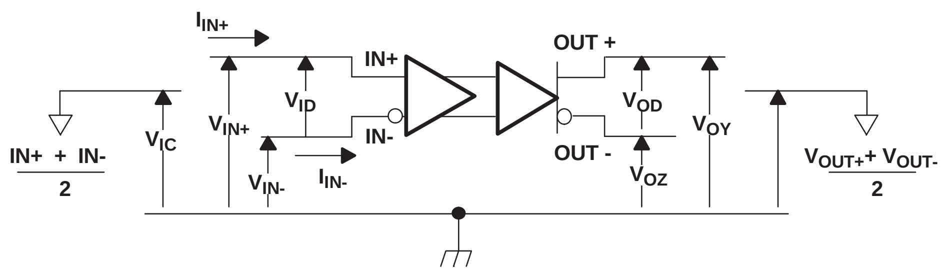


Figure 2. Voltage and Current Definitions

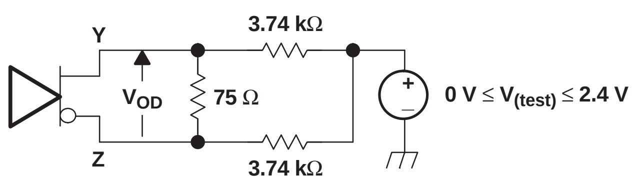
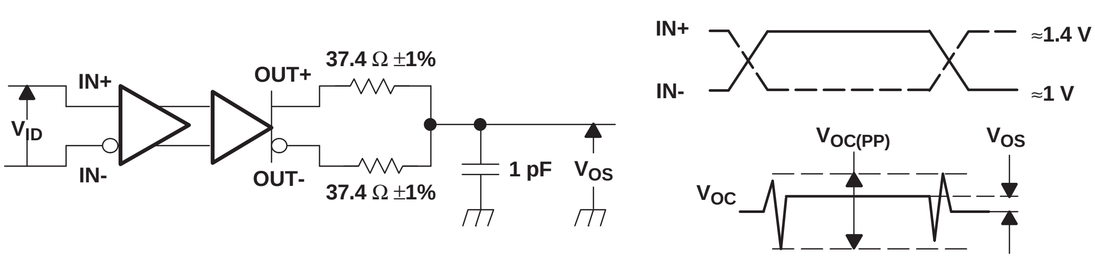


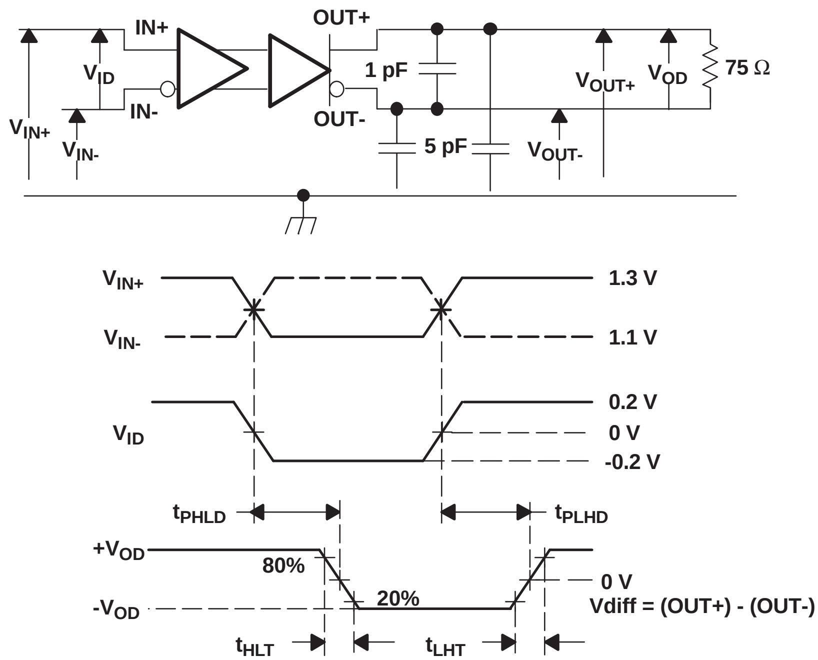
Figure 3. Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns; R_L = 100 Ω; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

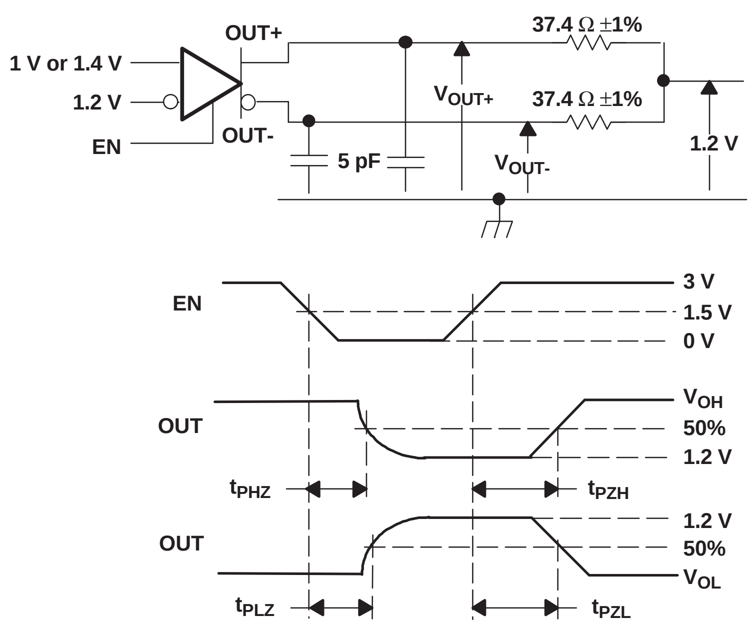
Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ .25 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Timing Test Circuit and Waveforms



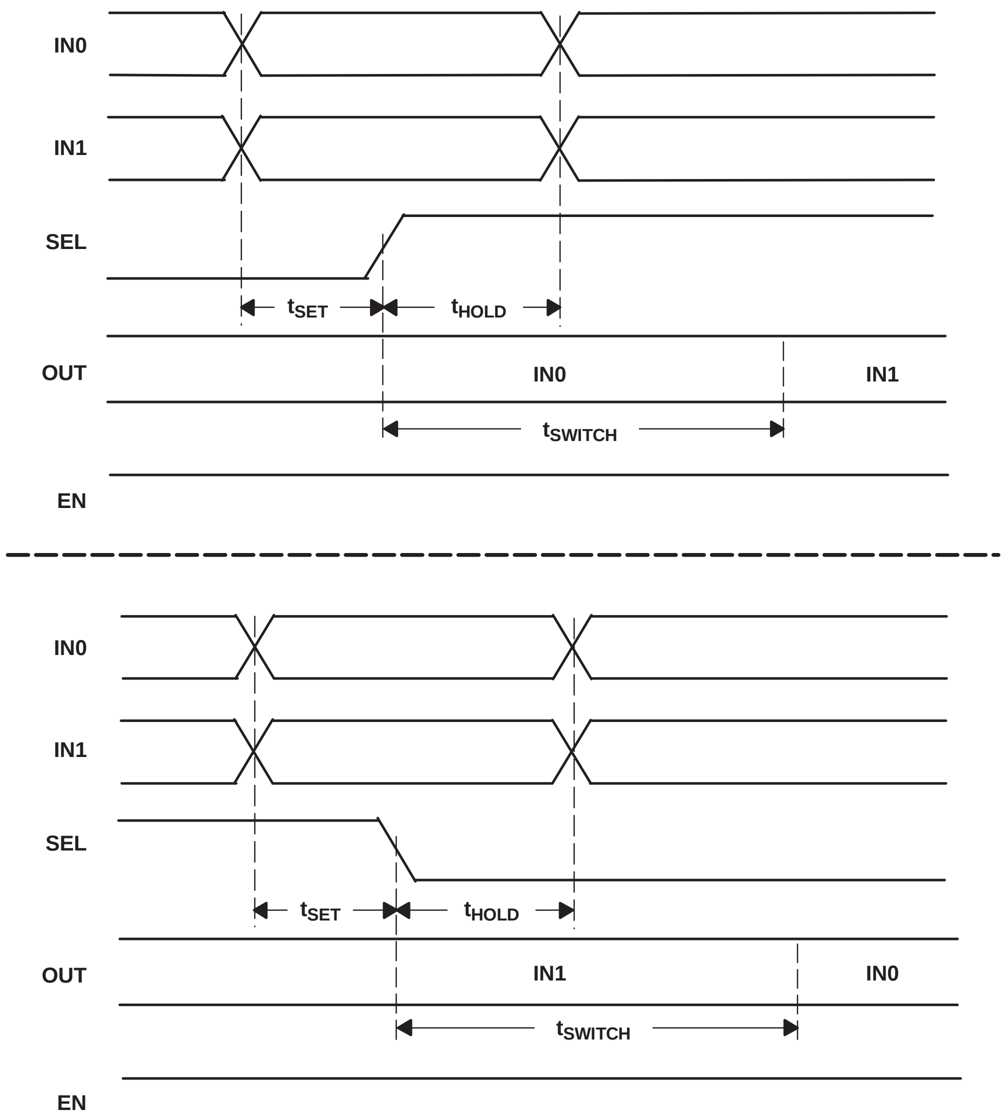
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 6. Enable and Disable Time Circuit and Definitions

Table 2. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

(1) H = high level, L = low level



NOTE: t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 7. Input to Select for Both Rising and Falling Edge Setup and Hold Times

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE vs RESISTIVE LOAD

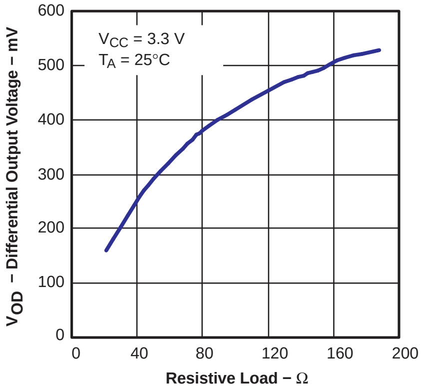


Figure 8.

SUPPLY CURRENT vs FREQUENCY

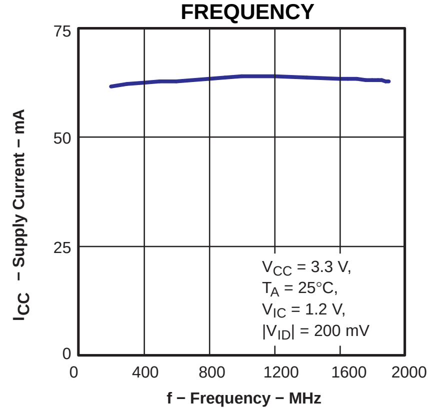


Figure 9.

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

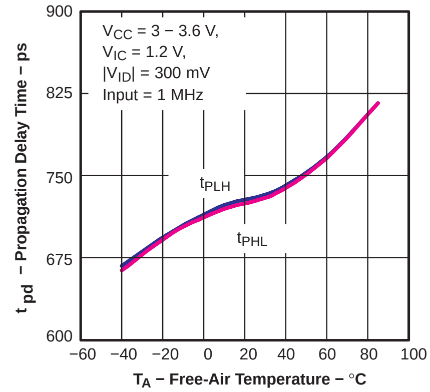


Figure 10.

PEAK-TO-PEAK JITTER vs FREQUENCY

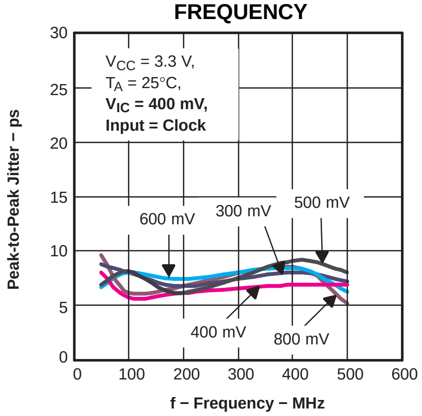


Figure 11.

PEAK-TO-PEAK JITTER vs DATA RATE

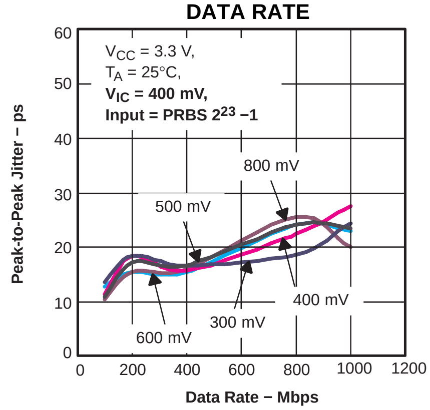


Figure 12.

PEAK-TO-PEAK JITTER vs FREQUENCY

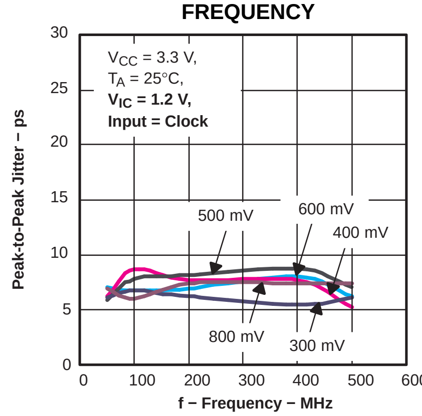


Figure 13.

PEAK-TO-PEAK JITTER vs DATA RATE

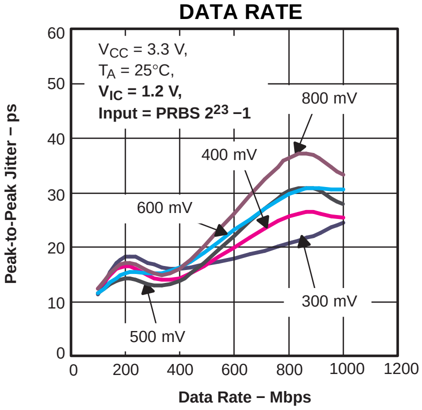


Figure 14.

PEAK-TO-PEAK JITTER vs FREQUENCY

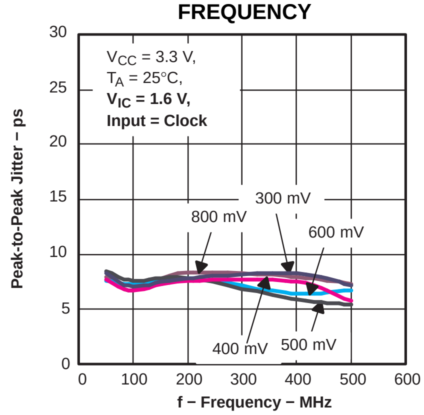


Figure 15.

PEAK-TO-PEAK JITTER vs DATA RATE

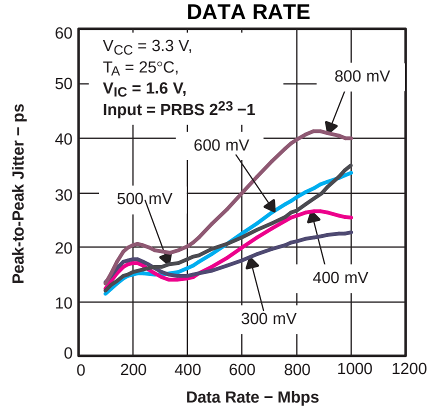


Figure 16.

TYPICAL CHARACTERISTICS (continued)

PEAK-TO-PEAK JITTER vs FREQUENCY

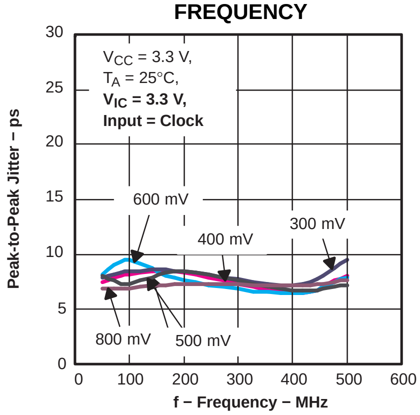


Figure 17.

PEAK-TO-PEAK JITTER vs DATA RATE

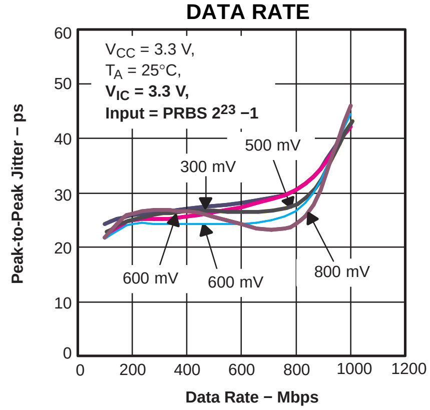


Figure 18.

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

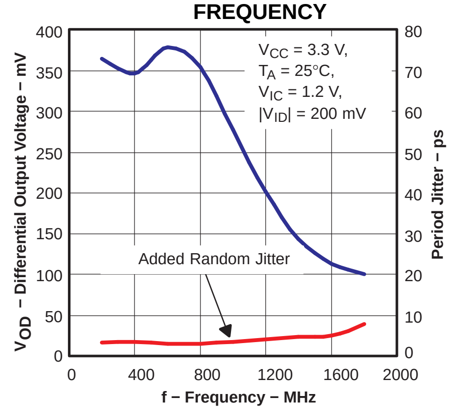


Figure 19.

PEAK-TO-PEAK JITTER vs DATA RATE

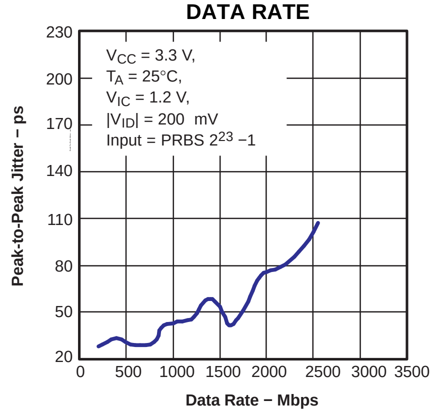


Figure 20.

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

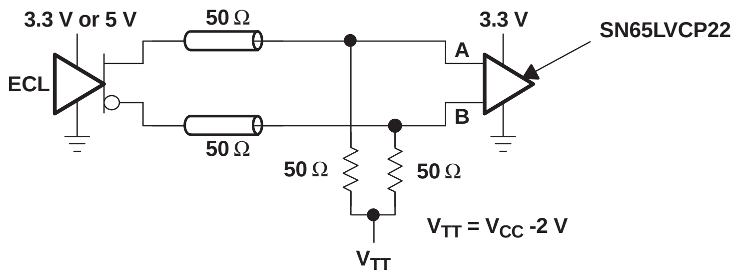


Figure 21. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

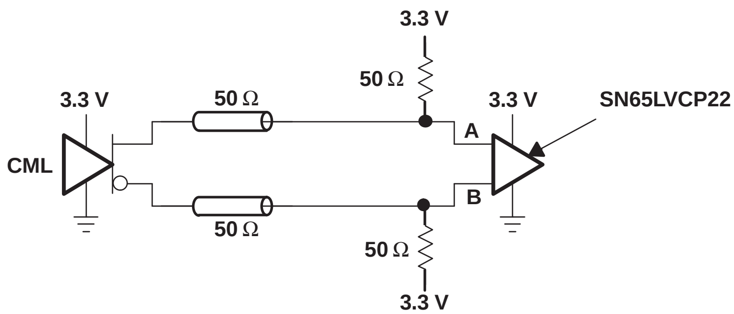


Figure 22. Current-Mode Logic (CML)

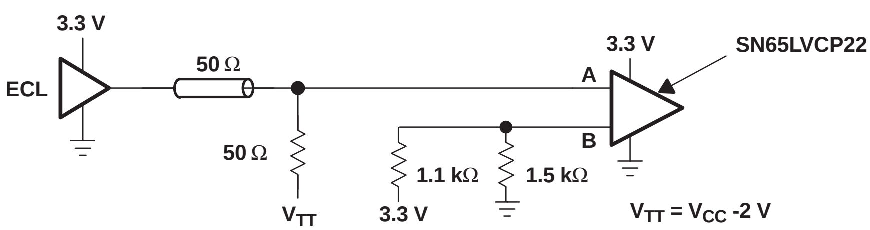


Figure 23. Single-Ended (LVPECL)

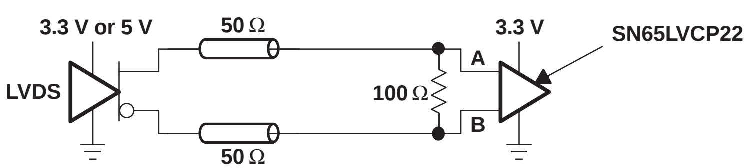


Figure 24. Low-Voltage Differential Signaling (LVDS)

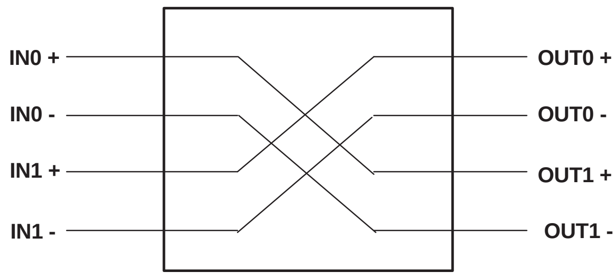


Figure 25. 2 x 2 Crosspoint

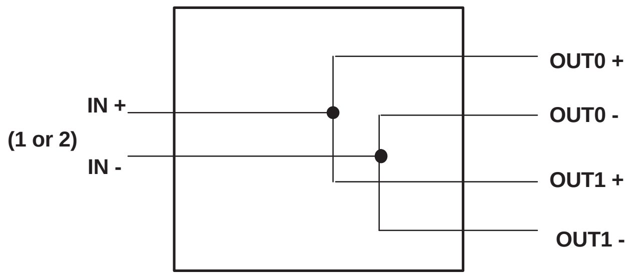


Figure 26. 1:2 Spitter

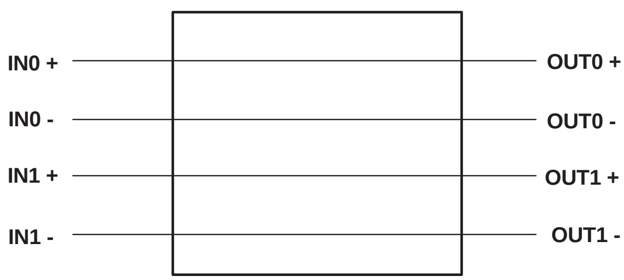


Figure 27. Dual Repeater

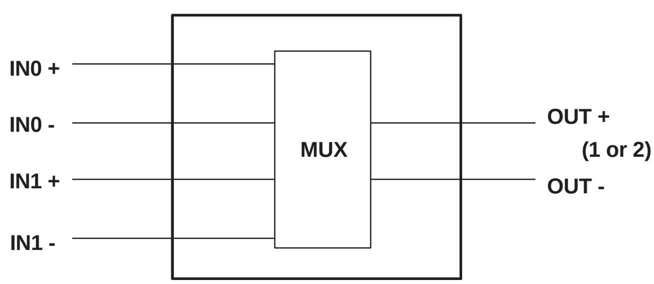


Figure 28. 2:1 MUX

修订历史记录

Changes from Original (June 2012) to Revision A	Page
• Added 将 /EM 着重号添加到特性中	1
• Deleted PACKAGE/ORDERING INFORMATION table	2
• Changed SWITCHING CHARACTERISTICS, t_{JIT} and t_{Jrms}	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1124201VFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-1124201VF A LVCP22W-SP	Samples
SN55LVCP22W/EM	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	0 to 0	SN55LVCP22W/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

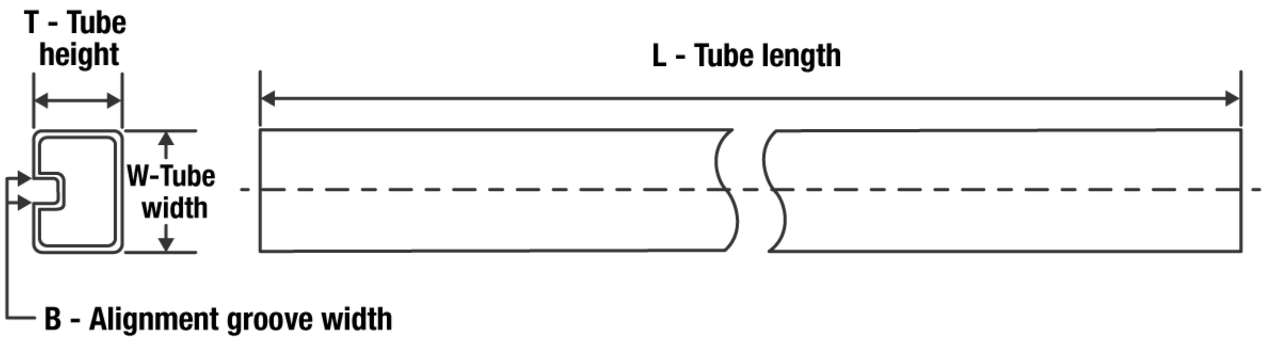
OTHER QUALIFIED VERSIONS OF SN55LVCP22-SP :

- Catalog : SN55LVCP22

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

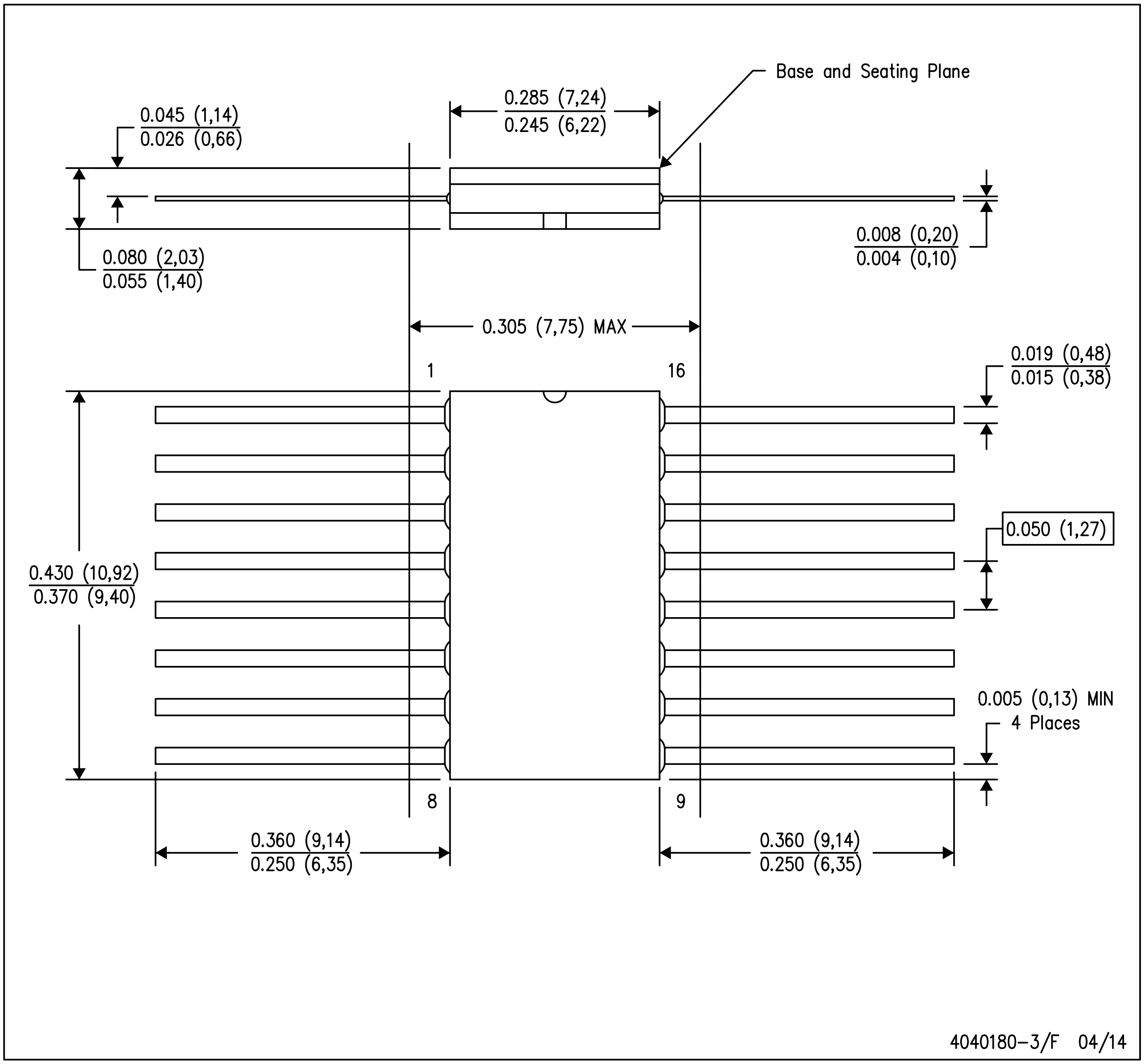
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1124201VFA	W	CFP	16	1	506.98	26.16	6220	NA

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

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