SN6501-Q1 用于隔离电源的变压器驱动器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
  - 器件人体放电模型 (HBM) 静电防护 (ESD) 分类等级 H2
  - 器件 CDM ESD 分类等级 C4B
- 提供功能安全
  - 有助于进行功能安全系统设计的文档
- 用于小型变压器的推挽驱动器
- 3.3V 或 5V 单电源
- 初级侧高电流驱动：
  - 5V 电源：350mA（最大值）
  - 3.3V 电源：150mA（最大值）
- 整流输出上的低纹波允许使用小型输出电容器
- 小型 5 引脚 SOT-23 封装

2 应用

- 用于控制器局域网 (CAN)，RS-485，RS-422，RS-232，串行外设接口 (SPI)，I2C，低功耗局域网 (LAN) 的隔离接口电源
- 工业自动化
- 过程控制
- 医疗设备

3 说明

SN6501-Q1 是一款单片振荡器/电源驱动器，特别设计用于隔离接口应用中的小外形尺寸隔离电源。该器件可驱动来自 3.3V 或者 5V 直流 (DC) 电源的薄型中间抽头的变压器初级。根据变压器的匝数比，变压器的次级可被卷绕以提供任意隔离电压。

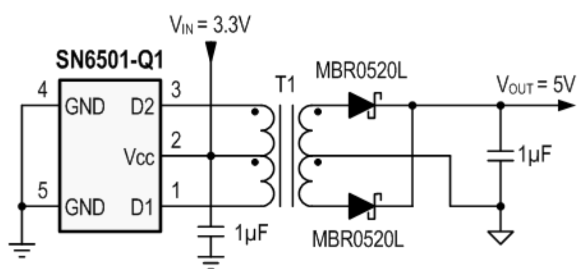
SN6501-Q1 包含一个振荡器，之后是一个栅极驱动电路，此电路提供互补输出信号，用于驱动以地为基准的 N 沟道开关管。此内部逻辑电路确保了两个开关之间的先开后和操作。

SN6501-Q1 采用小型 SOT-23 (5) 封装，其额定运行温度范围为 -40°C 至 125°C。

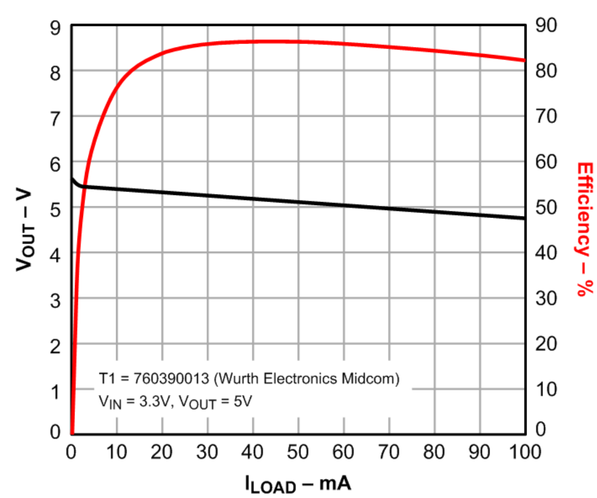
器件信息

器件型号(1)	封装	封装尺寸（标称值）
SN6501-Q1	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图



输出电压和效率与输出电流间的关系

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (October 2020) to Revision C (March 2021) — **Page**

- Added a short-circuit protection note to SN6501 Drive Capability 15
- Changed 方程式 4 18
- Removed duplicate equation labeled as (5) in Revision B........ 18
- Added 17 line items to Recommended Isolation Transformers Optimized for SN6501 20

Changes from Revision A (September 2014) to Revision B (October 2020) — **Page**

- 添加了“功能安全”要点........ 1

Changes from Revision * (June 2013) to Revision A (September 2014) — **Page**

- 添加了*引脚配置和功能* 部分、*处理等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分........ 1
- Changed 方程式 10 18
- Changed 方程式 11 18
- Changed 表 9-4, From: Wuerth-Elektronik / Midcom To: Wurth Electronics Midcom Inc........ 22
- Changed 图 9-16 22

5 Pin Configuration and Functions

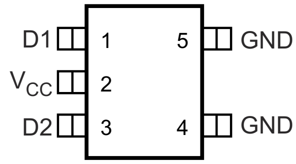


图 5-1. 5-Pin SOT-23 DBV Package Top View

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NUMBER	TYPE	
D1	1	OD	Open Drain output 1. Connect this pin to one end of the transformer primary side.
V_{CC}	2	P	Supply voltage input. Connect this pin to the center-tap of the transformer primary side. Buffer this voltage with a 1 μF to 10 μF ceramic capacitor.
D2	3	OD	Open Drain output 2. Connect this pin to the other end of the transformer primary side.
GND	4,5	P	Device ground. Connect this pin to board ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{D1}, V_{D2}	Output switch voltage		14	V
I_{D1P}, I_{D2P}	Peak output switch current		500	mA
P_{TOT}	Continuous power dissipation		250	mW
T_J	Junction temperature		170	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) AEC-Q100 Classification Level H2, all pins	–2	2	kV
		Charged device model (CDM) AEC-Q100 Classification Level C4B, all pins	–750	750	V

6.3 Recommended Operating Conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			3		5.5	V
V_{D1}, V_{D2}	Output switch voltage	V_{CC} = 5 V ± 10%,	When connected to Transformer with primary winding Center-tapped	0		11	V
		V_{CC} = 3.3 V ± 10%		0		7.2	
I_{D1}, I_{D2}	D1 and D2 output switch current – Primary-side	V_{CC} = 5 V ± 10%	V_{D1}, V_{D2} Swing ⩾ 3.8 V, see 图 6-32 for typical characteristics			350	mA
		V_{CC} = 3.3 V ± 10%	V_{D1}, V_{D2} Swing ⩾ 2.5 V, see 图 6-31 for typical characteristics			150	
T_A	Ambient temperature			–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		SN6501 DBV 5-PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	208.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	87.1	
θ_{JB}	Junction-to-board thermal resistance	40.4	
ψ_{JT}	Junction-to-top characterization parameter	5.2	
ψ_{JB}	Junction-to-board characterization parameter	39.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over full-range of recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON}	Switch-on resistance	V_{CC} = 3.3 V ± 10%, See 图 7-4		1	3	Ω
		V_{CC} = 5 V ± 10%, See 图 7-4		0.6	2	
I_{CC}	Average supply current[(1)]	V_{CC} = 3.3 V ± 10%, no load		150	400	µA
		V_{CC} = 5 V ± 10%, no load		300	700	
f_{ST}	Startup frequency	V_{CC} = 2.4 V, See 图 7-4		300		kHz
f_{SW}	D1, D2 Switching frequency	V_{CC} = 3.3 V ± 10%, See 图 7-4	250	360	495	kHz
		V_{CC} = 5 V ± 10%, See 图 7-4	300	410	620	

(1) Average supply current is the current used by SN6501 only. It does not include load current.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r\text{-}D}$	D1, D2 output rise time	V_{CC} = 3.3 V ± 10%, See 图 7-4		70		ns
		V_{CC} = 5 V ± 10%, See 图 7-4		80		
$t_{f\text{-}D}$	D1, D2 output fall time	V_{CC} = 3.3 V ± 10%, See 图 7-4		110		ns
		V_{CC} = 5 V ± 10%, See 图 7-4		60		
t_{BBM}	Break-before-make time	V_{CC} = 3.3 V ± 10%, See 图 7-4		150		ns
		V_{CC} = 5 V ± 10%, See 图 7-4		50		

6.7 Typical Characteristics

TP1 Curves are measured with the Circuit in 图 7-1; whereas, TP1 and TP2 Curves are measured with Circuit in 图 7-3 (T_A = 25°C unless otherwise noted). See 表 9-3 for Transformer Specifications.

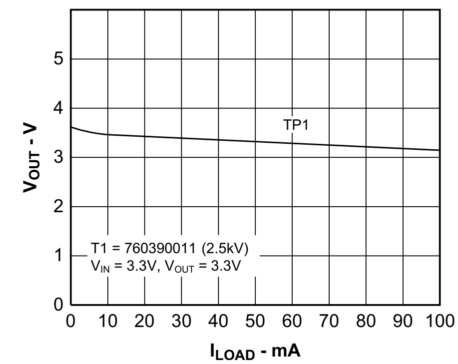


图 6-1. Output Voltage vs Load Current

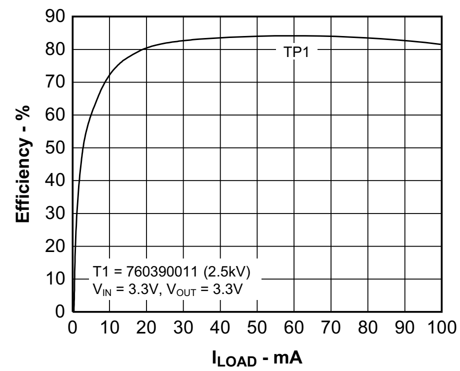


图 6-2. Efficiency vs Load Current

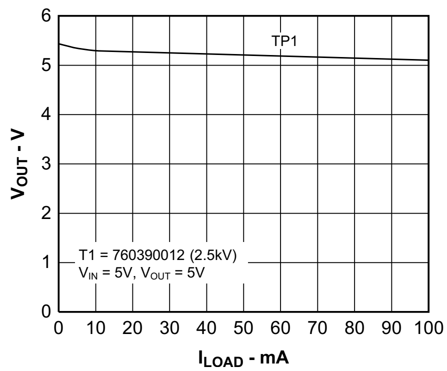


图 6-3. Output Voltage vs. Load Current

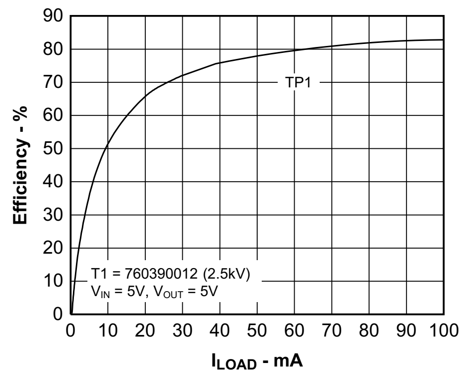


图 6-4. Efficiency vs Load Current

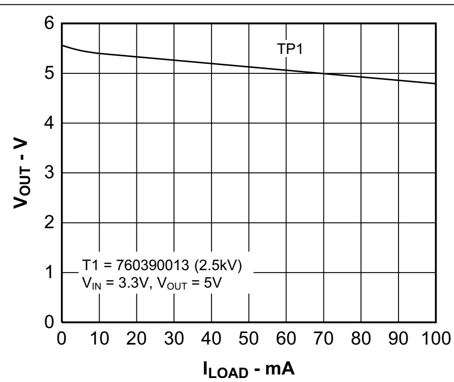


图 6-5. Output Voltage vs Load Current

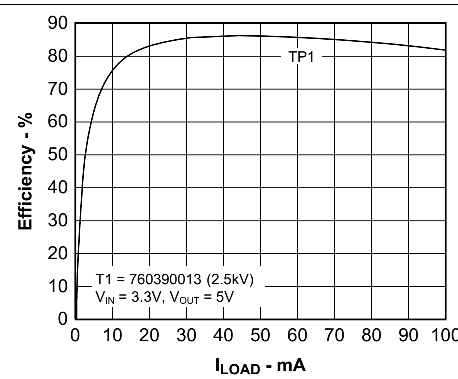


图 6-6. Efficiency vs Load Current

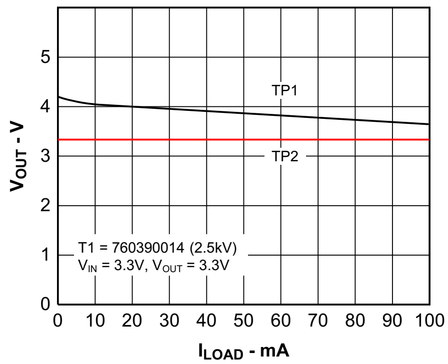


图 6-7. Output Voltage vs Load Current

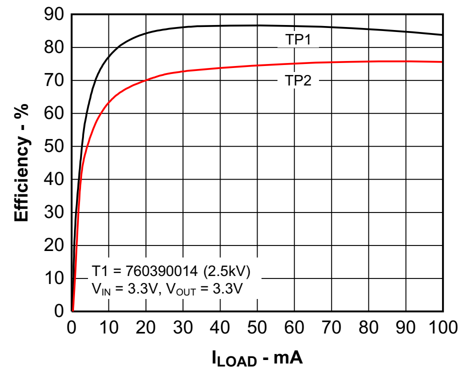


图 6-8. Efficiency vs Load Current

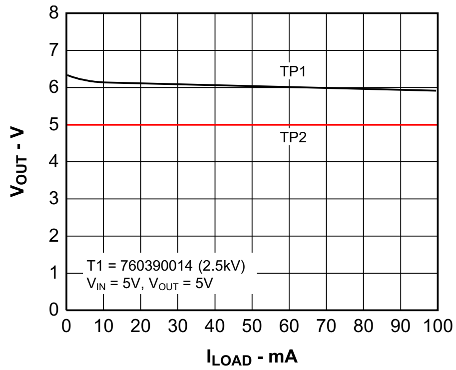


图 6-9. Output Voltage vs Load Current

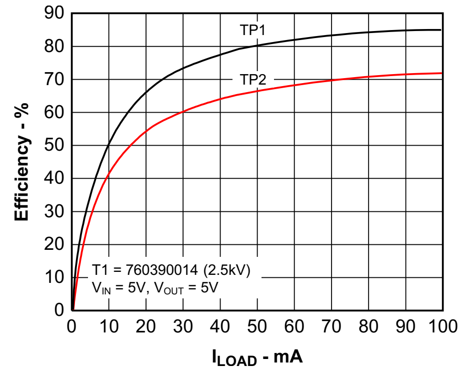


图 6-10. Efficiency vs Load Current

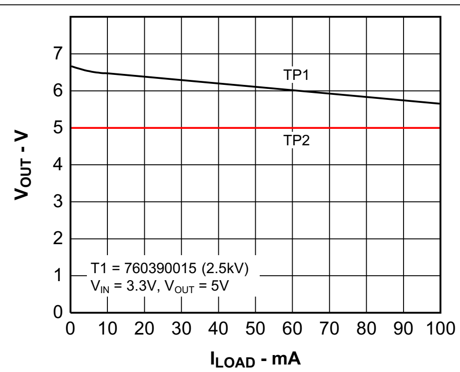


图 6-11. Output Voltage vs Load Current

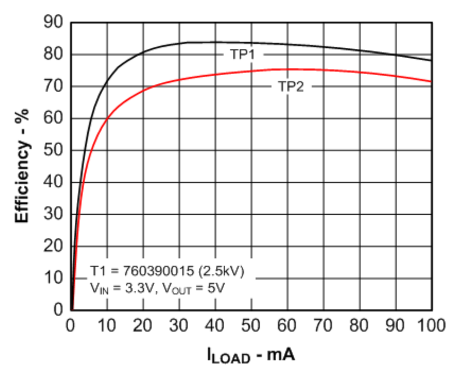


图 6-12. Efficiency vs Load Current

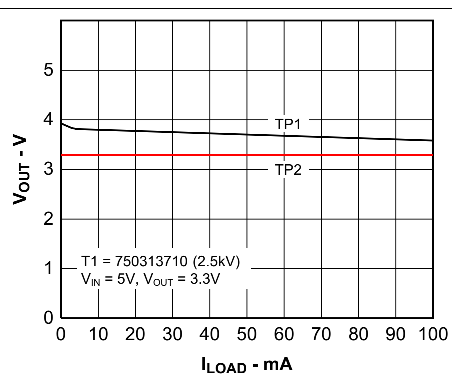


图 6-13. Output Voltage vs Load Current

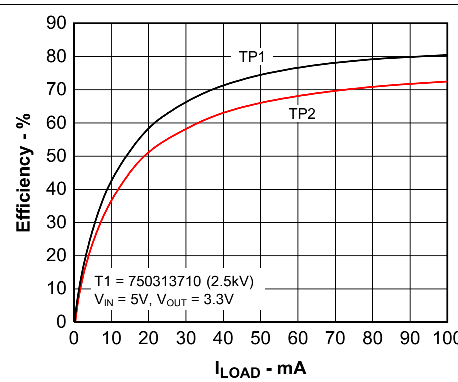


图 6-14. Efficiency vs Load Current

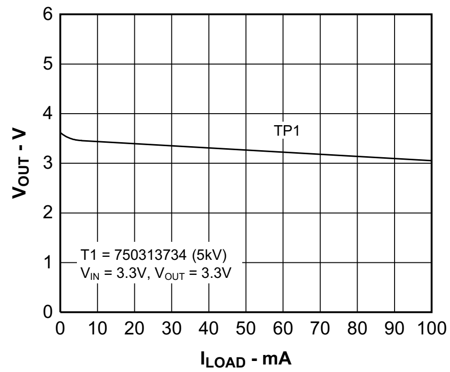


图 6-15. Output Voltage vs Load Current

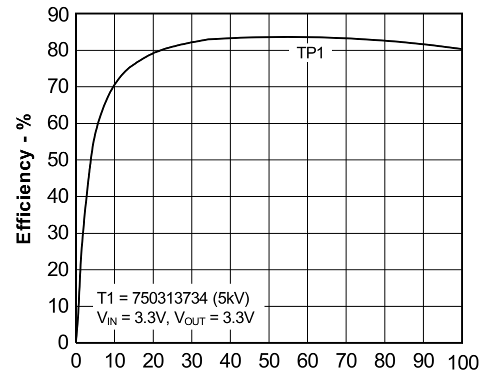


图 6-16. Efficiency vs Load Current

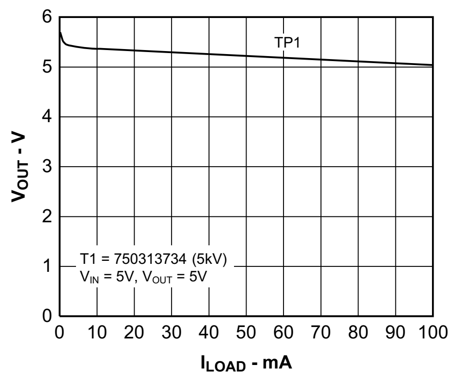


图 6-17. Output Voltage vs Load Current

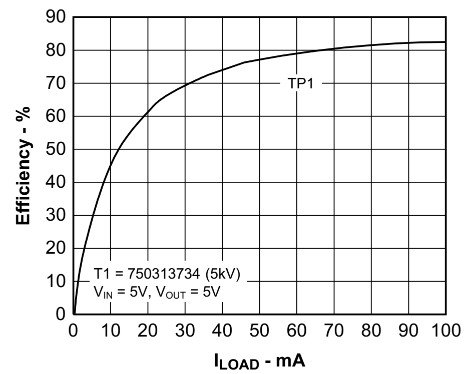


图 6-18. Efficiency vs Load Current

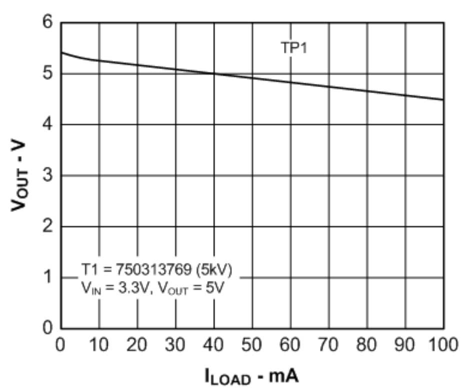


图 6-19. Output Voltage vs Load Current

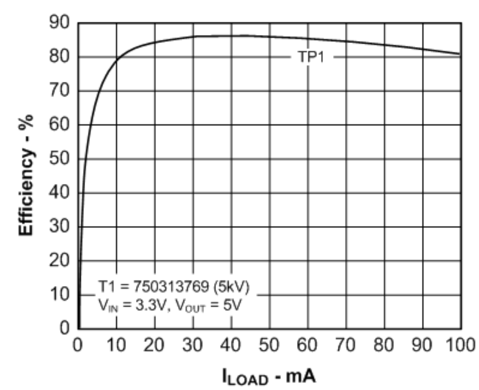


图 6-20. Efficiency vs Load Current

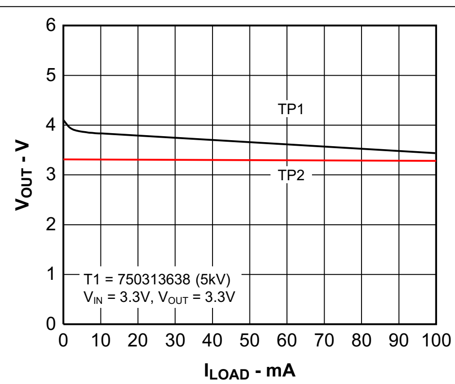


图 6-21. Output Voltage vs Load Current

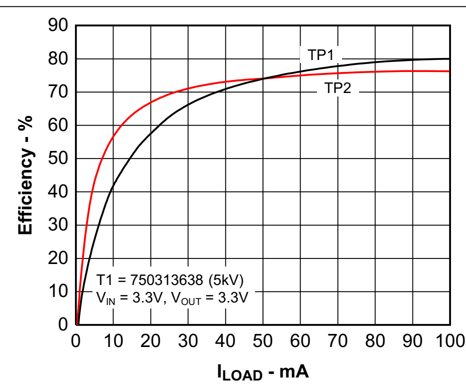


图 6-22. Efficiency vs Load Current

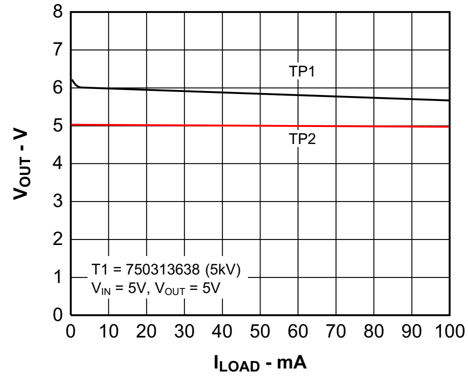


图 6-23. Output Voltage vs Load Current

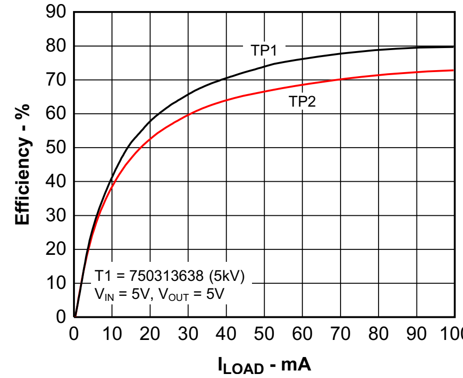


图 6-24. Efficiency vs Load Current

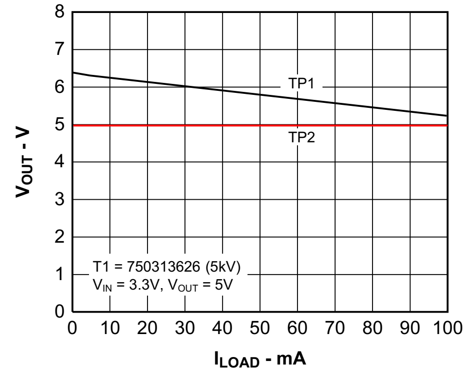


图 6-25. Output Voltage vs Load Current

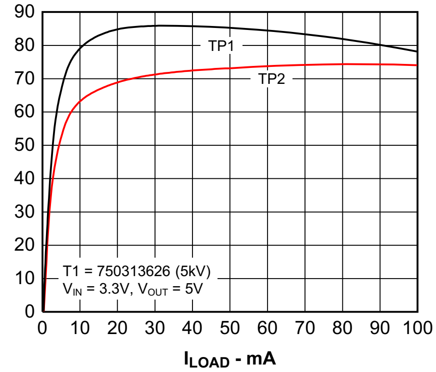


图 6-26. Efficiency vs Load Current

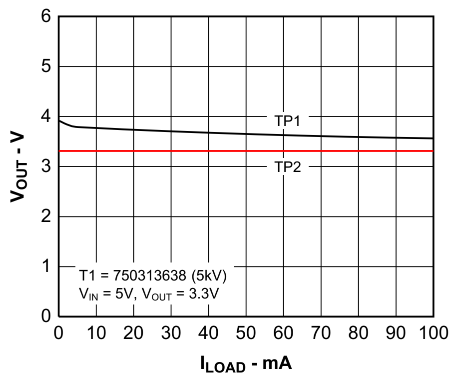


图 6-27. Output Voltage vs Load Current

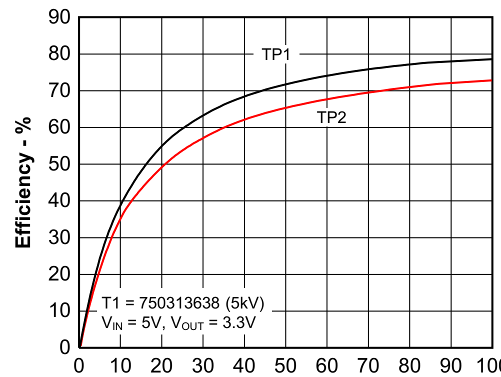


图 6-28. Efficiency vs Load Current

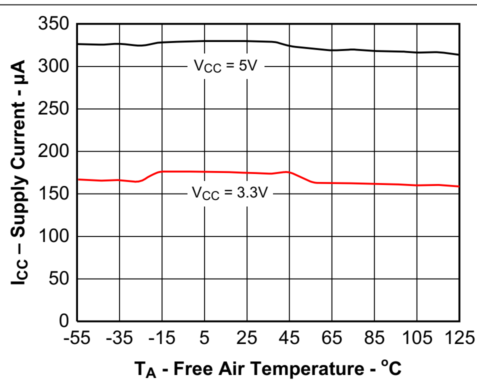


图 6-29. Average Supply Current vs Free-Air Temperature

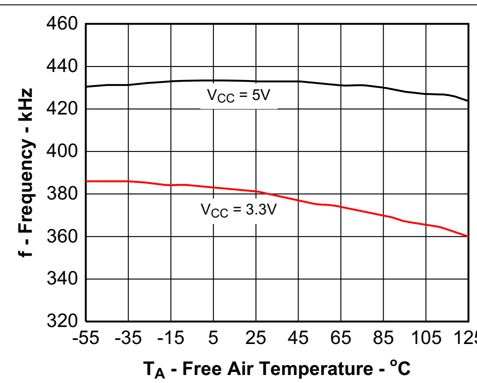


图 6-30. D1, D2 Switching Frequency vs Free-Air Temperature

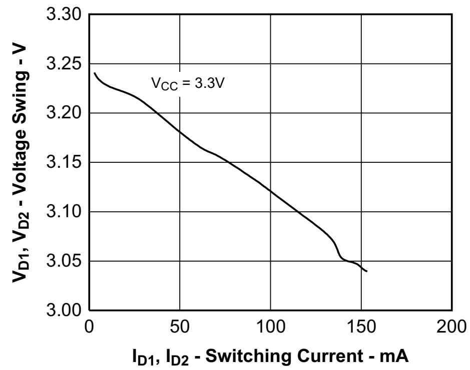


图 6-31. D1, D2 Primary-Side Output Switch Voltage Swing vs Current

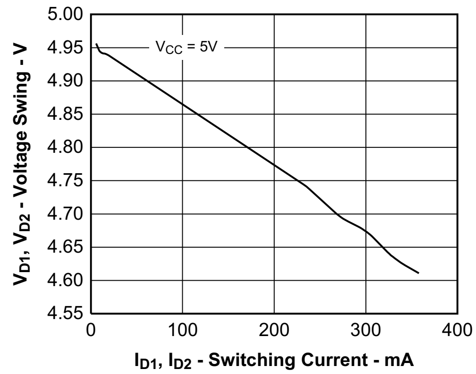


图 6-32. D1, D2 Primary-Side Output Switch Voltage Swing vs Current

7 Parameter Measurement Information

7.1

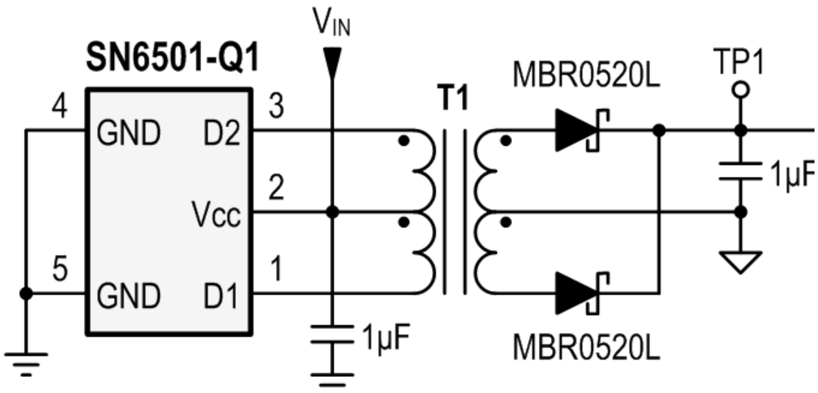


图 7-1. Measurement Circuit for Unregulated Output (TP1)

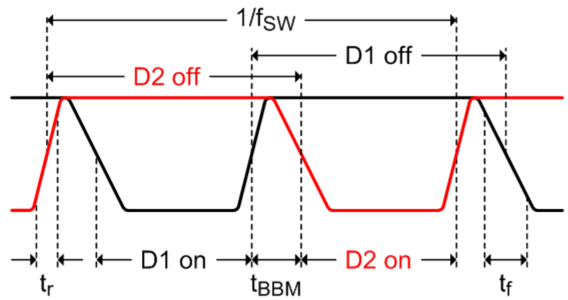


图 7-2. Timing Diagram

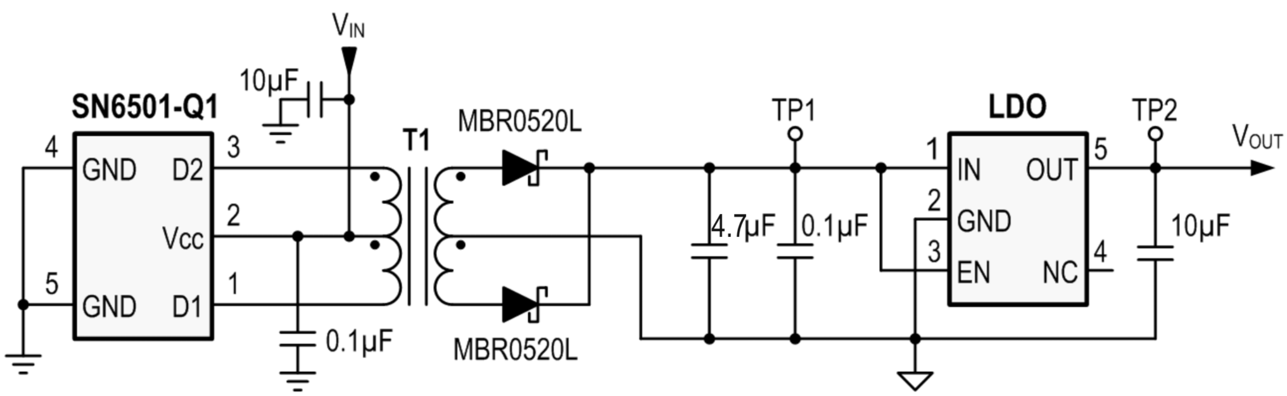


图 7-3. Measurement Circuit for regulated Output (TP1 and TP2)

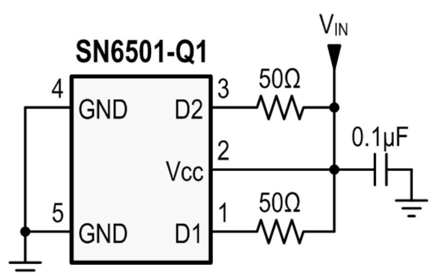


图 7-4. Test Circuit For R_{ON}, F_{SW}, F_{St}, $T_{r\text{-}D}$, $T_{f\text{-}D}$, T_{BBM}

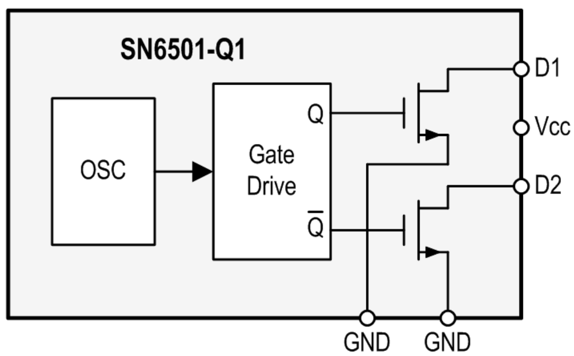
8 Detailed Description

8.1 Overview

The SN6501-Q1 is a transformer driver designed for low-cost, small form-factor, isolated DC-DC converters utilizing the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.

The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals with a 50% duty cycle. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. The resulting output signals, present the gate-drive signals for the output transistors. As shown in the functional block diagram, before either one of the gates can assume logic high, there must be a short time period during which both signals are low and both transistors are high-impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary (see 图 8-1).

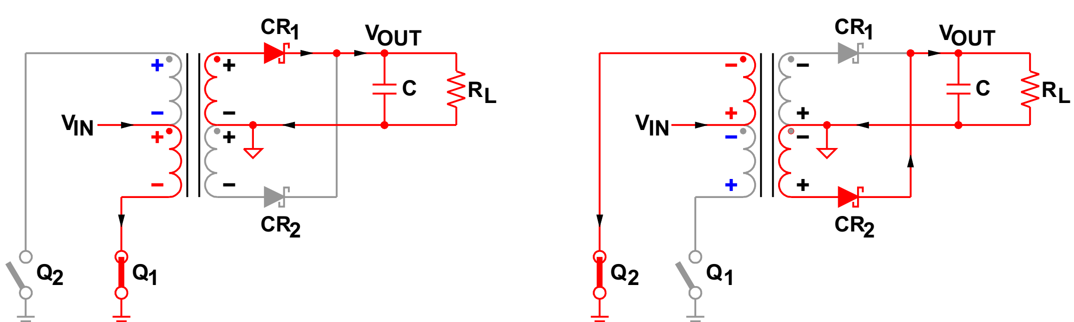


图 8-1. Switching Cycles of a Push-Pull Converter

When Q_1 conducts, V_{IN} drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the V_{IN} potential at the center-tap.

At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap in order to maintain the previously established current flow through Q_2, which now has turned high-impedance. The two voltage sources, each of which equaling V_{IN}, appear in series and cause a voltage potential at the open end of the primary of $2 \times V_{IN}$ with regards to ground.

Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode CR_1. The secondary current starting from the upper secondary end flows through CR_1, charges capacitor C, and returns through the load impedance R_L back to the center-tap.

When Q_2 conducts, Q_1 goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a $2 \times V_{IN}$ potential against ground. In this case CR_2 is forward biased while CR_1 is reverse biased and current flows from the lower secondary end through CR_2, charging the capacitor and returning through the load to the center-tap.

8.3.2 Core Magnetization

图 8-2 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q_1 conducts the magnetic flux is pushed from A to A’, and when Q_2 conducts the flux is pulled back from A’ to A. The difference in flux and thus in flux density is proportional to the product of the primary voltage, V_P, and the time, t_{ON}, it is applied to the primary: $B \approx V_P \times t_{ON}$.

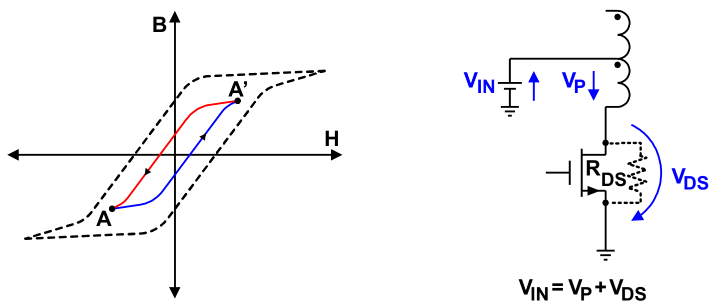


图 8-2. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of $R_{DS(on)}$

This volt-seconds (V-t) product is important as it determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

Fortunately, due to the positive temperature coefficient of a MOSFET’s on-resistance, the output FETs of the SN6501 have a self-correcting effect on V-t imbalance. In the case of a slightly longer on-time, the prolonged current flow through a FET gradually heats the transistor which leads to an increase in $R_{DS\text{-}on}$. The higher resistance then causes the drain-source voltage, V_{DS}, to rise. Because the voltage at the primary is the difference between the constant input voltage, V_{IN}, and the voltage drop across the MOSFET, $V_P = V_{IN} - V_{DS}$, V_P is gradually reduced and V-t balance restored.

8.4 Device Functional Modes

The functional modes of the SN6501 are divided into start-up, operating, and off-mode.

8.4.1 Start-Up Mode

When the supply voltage at Vcc ramps up to 2.4V typical, the internal oscillator starts operating at a start frequency of 300 kHz. The output stage begins switching but the amplitude of the drain signals at D1 and D2 has not reached its full maximum yet.

8.4.2 Operating Mode

When the device supply has reached its nominal value ±10% the oscillator is fully operating. However variations over supply voltage and operating temperature can vary the switching frequencies at D1 and D2 between 250 kHz and 495 kHz for V_{CC} = 3.3 V ±10%, and between 300 kHz and 620 kHz for V_{CC} = 5 V ±10%.

8.4.3 Off-Mode

The SN6501 is deactivated by reducing V_{CC} to 0 V. In this state both drain outputs, D1 and D2, are high-impedance.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN6501-Q1 is a transformer driver designed for low-cost, small form-factor, isolated DC-DC converters utilizing the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.

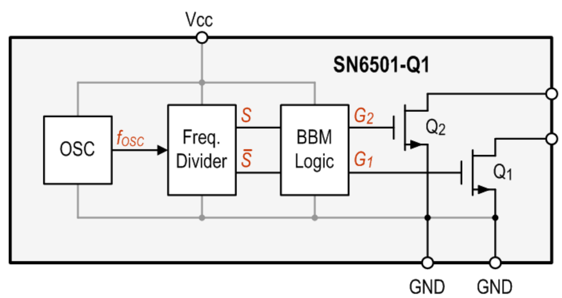


图 9-1. SN6501-Q1 Block Diagram

The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals, S and $\overline{S}$, with a 50% duty cycle. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. The resulting output signals, G_1 and G_2, present the gate-drive signals for the output transistors Q_1 and Q_2. As shown in 图 9-2, before either one of the gates can assume logic high, there must be a short time period during which both signals are low and both transistors are high-impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.

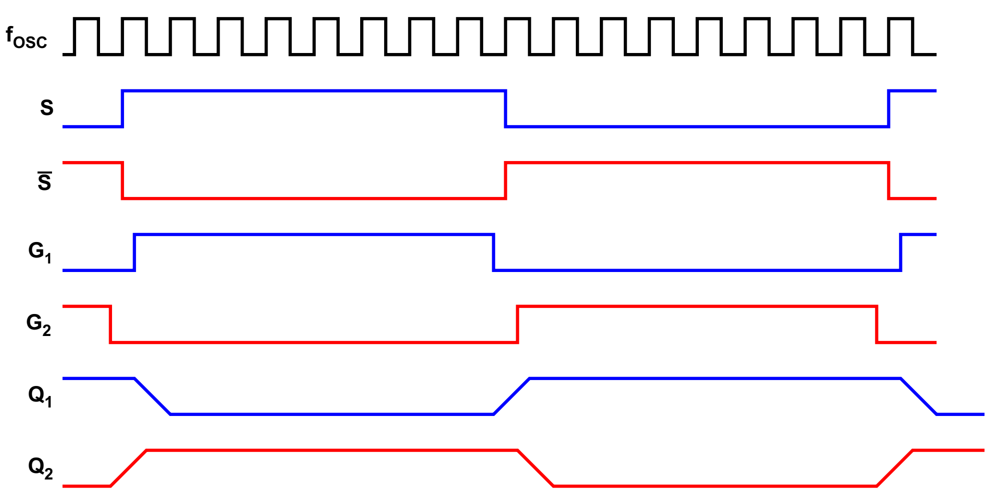


图 9-2. Detailed Output Signal Waveforms

9.2 Typical Application

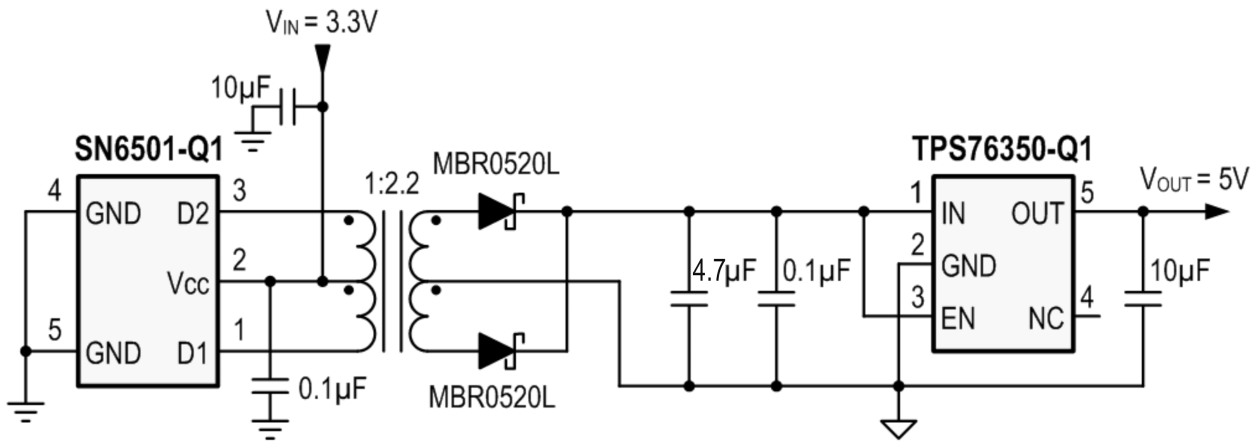


图 9-3. Typical Application Schematic (SN6501-Q1)

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as design parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.3 V ± 3%
Output voltage	5 V
Maximum load current	100 mA

9.2.2 Detailed Design Procedure

The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Contrary to popular belief, the output voltage of the unregulated converter output drops significantly over a wide range in load current. The characteristic curve in 图 6-11 for example shows that the difference between V_{OUT} at minimum load and V_{OUT} at maximum load exceeds a transceiver's supply range. Therefore, in order to provide a stable, load independent supply while maintaining maximum possible efficiency the implementation of a low dropout regulator (LDO) is strongly advised.

The final converter circuit is shown in 图 9-7. The measured V_{OUT} and efficiency characteristics for the regulated and unregulated outputs are shown in 图 6-1 to 图 6-28.

9.2.2.1 SN6501 Drive Capability

The SN6501 transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 3 V to 5.5 V. While converter designs with higher output voltages are possible, care must be taken that higher turns ratios don't lead to primary currents that exceed the SN6501 specified current limits.

Unlike SN6505 devices, SN6501 does not have soft-start, internal current limit, or thermal shutdown (TSD) features. Therefore, unregulated large currents exceeding device absolute maximum current ratings may damage the device or affect its long-term reliability. In addition, high capacitive loads at the isolated power supply output may appear as short circuits to SN6501 during power-up and may exceed the device's maximum current ratings. When using SN6501, it is recommended to incorporate LDOs with low short-circuit current limits or soft-start features to ensure excessive current is not drawn from SN6501.

9.2.2.2 LDO Selection

The minimum requirements for a suitable low dropout regulator are:

- Its current drive capability should slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore for a load current of 100 mA, choose a 100 mA to 150 mA LDO. While regulators with higher drive capabilities are acceptable, they also usually possess higher dropout voltages that will reduce overall converter efficiency.
- The internal dropout voltage, V_{DO}, at the specified load current should be as low as possible to maintain efficiency. For a low-cost 150 mA LDO, a V_{DO} of 150 mV at 100 mA is common. Be aware however, that this lower value is usually specified at room temperature and can increase by a factor of 2 over temperature, which in turn will raise the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max} \quad (1)$$

  This means in order to determine V_I for worst-case condition, the user must take the maximum values for V_{DO} and V_O specified in the LDO data sheet for rated output current (i.e., 100 mA) and add them together. Also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than $V_{I\text{-}min}$. If it is not, the LDO will lose line-regulation and any variations at the input will pass straight through to the output. Hence below $V_{I\text{-}min}$ the output voltage will follow the input and the regulator behaves like a simple conductor.
- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across $R_{DS\text{-}on}$ negligible and allowing the entire converter input voltage to drop across the primary. At this point the secondary reaches its maximum voltage of

$$V_{S\text{-}max} = V_{IN\text{-}max} \times n \quad (2)$$

with $V_{IN\text{-}max}$ as the maximum converter input voltage and n as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than $V_{S\text{-}max}$. 表 9-2 lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters with 100 mA output drive.

表 9-2. Required Maximum LDO Input Voltages for Various Push-Pull Configurations

PUSH-PULL CONVERTER				LDO
CONFIGURATION	$V_{IN\text{-}max}$ [V]	TURNS-RATIO	$V_{S\text{-}max}$ [V]	$V_{I\text{-}max}$ [V]
3.3 V_{IN} to 3.3 V_{OUT}	3.6	1.5 ± 3%	5.6	6 to 10
3.3 V_{IN} to 5 V_{OUT}	3.6	2.2 ± 3%	8.2	10
5 V_{IN} to 5 V_{OUT}	5.5	1.5 ± 3%	8.5	10

9.2.2.3 Diode Selection

A rectifier diode should always possess low-forward voltage to provide as much voltage to the converter output as possible. When used in high-frequency switching applications, such as the SN6501 however, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs. A good choice for low-volt applications and ambient temperatures of up to 85°C is the low-cost Schottky rectifier MBR0520L with a typical forward voltage of 275 mV at 100-mA forward current. For higher output voltages such as ±10 V and above use the MBR0530 which provides a higher DC blocking voltage of 30 V.

Lab measurements have shown that at temperatures higher than 100°C the leakage currents of the above Schottky diodes increase significantly. This can cause thermal runaway leading to the collapse of the rectifier output voltage. Therefore, for ambient temperatures higher than 85°C use low-leakage Schottky diodes, such as RB168M-40.

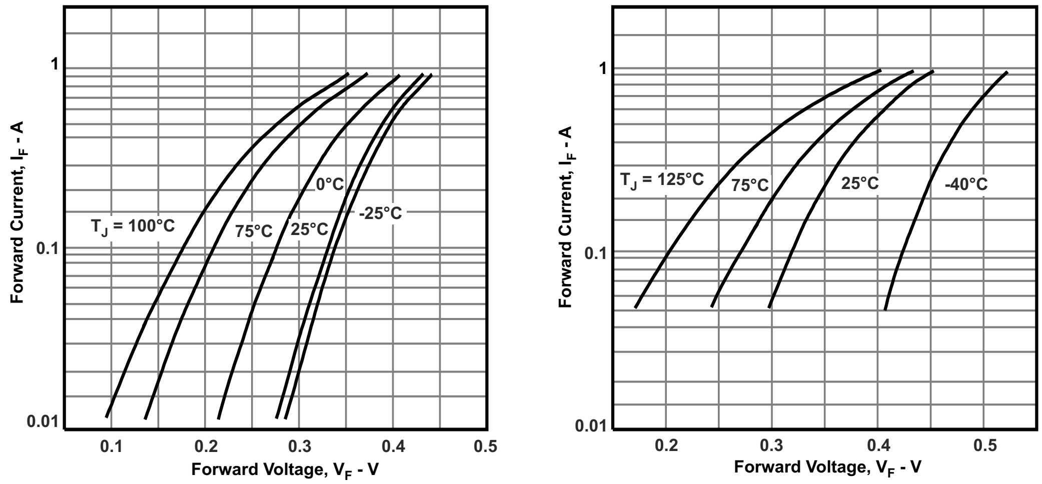


图 9-4. Diode Forward Characteristics for MBR0520L (Left) and MBR0530 (Right)

9.2.2.4 Capacitor Selection

The capacitors in the converter circuit in 图 9-7 are multi-layer ceramic chip (MLCC) capacitors.

As with all high speed CMOS ICs, the SN6501 requires a bypass capacitor in the range of 10 nF to 100 nF.

The input bulk capacitor at the center-tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple make this capacitor 1 μF to 10 μF. In a 2-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layer board design with low-inductance reference planes for ground and V_{IN}, the capacitor can be placed at the supply entrance of the board. To ensure low-inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smoothes the output voltage. Make this capacitor 1 μF to 10 μF.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47 nF to 100 nF improves the regulator's transient response and noise rejection.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7 μF to 10 μF will satisfy these requirements.

9.2.2.5 Transformer Selection

9.2.2.5.1 V-t Product Calculation

To prevent a transformer from saturation its V-t product must be greater than the maximum V-t product applied by the SN6501. The maximum voltage delivered by the SN6501 is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined through:

$$Vt_{min} \geq V_{IN\text{-}max} \times \frac{T_{max}}{2} = \frac{V_{IN\text{-}max}}{2 \times f_{min}} \tag{3}$$

Inserting the numeric values from the data sheet into the equation above yields the minimum V-t products of

$$Vt_{min} \geq \frac{3.6\ V}{2 \times 250\ kHz} = 7.2\ V\mu s \quad \text{for 3.3 V, and}$$

$$Vt_{min} \geq \frac{5.5\ V}{2 \times 300\ kHz} = 9.1\ V\mu s \quad \text{for 5 V applications.} \tag{4}$$

Common V-t values for low-power center-tapped transformers range from 22 Vμs to 150 Vμs with typical footprints of 10 mm x 12 mm. However, transformers specifically designed for PCMCIA applications provide as little as 11 Vμs and come with a significantly reduced footprint of 6 mm x 6 mm only.

While Vt-wise all of these transformers can be driven by the SN6501, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

9.2.2.5.2 Turns Ratio Estimate

Assume the rectifier diodes and linear regulator has been selected. Also, it has been determined that the transformer choosen must have a V-t product of at least 11 Vμs. However, before searching the manufacturer websites for a suitable transformer, the user still needs to know its minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer's typical efficiency of 97% into account.

$$n_{min} = 1.031 \times \frac{V_{s-min}}{V_{p-min}} \quad (5)$$

$V_{S\text{-}min}$ must be large enough to allow for a maximum voltage drop, $V_{F\text{-}max}$, across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the LDO SELECTION section, this minimum input voltage is known and by adding $V_{F\text{-}max}$ gives the minimum secondary voltage with:

$$V_{S\text{-}min} = V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max} \quad (6)$$

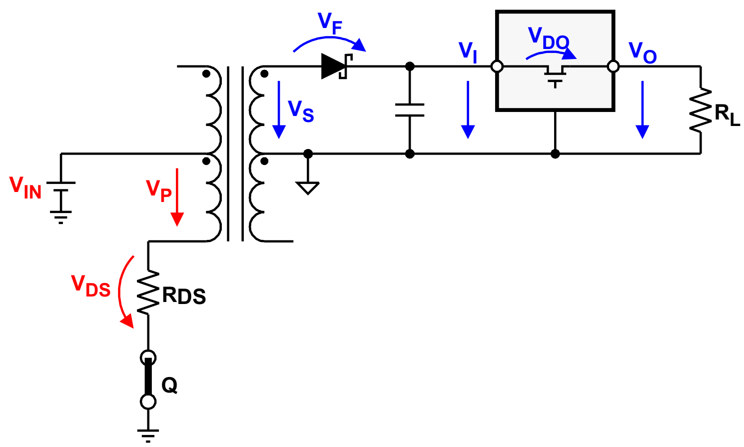


图 9-5. Establishing the Required Minimum Turns Ratio Through $N_{min} = 1.031 \times V_{S\text{-}min} / V_{P\text{-}min}$

Then calculating the available minimum primary voltage, $V_{P\text{-}min}$, involves subtracting the maximum possible drain-source voltage of the SN6501, $V_{DS\text{-}max}$, from the minimum converter input voltage $V_{IN\text{-}min}$:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max} \quad (7)$$

$V_{DS\text{-}max}$ however, is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the SN6501 data sheet:

$$V_{DS\text{-}max} = R_{DS\text{-}max} \times I_{Dmax} \quad (8)$$

Then inserting 方程式 8 into 方程式 7 yields:

$$V_{P\text{-}min} = V_{IN\text{-}min} - R_{DS\text{-}max} \times I_{Dmax} \quad (9)$$

and inserting 方程式 9 and 方程式 6 into 方程式 5 provides the minimum turns ration with:

$$n_{min} = 1.031 \times \frac{V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max}}{V_{IN\text{-}min} - R_{DS\text{-}max} \times I_{D\text{-}max}} \quad (10)$$

Example:

For a 3.3 V_{IN} to 5 V_{OUT} converter using the rectifier diode MBR0520L and the 5 V LDO TPS76350, the data sheet values taken for a load current of 100 mA and a maximum temperature of 85°C are $V_{F\text{-}max}$ = 0.2 V, $V_{DO\text{-}max}$ = 0.2 V, and $V_{O\text{-}max}$ = 5.175 V.

Then assuming that the converter input voltage is taken from a 3.3 V controller supply with a maximum ±2% accuracy makes $V_{IN\text{-}min}$ = 3.234 V. Finally the maximum values for drain-source resistance and drain current at 3.3 V are taken from the SN6501 data sheet with $R_{DS\text{-}max}$ = 3 Ω and $I_{D\text{-}max}$ = 150 mA.

Inserting the values above into 方程式 10 yields a minimum turns ratio of:

$$n_{min} = 1.031 \times \frac{0.2V + 0.2V + 5.175\ V}{3.234\ V - 3\ \Omega \times 150\ mA} = 2 \tag{11}$$

Most commercially available transformers for 3-to-5 V push-pull converters offer turns ratios between 2.0 and 2.3 with a common tolerance of ±3%.

9.2.2.5.3 Recommended Transformers

Depending on the application, use the minimum configuration in 图 9-6 or standard configuration in 图 9-7.

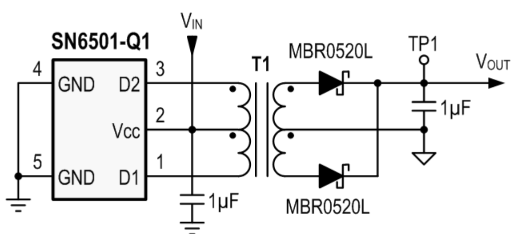


图 9-6. Unregulated Output for Low-Current Loads With Wide Supply Range

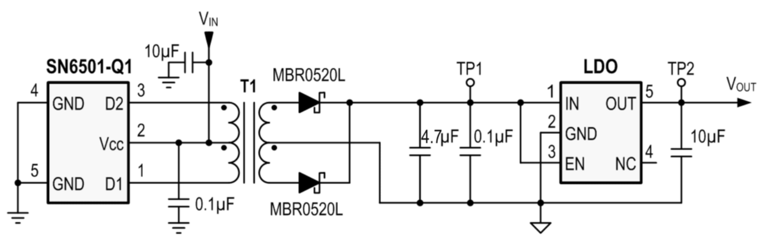


图 9-7. Regulated Output for Stable Supplies and High Current Loads

The Wurth Electronics Midcom isolation transformers in 表 9-3 are optimized designs for the SN6501, providing high efficiency and small form factor at low-cost.

The 1:1.1 and 1:1.7 turns-ratios are designed for logic applications with wide supply rails and low load currents. These applications operate without LDO, thus achieving further cost-reduction.

表 9-3. Recommended Isolation Transformers Optimized for SN6501

Turns Ratio	V x T (V µ s)	Isolation (V_{RMS})	Dimensions (mm)	Application	LDO	Figures	Order No.	Manufacturer
1:1.1 ±2%	7			3.3 V → 3.3 V		图 6-1 图 6-2	760390011	
1:1.1 ±2%				5 V → 5 V	No	图 6-3 图 6-4	760390012	
1:1.7 ±2%				3.3 V → 5 V		图 6-5 图 6-6	760390013	
1:1.3 ±2%	11	2500	6.73 x 10.05 x 4.19	3.3 V → 3.3 V 5 V → 5 V		图 6-7 图 6-8 图 6-9 图 6-10	760390014	
1:2.1 ±2%				3.3 V → 5 V	Yes	图 6-11 图 6-12	760390015	
1.23:1 ±2%				5 V → 3.3 V		图 6-13 图 6-14	750313710	Wurth Electronics/ Midcom
1:1.1 ±2%				3.3 V → 3.3 V		图 6-15 图 6-16	750313734	
1:1.1 ±2%				5 V → 5 V	No	图 6-17 图 6-18	750313734	
1:1.7 ±2%				3.3 V → 5 V		图 6-19 图 6-20	750313769	
1:1.3 ±2%	11	5000	9.14 x 12.7 x 7.37	3.3 V → 3.3 V 5 V → 5 V		图 6-21 图 6-22 图 6-23 图 6-24	750313638	
1:2.1 ±2%				3.3 V → 5 V	Yes	图 6-25 图 6-26	750313626	
1.3:1 ±2%				5 V → 3.3 V		图 6-27 图 6-28	750313638	

表 9-3. Recommended Isolation Transformers Optimized for SN6501 (continued)

Turns Ratio	V x T (V µs)	Isolation (V_{RMS})	Dimensions (mm)	Application	LDO	Figures	Order No.	Manufacturer
1:1.1 ±2%	7	1500	7.1 x 11 x 4.19	3.3 V → 3.3V	No	N/A	EPC3804G-L	PCA Electronics
1:1.1 ±2%	11	2500		5V → 5V	No	N/A	EPC3805G-L	
1:1.7 ±2%	11			3.3V → 5V 3.3V → 3.3V	No / Yes	N/A	EPC3806G-L	
1:1.3 ±2%	11			3.3V → 3.3V 5V → 5V	Yes	N/A	EPC3807G-L	
1:2 ±2%	11			3.3V → 5V	Yes	N/A	EPC3808G-L	
1:1.1 ±2%	4.3		8.6 x 12.5 x 5.97	5V → 5V	No	N/A	EPC3809G-L	
1:1	11	4200	10.8 x 15.2 x 6.6	3.3V → 3.3V 5V → 5V	No	N/A	HCTSM80101AAL	Bourns
1:2				3.3V → 5V	Yes	N/A	HCTSM80102AAL	
2:1				5V → 1.8V	Yes	N/A	HCTSM80201AAL	
3:4				3.3V → 3.3V 5V → 5V	Yes	N/A	HCTSM80304BAL	
3:5				3.3V → 5V	No	N/A	HCTSM80305BAL	
3:8				5V → 12V	Yes	N/A	HCTSM80308BAL	
4:3				5V → 3.3V	No	N/A	HCTSM80403AAL	
8:3				5V → 1.8V	No	N/A	HCTSM80803AAL	
8:9				3.3V → 3.3V 5V → 5V	No	N/A	HCTSM80809AAL	
9:10						N/A	HCTSM80910BAL	
10:17				3.3V → 5V	Yes	N/A	HCTSM81017CAL	

9.2.3 Application Curve

See 表 9-3 for application curves.

9.2.4 Higher Output Voltage Designs

The SN6501 can drive push-pull converters that provide high output voltages of up to 30 V, or bipolar outputs of up to ±15 V. Using commercially available center-tapped transformers, with their rather low turns ratios of 0.8 to 5, requires different rectifier topologies to achieve high output voltages. 图 9-8 to 图 9-11 show some of these topologies together with their respective open-circuit output voltages.

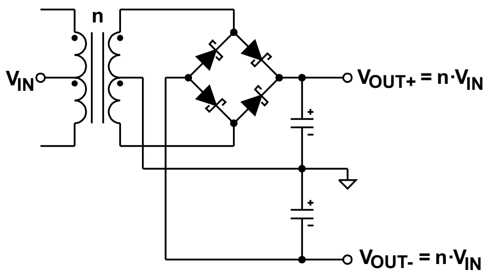


图 9-8. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs

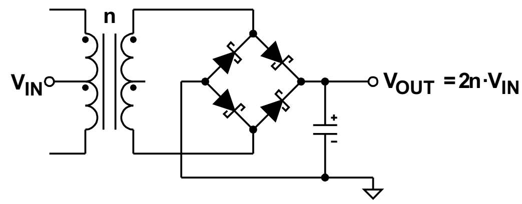


图 9-9. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Doubling

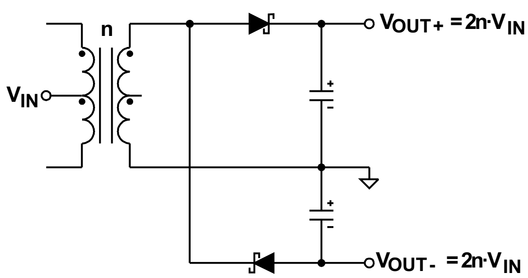


图 9-10. Half-Wave Rectifier Without Center-Tapped Secondary Performs Voltage Doubling, Centered Ground Provides Bipolar Outputs

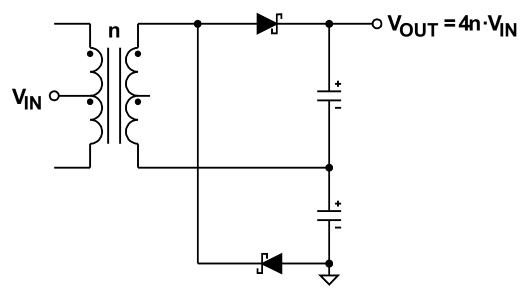


图 9-11. Half-Wave Rectifier Without Centered Ground and Center-Tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling V_{IN}

9.2.5 Application Circuits

The following application circuits are shown for a 3.3 V input supply commonly taken from the local, regulated micro-controller supply. For 5 V input voltages requiring different turn ratios refer to the transformer manufacturers and their websites listed in 表 9-4.

表 9-4. Transformer Manufacturers

Coilcraft Inc.	http://www.coilcraft.com
Halo-Electronics Inc.	http://www.haloelectronics.com
Murata Power Solutions	http://www.murata-ps.com
Wurth Electronics Midcom Inc	http://www.midcom-inc.com

Certain components might not possess AEC-Q100 Q1 qualification. For more detailed information on qualified components for automotive applications please refer to the automotive web page: http://www.ti.com/lsds/ti/apps/automotive/applications.page.

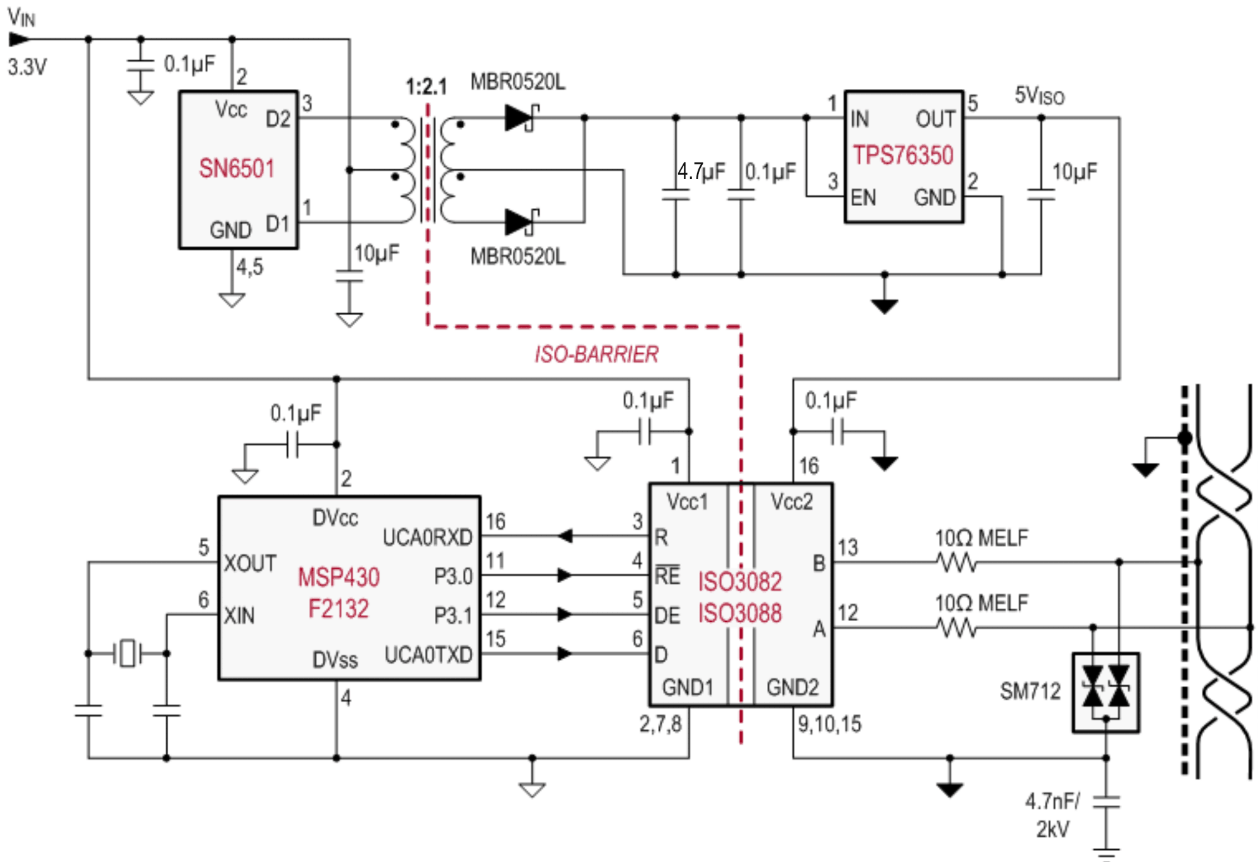


图 9-12. Isolated RS-485 Interface

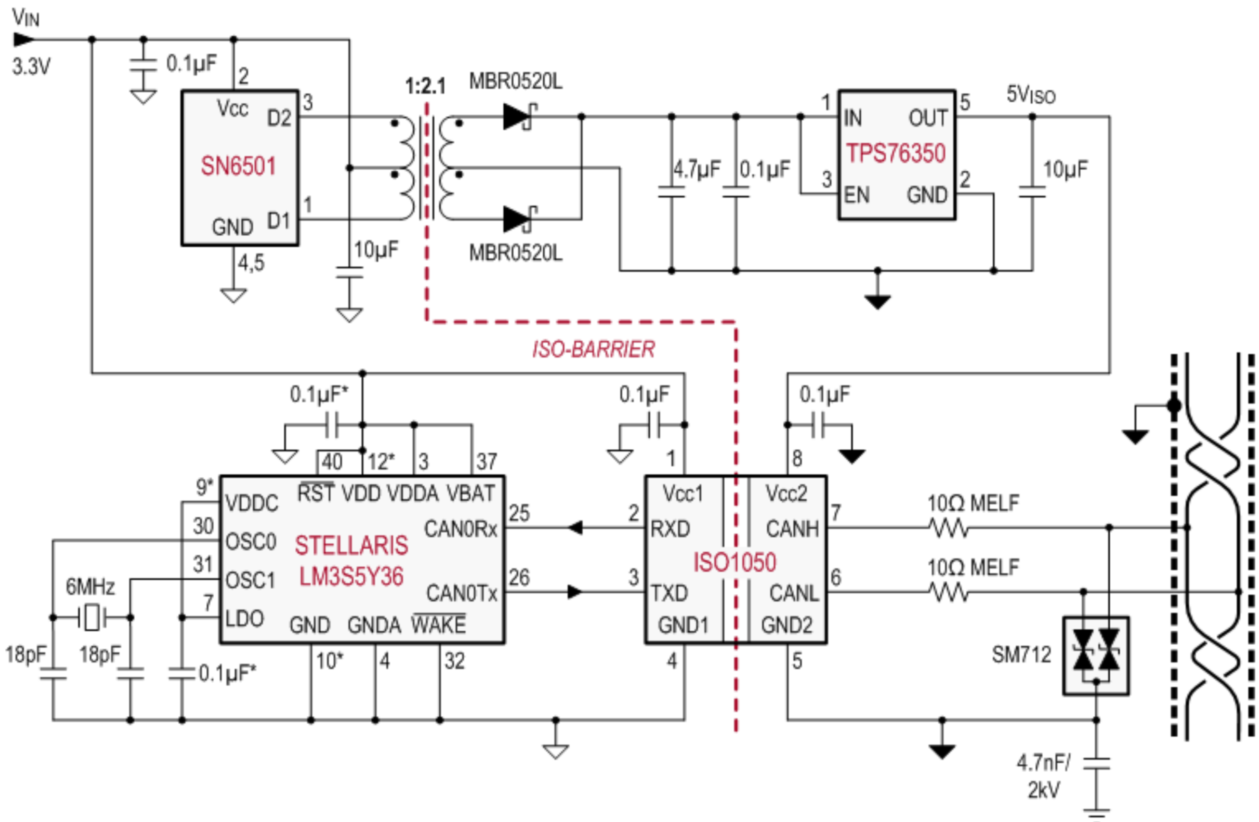


图 9-13. Isolated Can Interface

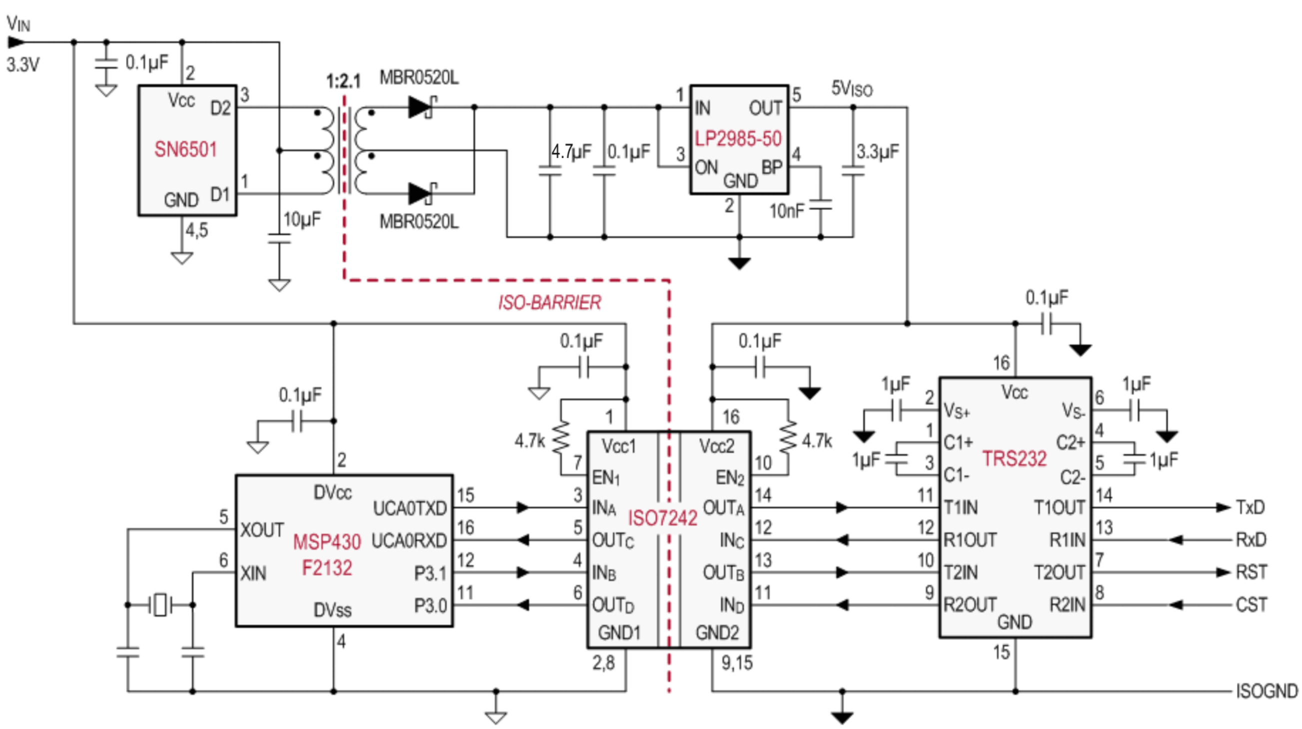


图 9-14. Isolated RS-232 Interface

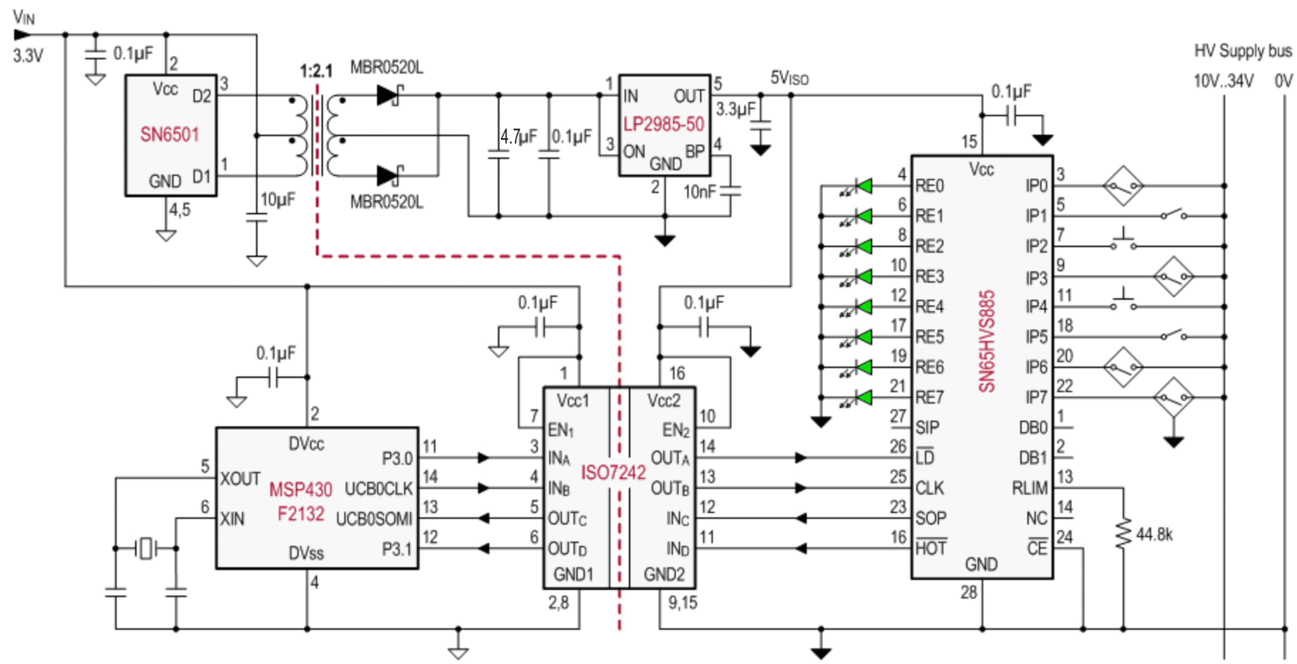


图 9-15. Isolated Digital Input Module

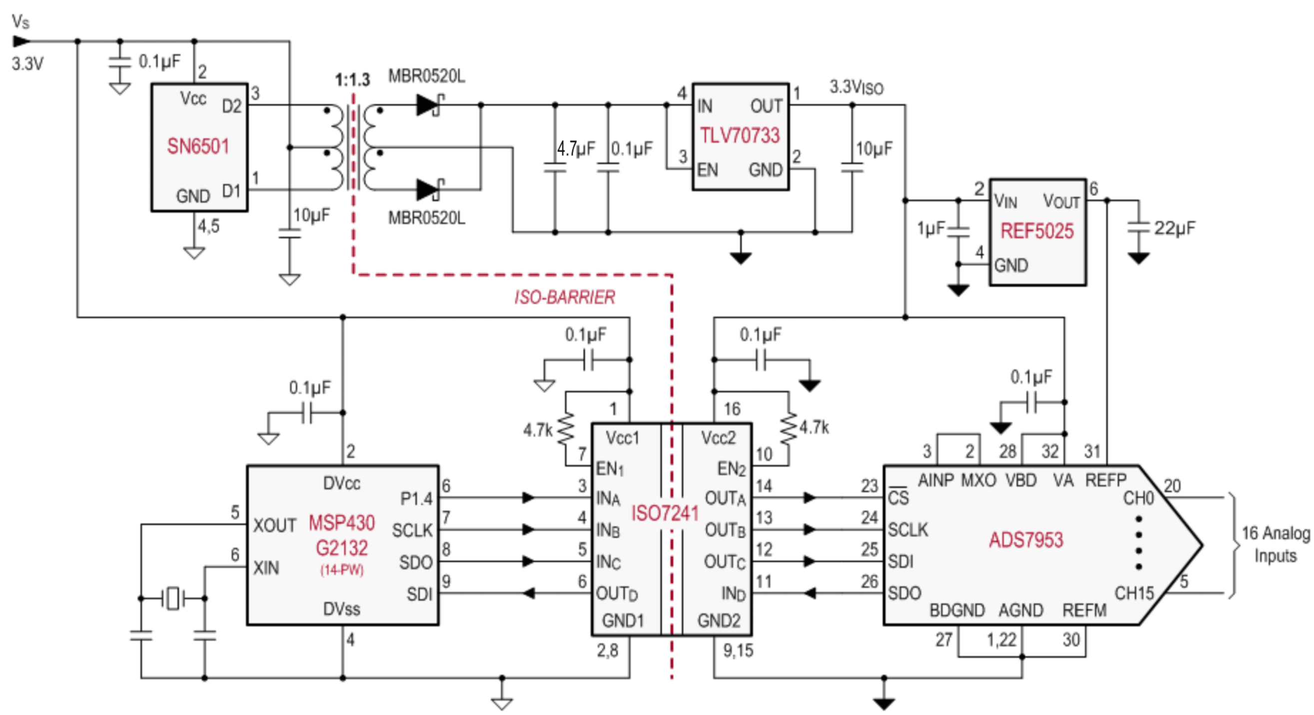


图 9-16. Isolated SPI Interface for an Analog Input Module With 16 Inputs

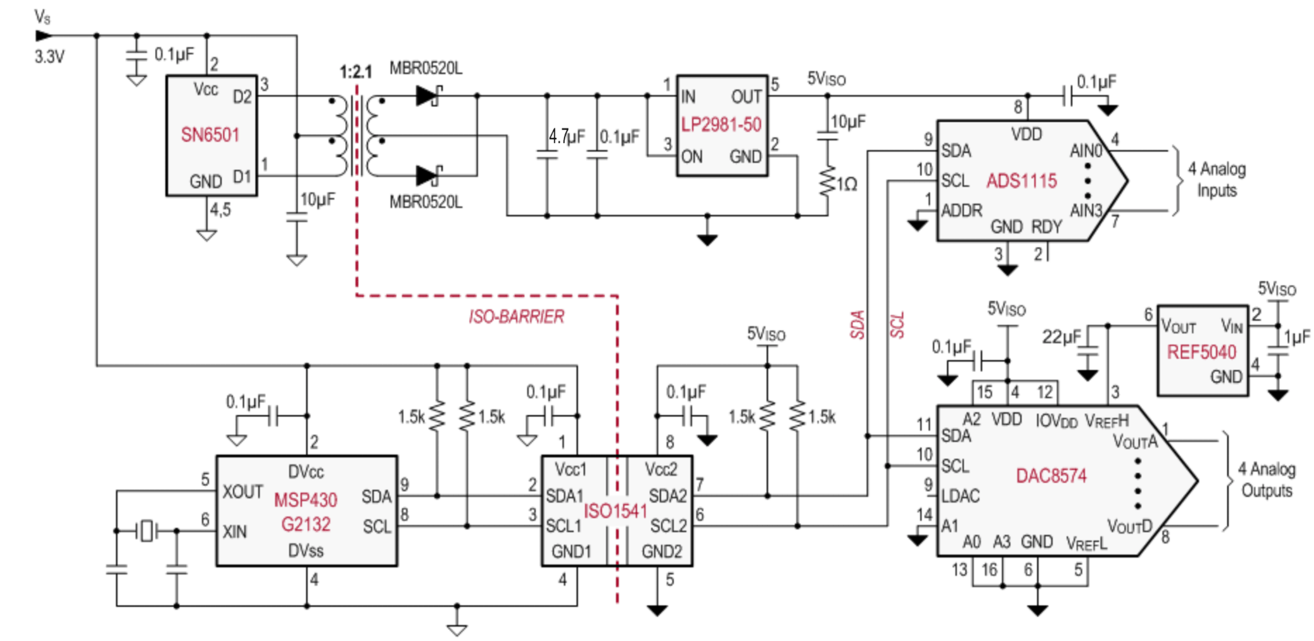


图 9-17. Isolated I^{2}C Interface for an Analog Data Acquisition System With 4 Inputs and 4 Outputs

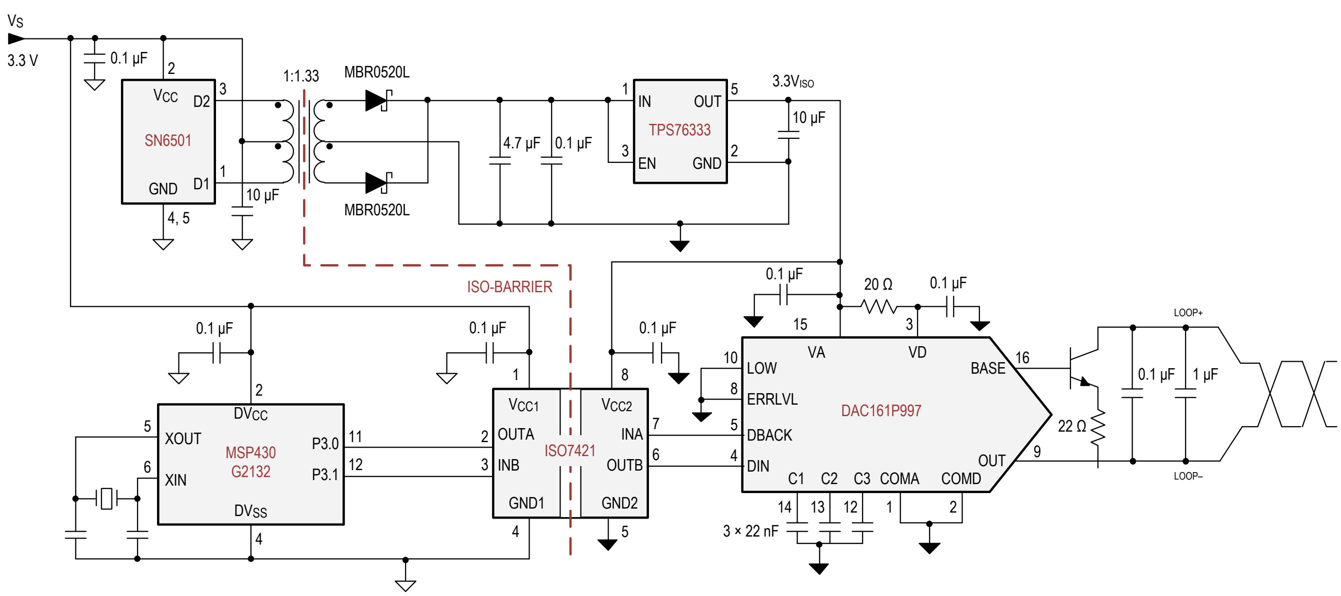


图 9-18. Isolated 4-20 mA Current Loop

10 Power Supply Recommendations

10.1

The device is designed to operate from an input voltage supply range between 3.3 V and 5 V nominal. This input supply must be regulated within ±10%. If the input supply is located more than a few inches from the SN6501 a 0.1 µF by-pass capacitor should be connected as possible to the device V_{CC} pin, and a 10 µF capacitor should be connected close to the transformer center-tap pin.

11 Layout

11.1 Layout Guidelines

- The V_{IN} pin must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 μF to 10 μF. The capacitor must have a voltage rating of 10 V minimum and a X5R or X7R dielectric.
- The optimum placement is closest to the V_{IN} and GND pins at the board entrance to minimize the loop area formed by the bypass-capacitor connection, the V_{IN} terminal, and the GND pin. See 图 11-1 for a PCB layout example.
- The connections between the device D1 and D2 pins and the transformer primary endings, and the connection of the device V_{CC} pin and the transformer center-tap must be as close as possible for minimum trace inductance.
- • The connection of the device V_{CC} pin and the transformer center-tap must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 μF to 10 μF. The capacitor must have a voltage rating of 16 V minimum and a X5R or X7R dielectric.
- The device GND pins must be tied to the PCB ground plane using two vias for minimum inductance.
- The ground connections of the capacitors and the ground plane should use two vias for minimum inductance.
- The rectifier diodes should be Schottky diodes with low forward voltage in the 10 mA to 100 mA current range to maximize efficiency.
- The V_{OUT} pin must be buffered to ISO-Ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 μF to 10 μF. The capacitor must have a voltage rating of 16 V minimum and a X5R or X7R dielectric.

11.2 Layout Example

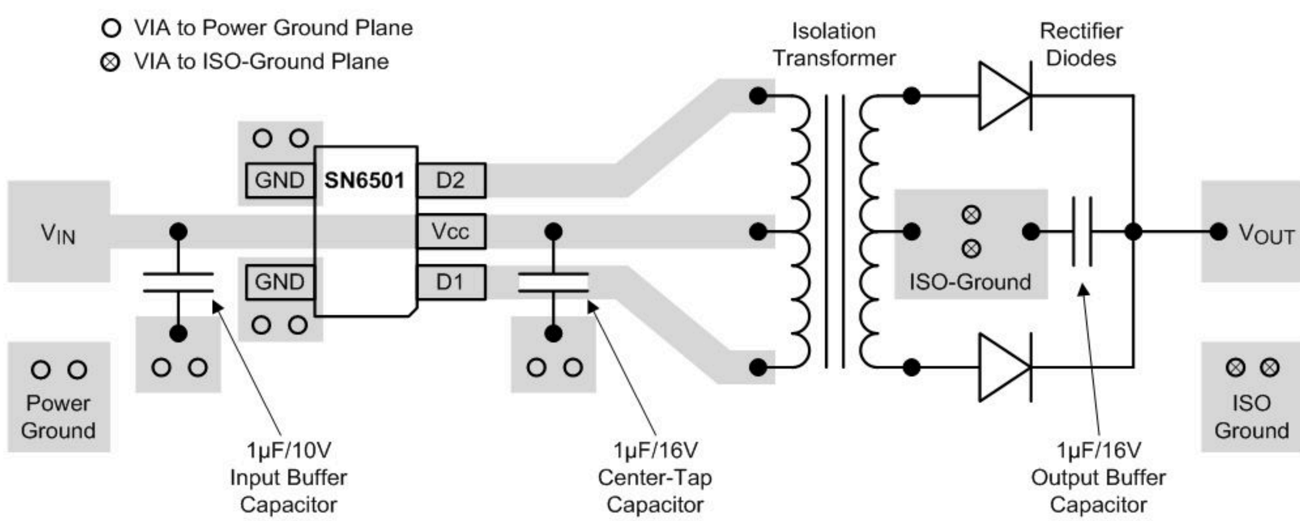


图 11-1. Layout Example of a 2-Layer Board (SN6501)

12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.2 Trademarks

所有商标均为其各自所有者的财产。

12.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.4 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN6501QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBRQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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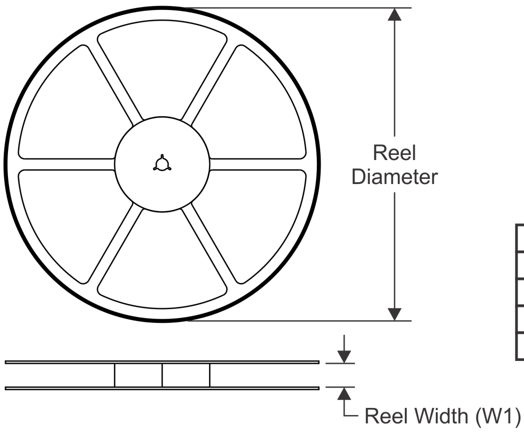
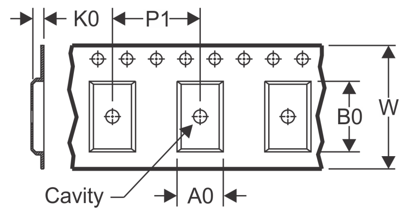
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

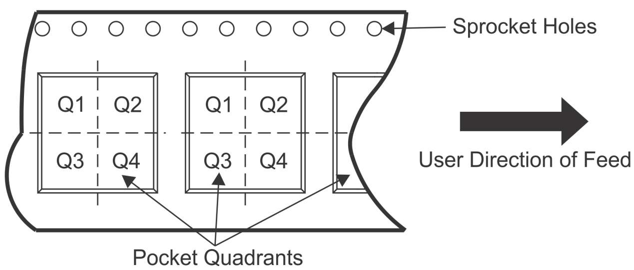


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

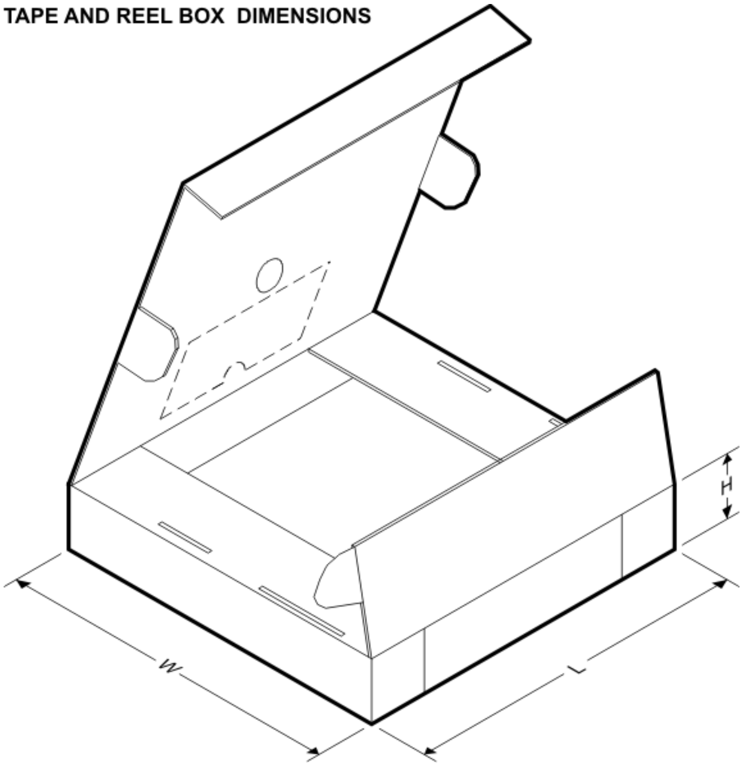
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

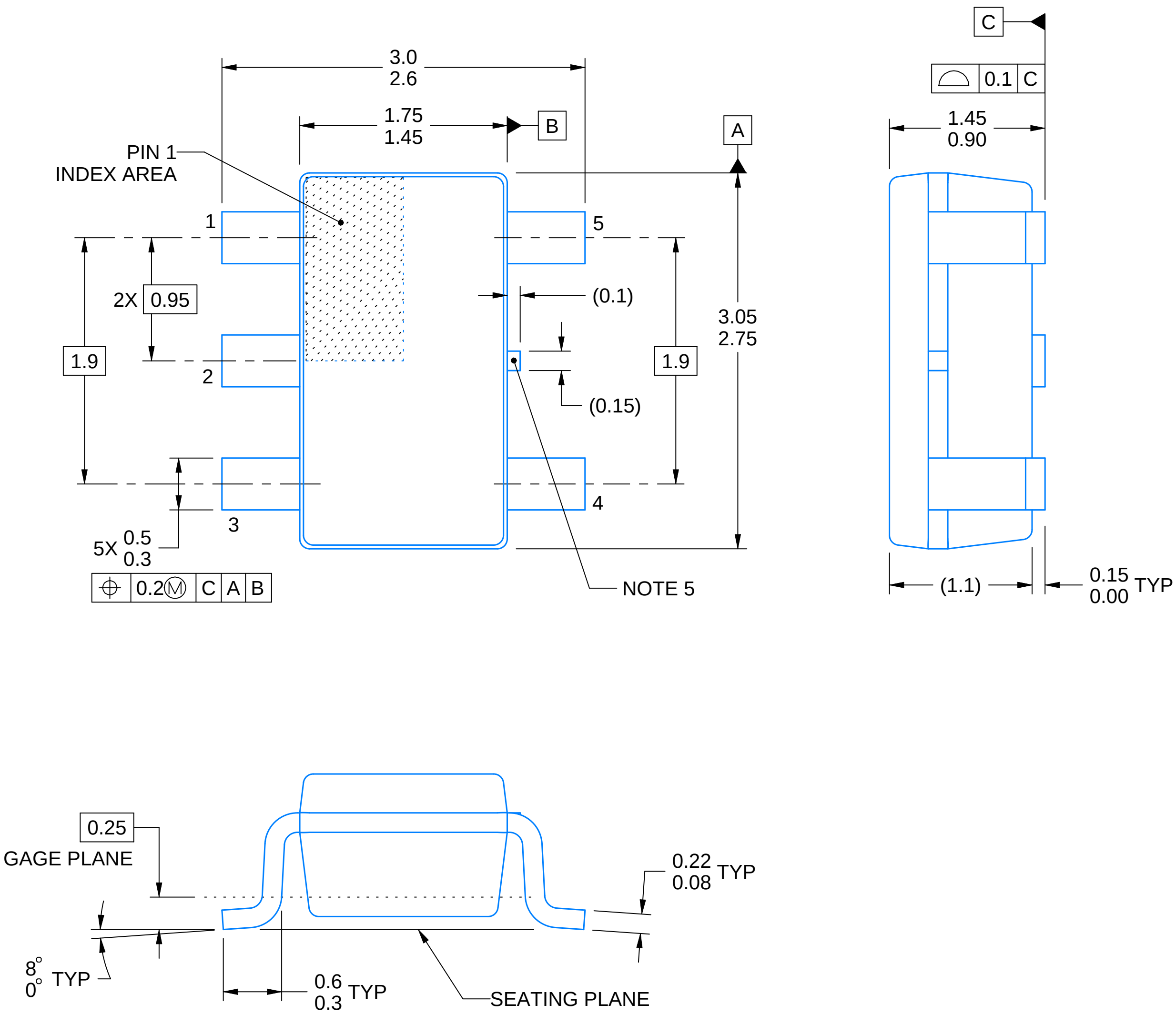
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN6501QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN6501QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0



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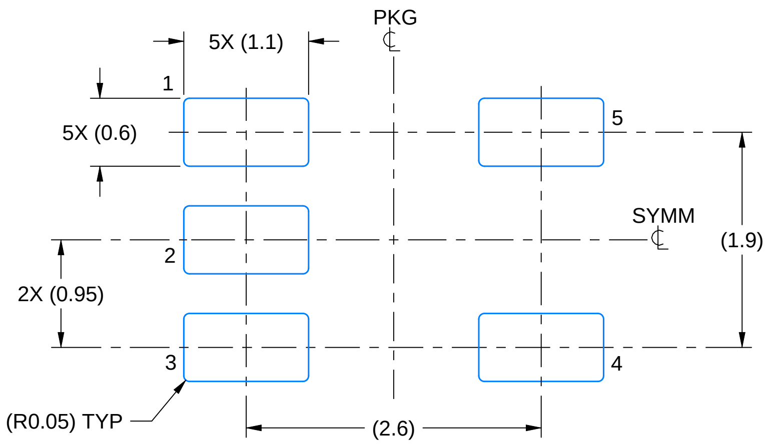
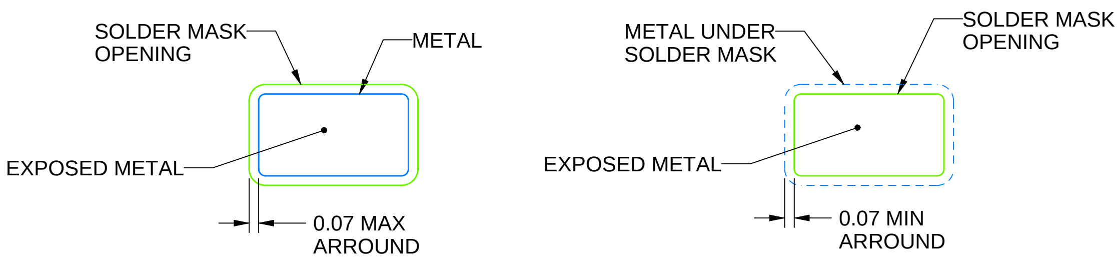
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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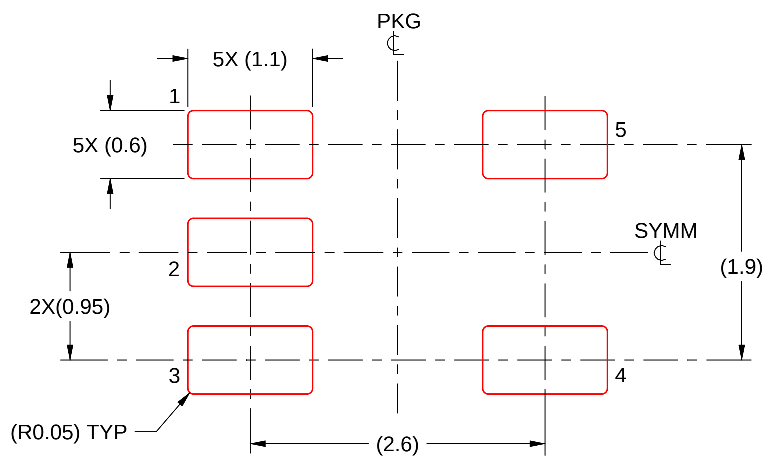
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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