

SN74LV11A-Q1 汽车类三路 3 输入正与非门

1 特性

- 符合汽车应用要求
- 工作范围为 2V 至 5.5V V_{CC}
- V_{OLP} (输出接地反弹) 典型值小于 0.8V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- V_{OHV} (输出 V_{OH} 下冲) 典型值大于 2.3V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时)
- 所有端口上均支持以混合模式电压运行
- I_{off} 支持局部关断模式运行

2 说明

这些三路 3 输入正与非门可在 2V 至 5.5V V_{CC} 电压下运行。

SN74LV11A-Q1 器件以正逻辑执行布尔函数 $Y = A \cdot B \cdot C$ or $Y = \overline{A + B + C}$ 。

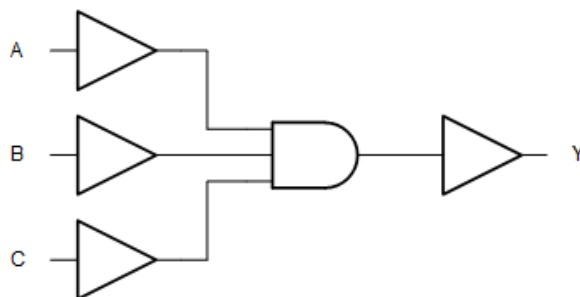
这些器件专用于使用 I_{off} 的局部断电应用。 I_{off} 电路禁用输出，从而可防止其断电时破坏性电流从该器件回流。

封装信息

器件型号	封装 ¹	封装尺寸 ²
SN74LV11A-Q1	PW (TSSOP , 14)	5.00 mm x 6.4 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 x 宽) 为标称值，并包括引脚 (如适用)。



简化原理图

Table of Contents

1 特性	1	5.10 Operating Characteristics.....	6
2 说明	1	6 Parameter Measurement Information	7
3 Revision History	2	7 Detailed Description	8
4 Pin Configuration and Functions	3	7.1 Overview.....	8
5 Specifications	4	7.2 Functional Block Diagram.....	8
5.1 Absolute Maximum Ratings.....	4	7.3 Device Functional Modes.....	8
5.2 ESD Ratings.....	4	8 Device and Documentation Support	9
5.3 Recommended Operating Conditions	4	8.1 Documentation Support (Analog).....	9
5.4 Thermal Information.....	5	8.2 接收文档更新通知.....	9
5.5 Electrical Characteristics.....	5	8.3 支持资源.....	9
5.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	5	8.4 Trademarks.....	9
5.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	5	8.5 静电放电警告.....	9
5.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	8.6 术语表.....	9
5.9 Noise Characteristics.....	6	9 Mechanical, Packaging, and Orderable Information	9

3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (May 2023) to Revision E (July 2023)

Page

- | | |
|--|----------|
| • 添加了封装信息表、引脚功能表、ESD 等级表、热信息表、器件功能模式、器件和文档支持部分以及机械、封装和可订购信息部分..... | 1 |
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4 Pin Configuration and Functions

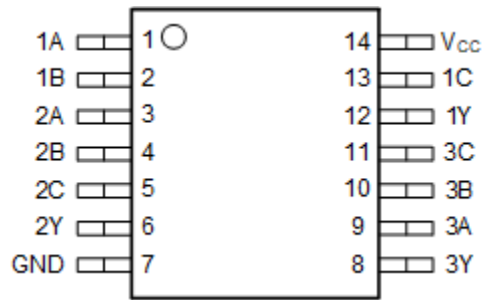


图 4-1. SN74LV11A-Q1 PW Package (Top View)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I	1A Input
1B	2	I	1B Input
2A	3	I	2A Input
2B	4	I	2B Input
2C	5	I	2C Input
2Y	6	O	2Y Output
3Y	8	O	3Y Output
3A	9	I	3A Input
3B	10	I	3B Input
3C	11	I	3C Input
1Y	12	O	1Y Output
1C	13	I	1C Input
GND	7	—	Ground Pin
V _{CC}	14	—	Power Pin

(1) Signal Types: I = Input, O = Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	- 0.5	7	V
V _I	Input voltage range ⁽²⁾	- 0.5	7	V
V _O	Output voltage range applied in high or low state ^{(2) (3)}	- 0.5	V _{CC} + 0.5	V
V _O	Output voltage range applied in power-off state ⁽²⁾	- 0.5	7	V
I _{IK}	Input clamp current (V _I < 0)		- 20	mA
I _{OK}	Output clamp current (V _O < 0)		- 50	mA
I _O	Continuous output current (V _O = 0 to V _{CC})		±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High level output current	V _{CC} = 2 V	- 50	mA
		V _{CC} = 2.3 V to 2.7 V	- 2	
		V _{CC} = 3 V to 3.6 V	- 6	
		V _{CC} = 4.5 V to 5.5 V	- 12	
I _{OL}	Low level output current	V _{CC} = 2 V	50	mA
		V _{CC} = 2.3 V to 2.7 V	2	
		V _{CC} = 3 V to 3.6 V	6	
		V _{CC} = 4.5 V to 5.5 V	12	

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
$\Delta t / \Delta v$	Input transition rise and fall rate	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	200	ns/V
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	100	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	20	
T_A	Operating free-air temperature	- 40	105	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#)

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV11A-Q1		UNIT
		PW		
		14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113		°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -50 \mu\text{A}$	2 V to 5.5 V		$V_{CC} - 0.1$	V
		$I_{OH} = -2 \text{ mA}$	2.3 V		2	
		$I_{OH} = -6 \text{ mA}$	3 V		2.48	
		$I_{OH} = -12 \text{ mA}$	4.5 V		3.8	
V_{OL}	Low-level output voltage	$I_{OL} = 50 \mu\text{A}$	2 V to 5.5 V		0.1	V
		$I_{OL} = 2 \text{ mA}$	2.3 V		0.4	
		$I_{OL} = 6 \text{ mA}$	3 V		0.44	
		$I_{OL} = 12 \text{ mA}$	4.5 V		0.55	
I_I	Input leakage current	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V		± 1	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		20	μA
I_{off}	Off-state leakage current	V_I or $V_O = 0$ to 5.5 V	0 V		5	μA
C_i	Input capacitance	$V_I = V_{CC}$ or GND	3.3 V		1.9	pF

5.6 Switching Characteristics, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV11A-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	$C_L = 50 \text{ pF}$		9.9	17.5	1	21	ns

5.7 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV11A-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	$C_L = 50 \text{ pF}$		7.2	12.3	1	14	ns

5.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV11A-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	$C_L = 50\text{ pF}$		5.4	7.9	1	9	ns

5.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		0	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

5.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$,	$f = 10\text{ MHz}$	3.3 V	13.9	pF
				5 V	15.4	

6 Parameter Measurement Information



图 6-1. Load Circuit and Voltage Waveforms

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

7 Detailed Description

7.1 Overview

This triple 3-input positive-AND gate is designed for 2-V to 5.5-V V_{CC} operation. The SN74LV11A-Q1 device performs the Boolean function $Y = \overline{A + B + C}$ in positive logic. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram

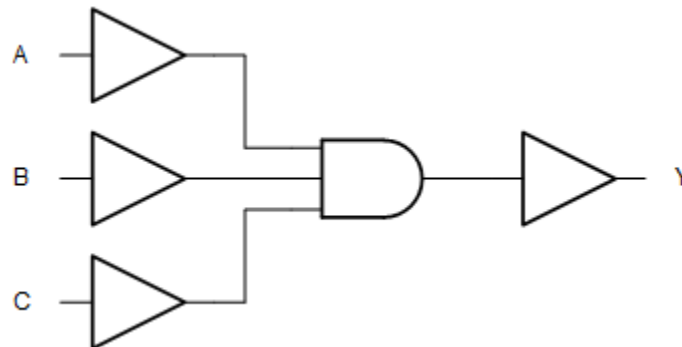


图 7-1. logic diagram, each gate (positive logic)

7.3 Device Functional Modes

表 7-1. FUNCTION TABLE
(each gate)

INPUT ⁽¹⁾			OUTPUT ⁽²⁾
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV11A-Q1	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

8.4 Trademarks

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8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV11ATPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LV11AT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LV11A-Q1 :

- Catalog : [SN74LV11A](#)
- Enhanced Product : [SN74LV11A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV11ATPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

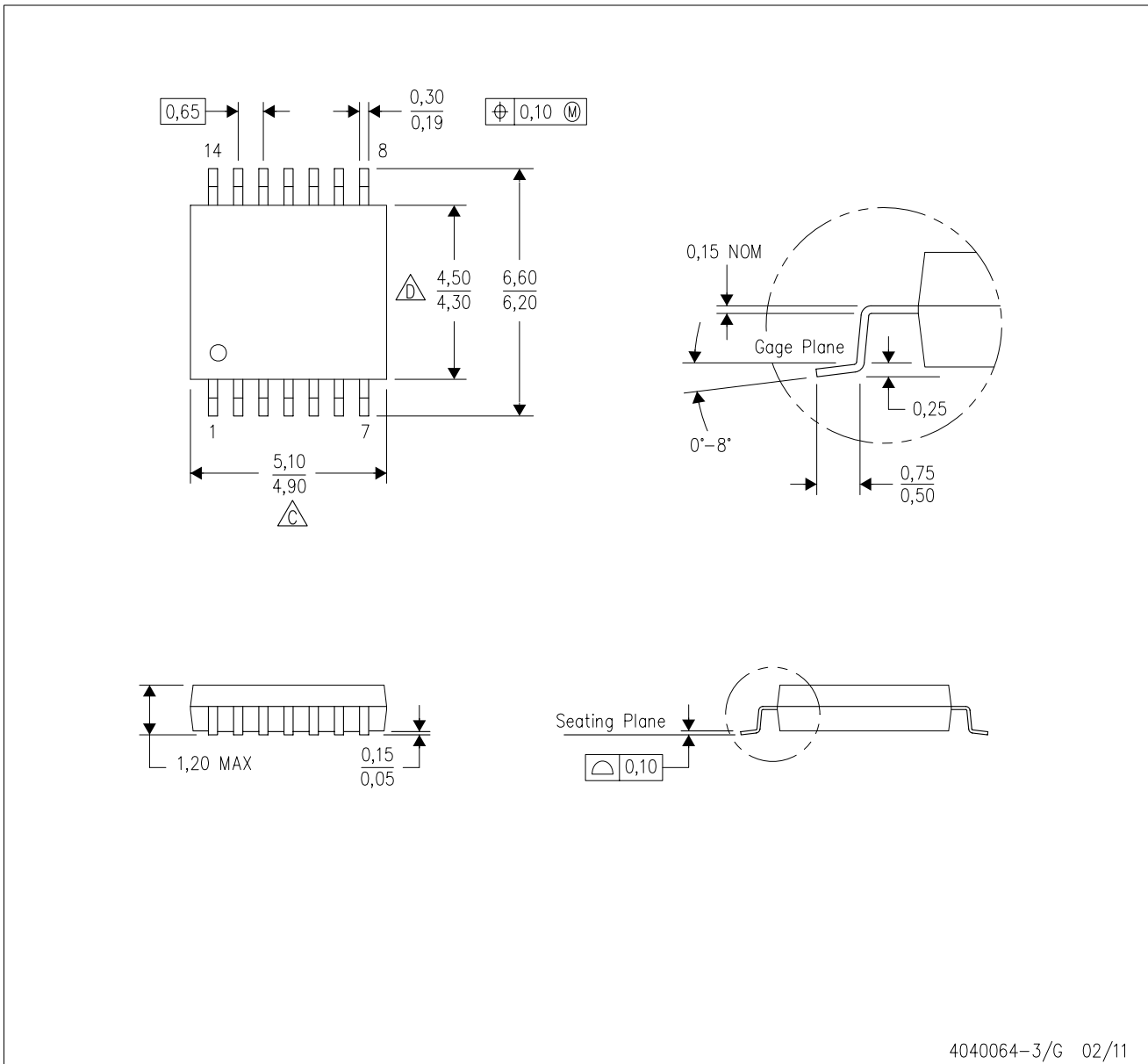

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV11ATPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0



MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

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