

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

- Choice of Open-Collector or Active Pullup (Totem-Pole) Outputs
- Single 5-V Supply
- Differential Line Operation
- Dual-Channel Operation
- TTL Compatible
- ± 15 -V Common-Mode Input Voltage Range
- Optional-Use Built-In 130- Ω Line-Terminating Resistor
- Individual Frequency-Response Controls
- Individual Channel Strobes
- Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers
- Designed to Be Interchangeable With National DS9615 Line Receivers

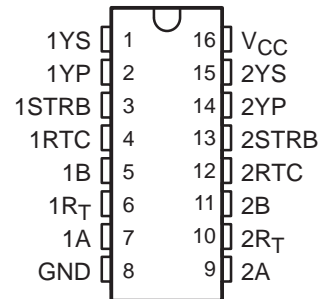
description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay.

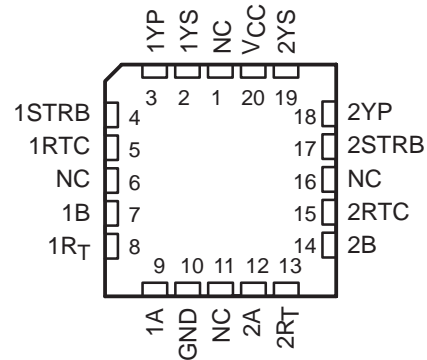
The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pullup terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

The SN55115 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75115 is characterized for operation from 0°C to 70°C .

SN55115 . . . J OR W PACKAGE
SN75115 . . . N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

STRB	DIFF INPUT (A AND B)	OUTPUT (YP AND YS TIED TOGETHER)
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH \text{ min}}$ or V_{ID} more positive than $V_{T+ \text{ max}}$
L = $V_I \leq V_{IL \text{ max}}$ or V_{ID} more negative than $V_{T- \text{ max}}$
X = irrelevant



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

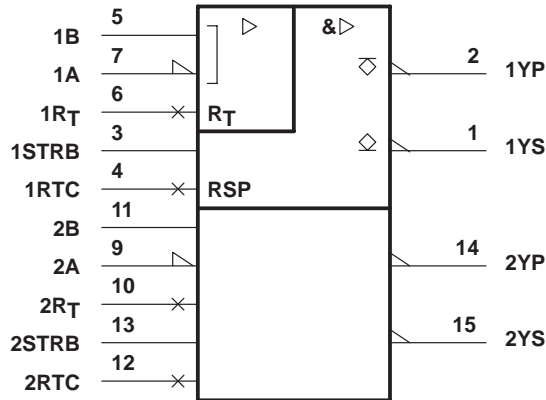
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

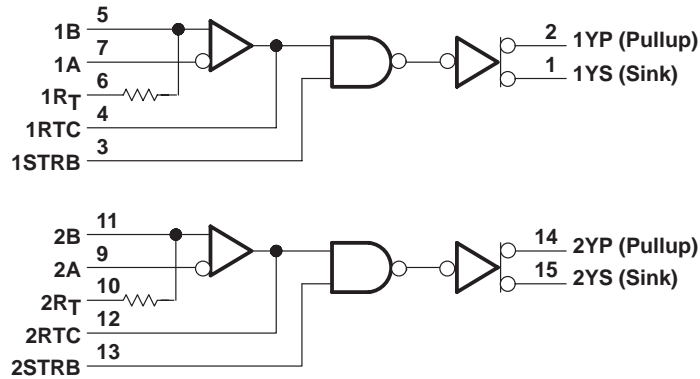
SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

logic symbol†

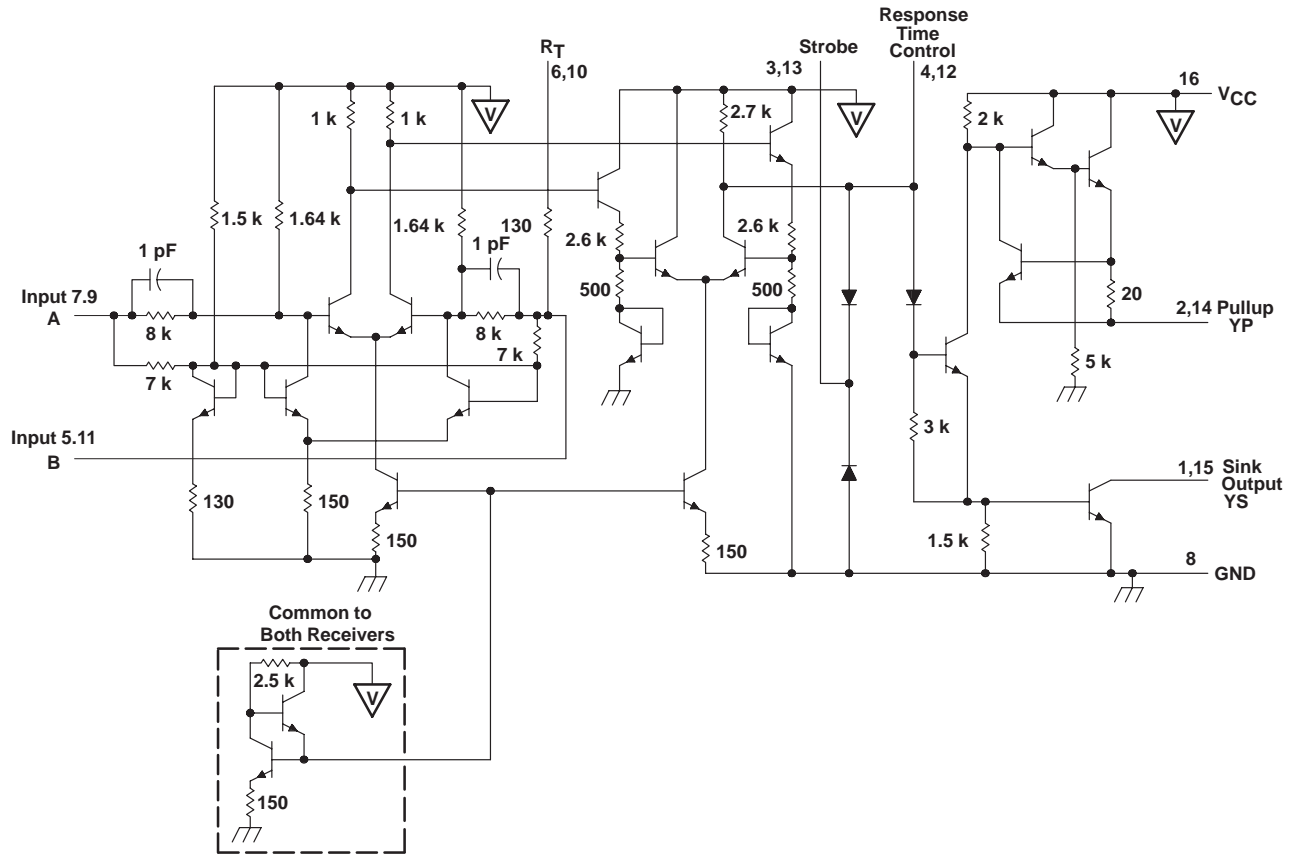


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values are nominal and in ohms.
Pin numbers shown are for the J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage V_I (A, B, and R_T)	± 25 V
Input voltage V_I (STRB)	5.5 V
Off-state voltage applied to open-collector outputs	14 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{Stg}	-65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input voltage, are with respect to network ground terminal.

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W†	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK, J, and W packages, SN55115 chips are either silver glass or alloy mounted. SN75115 chips are glass mounted.

recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage at STRB, V_{IH}	2.4			2.4			V
Low-level input voltage at STRB, V_{IL}	0.4			0.4			V
High-level output current, I_{OH}	-5			-5			mA
Low-level output current, I_{OL}	15			15			mA
Operating free-air temperature, T_A	-55			125			°C



SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55115			SN75115			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V_{IT+} §	Positive-going threshold voltage $V_O = 0.4\text{ V}$, $I_{OL} = 15\text{ mA}$, $V_{IC} = 0$	500			500			mV	
V_{IT-} §	Negative-going threshold voltage $V_O = 2.4\text{ V}$, $I_{OH} = -5\text{ mA}$, $V_{IC} = 0$	-500¶			-500¶			mV	
V_{ICR}	Common-mode input voltage range $V_{ID} = \pm 1\text{ V}$	+15 to -15	+24 to -19		+15 to -15	+24 to -19		V	
V_{OH}	High-level output voltage $V_{CC} = \text{MIN}$, $I_{OH} = -5\text{ mA}$, $V_{ID} = -0.5\text{ V}$	$T_A = \text{MIN}$	2.2		2.4		V		
		$T_A = 25^\circ\text{C}$	2.4	3.4	2.4	3.4			
		$T_A = \text{MAX}$	2.4		2.4				
V_{OL}	Low-level output voltage $V_{CC} = \text{MIN}$, $I_{OL} = 15\text{ mA}$, $V_{ID} = -0.5\text{ V}$	0.22		0.4	0.22 0.45		V		
I_{IL}	Low-level input current $V_{CC} = \text{MAX}$, $V_I = 0.4\text{ V}$, Other input at 5.5 V	$T_A = \text{MIN}$	-0.9		-0.9		mA		
		$T_A = 25^\circ\text{C}$	-0.5	-0.7	-0.5	-0.7			
		$T_A = \text{MAX}$	-0.7		-0.7				
I_{SH}	High-level strobe current $V_{CC} = \text{MIN}$, $V_{ID} = -0.5\text{ V}$, $V_{\text{strobe}} = 4.5\text{ V}$	$T_A = 25^\circ\text{C}$	2		5		μA		
		$T_A = \text{MAX}$	5		10				
I_{SL}	Low-level strobe current $V_{CC} = \text{MAX}$, $V_{ID} = 0.5\text{ V}$, $V_{\text{strobe}} = 0.4\text{ V}$	$T_A = 25^\circ\text{C}$	-1.15	-2.4	-1.15	-2.4	mA		
$I_{(RTC)}$	Response-time-control current $V_{CC} = \text{MAX}$, $V_{ID} = 0.5\text{ V}$, $V_{RC} = 0$	$T_A = 25^\circ\text{C}$	-1.2	-3.4	-1.2	-3.4	mA		
$I_{O(\text{off})}$	Off-state open-collector output current $V_{CC} = \text{MIN}$, $V_{ID} = -4.5\text{ V}$, $V_{OH} = 12\text{ V}$	$T_A = 25^\circ\text{C}$	100				μA		
		$T_A = \text{MAX}$	200						
	$V_{CC} = \text{MIN}$, $V_{ID} = -4.75\text{ V}$, $V_{OH} = 5.25\text{ V}$	$T_A = 25^\circ\text{C}$			100				
		$T_A = \text{MAX}$			200				
R_T	Line-terminating resistance $V_{CC} = 5\text{ V}$	$T_A = 25^\circ\text{C}$	77	130	167	74	130	179	Ω
I_{OS}	Supply-circuit output current# $V_{CC} = \text{MAX}$, $V_{ID} = -0.5\text{ V}$, $V_O = 0$	$T_A = 25^\circ\text{C}$	-15	-40	-80	-14	-40	-100	mA
I_{CC}	Supply current (both receivers) $V_{CC} = \text{MAX}$, $V_{ID} = 0.5\text{ V}$, $V_{IC} = 0$	$T_A = 25^\circ\text{C}$	32		50	32		50	mA

† Unless otherwise noted, $V_{\text{strobe}} = 2.4\text{ V}$. All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, and $V_{IC} = 0$.

§ Differential voltages are at the B input terminal with respect to the A input terminal.

¶ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.



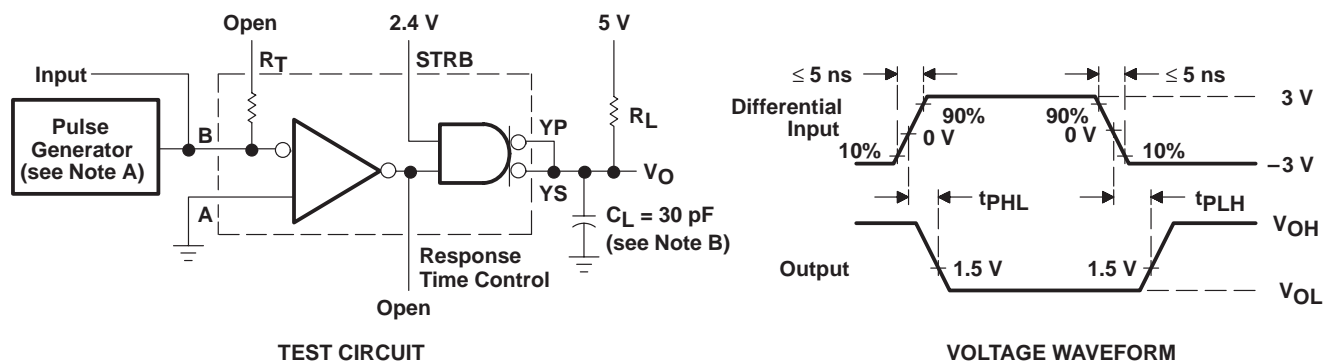
SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 30\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	SN55115			SN75115			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high level output	$R_L = 3.9\text{ k}\Omega$, See Figure 1		18	50		18	75	ns
t_{PHL} Propagation delay time, high-to-low level output	$R_L = 390\ \Omega$, See Figure 1		20	50		20	75	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, $PRR \leq 500\text{ kHz}$, $t_w \leq 100\text{ ns}$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

INPUT CURRENT
vs
INPUT VOLTAGE

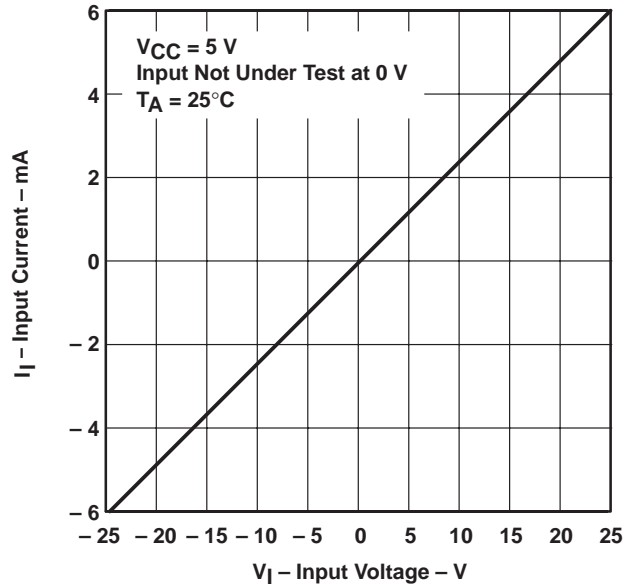


Figure 2

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

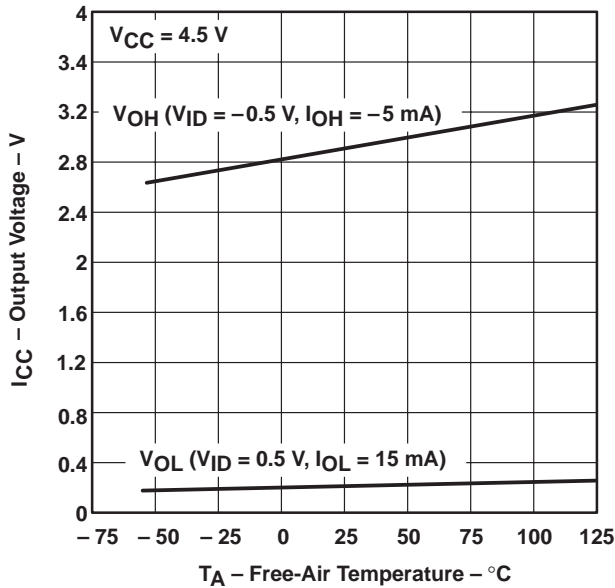


Figure 3

OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

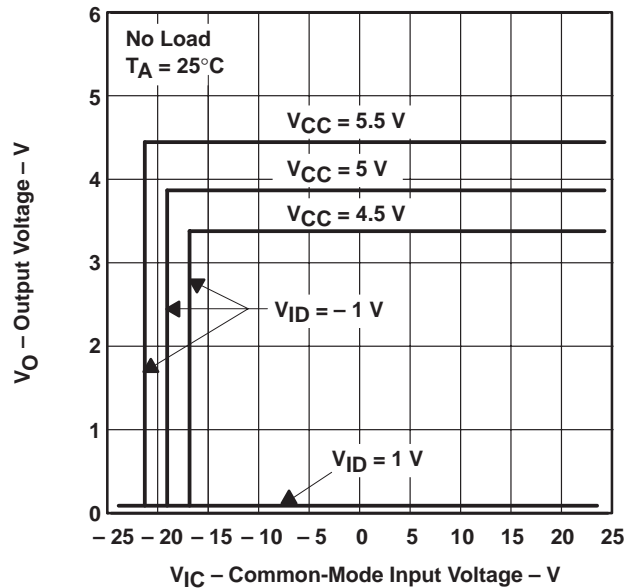


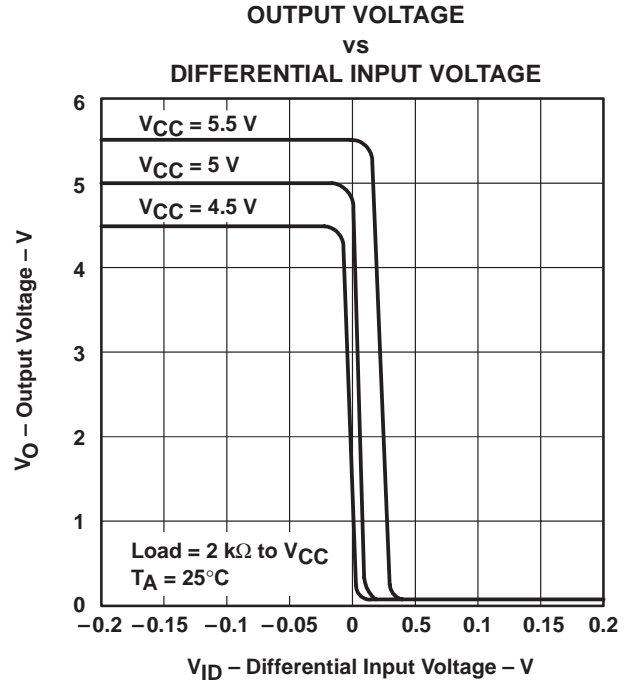
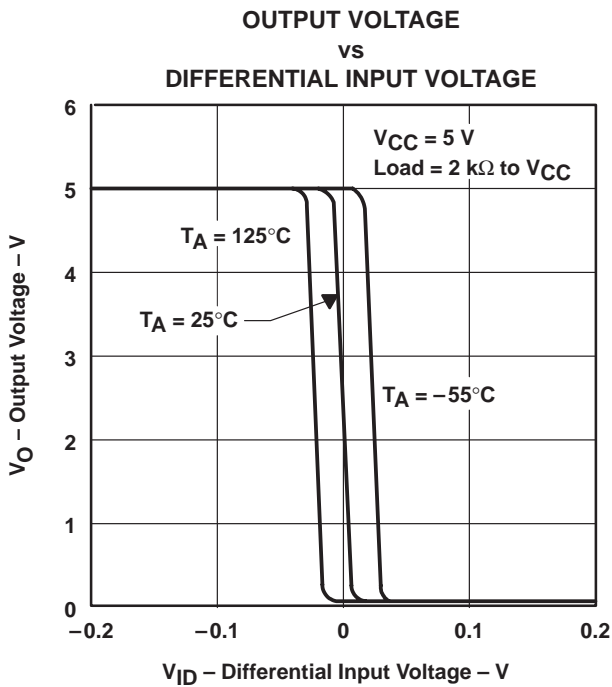
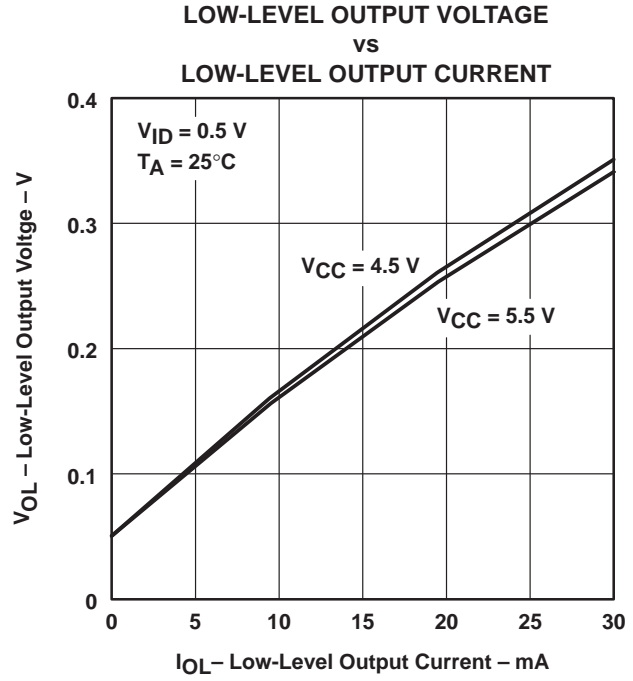
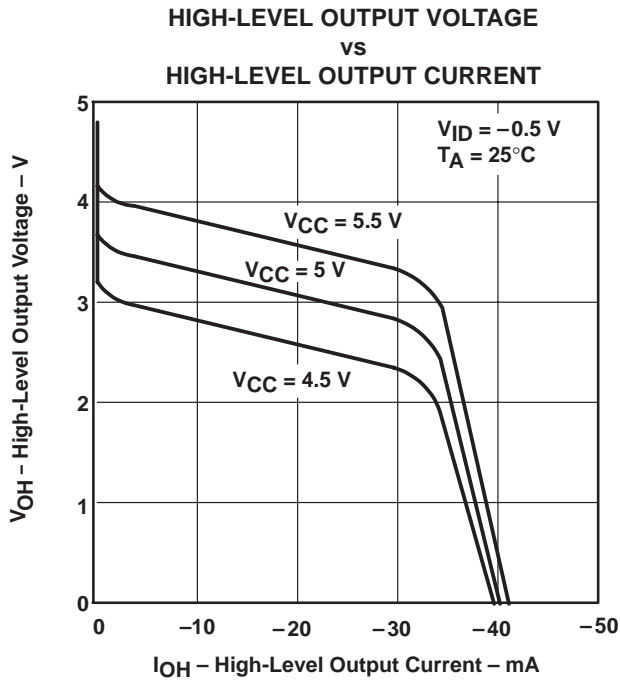
Figure 4

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS†

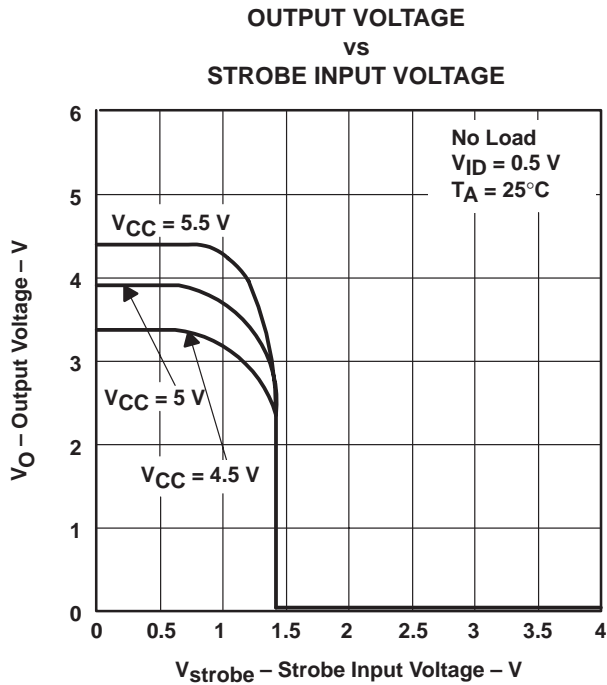


Figure 9

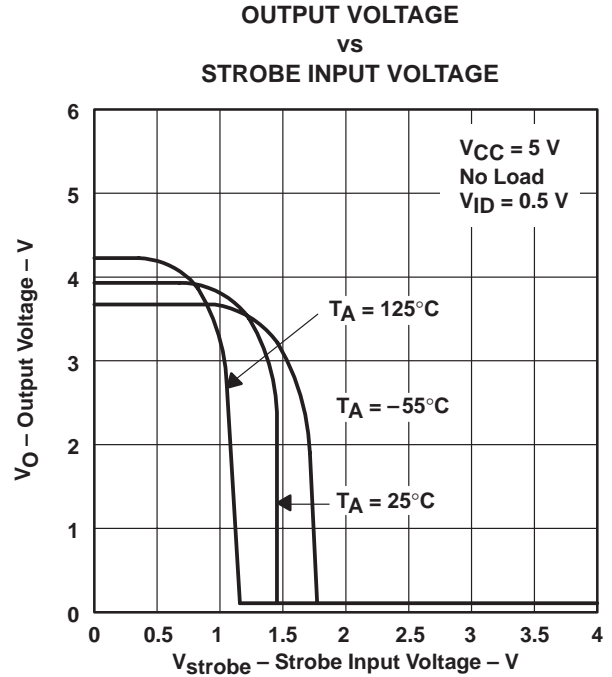


Figure 10

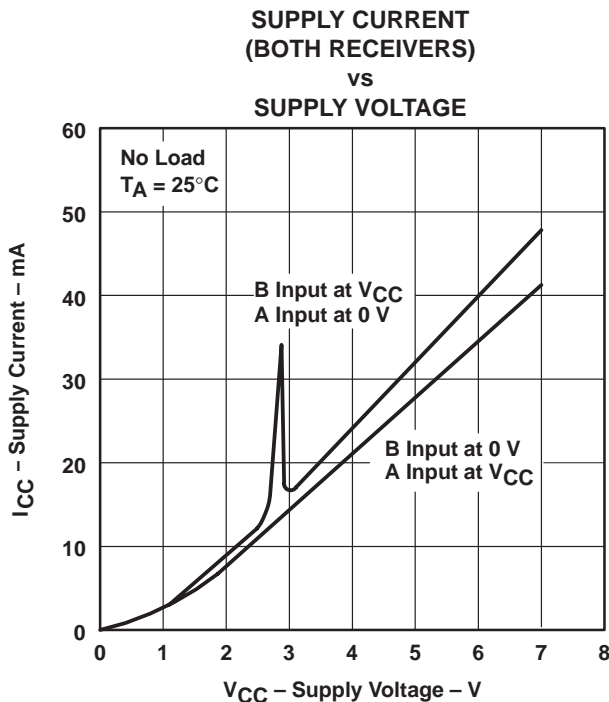


Figure 11

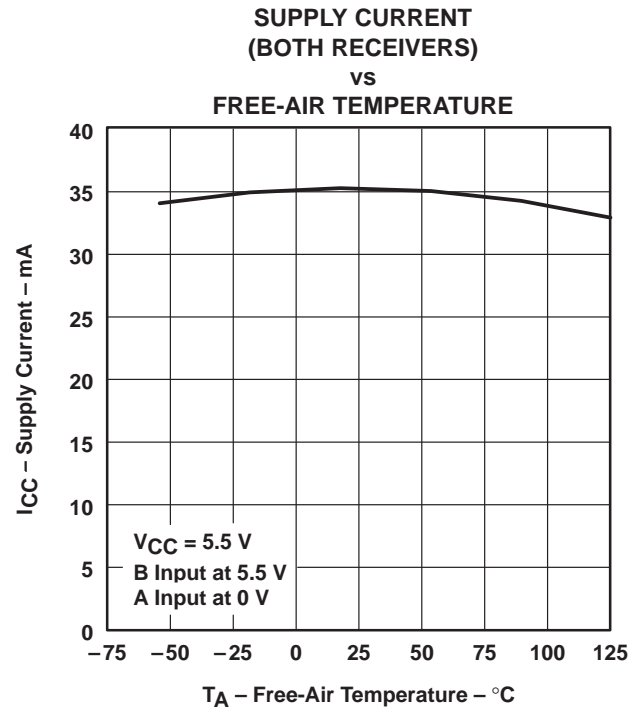


Figure 12

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

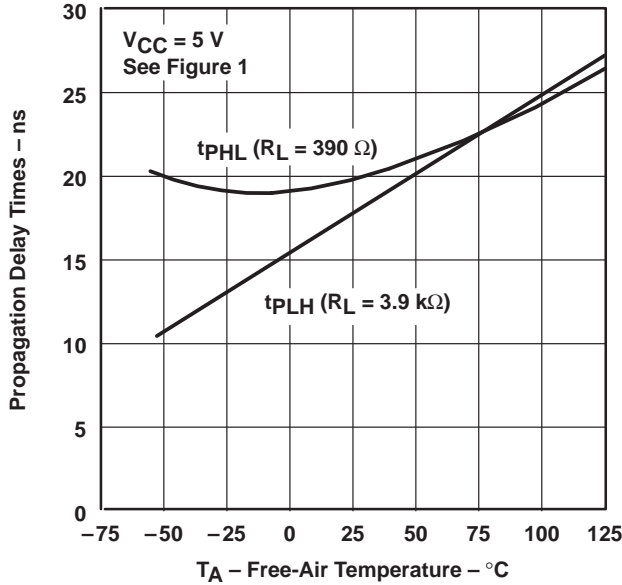


Figure 13

MAXIMUM OPERATING FREQUENCY
vs
RESPONSE-TIME-CONTROL CAPACITANCE

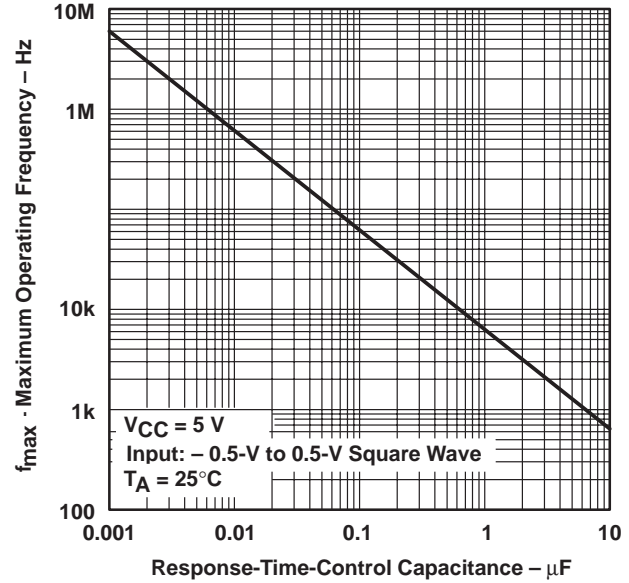
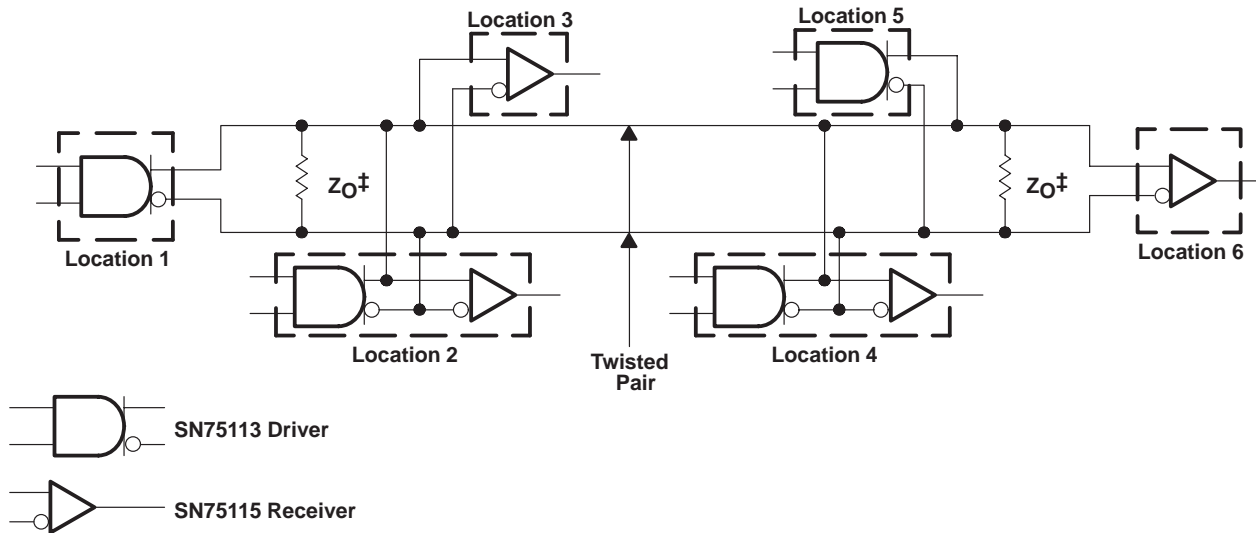


Figure 14

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



‡ $Z_O = R_T$. A capacitor may be connected in series with Z_O to reduce power dissipation.

Figure 15. Basic Party-Line or Data-Bus Differential Data Transmission

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88745012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 88745012A SNJ55 115FK	Samples
5962-8874501FA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8874501FA SNJ55115W	Samples
JM38510/10404BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10404BEA	Samples
M38510/10404BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10404BEA	Samples
SN55115J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN55115J	Samples
SN75115D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	
SN75115DR	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	
SN75115N	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75115N	
SN75115N-A	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type		SN75115N-A	
SN75115NE4	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75115N	
SN75115NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75115	Samples
SNJ55115FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 88745012A SNJ55 115FK	Samples
SNJ55115J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ55115J	Samples
SNJ55115W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8874501FA SNJ55115W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55115, SN75115 :

● Catalog : [SN75115](#)

● Military : [SN55115](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75115DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75115NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75115DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75115NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-88745012A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-8874501FA	W	CFP	16	1	506.98	26.16	6220	NA
SN75115D	D	SOIC	16	40	507	8	3940	4.32
SN75115N	N	PDIP	16	25	506	13.97	11230	4.32
SN75115N-A	N	PDIP	16	25	506	13.97	11230	4.32
SN75115NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ55115FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ55115W	W	CFP	16	1	506.98	26.16	6220	NA



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated