

SNx5C3243 符合 RS-232 的 3V 至 5.5V 多通道线路驱动器和接收器

1 特性

- 由 3V 至 5.5V V_{CC} 电源供电
- 始终有效同相接收器输出 (ROUT2B)
- 低待机电流: $1 \mu A$ (典型值)
- 外部电容器: $4 \times 0.1 \mu F$
- 接受 5V 逻辑输入及 3.3V 电源
- 可与 SN65C3238、SN75C3238 互操作
- 支持 250kbit/s 至 1Mbit/s 的运行速度
- 使用人体放电模型 (HBM) 时, RS-232 总线引脚 ESD 保护大于 $\pm 15kV$

2 应用

- 电池供电型系统
- 个人电子产品
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

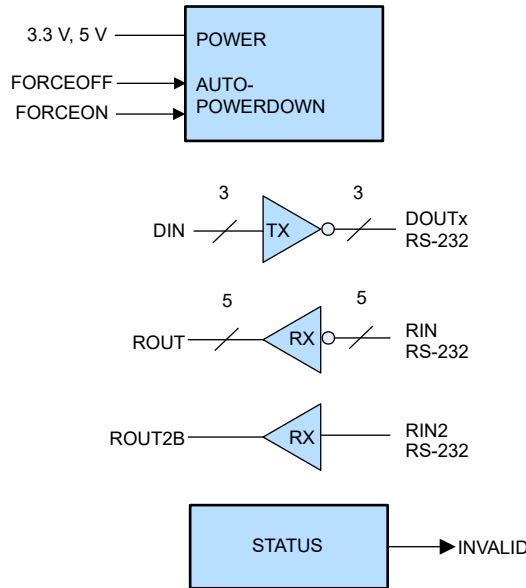
3 说明

SN65C3243 和 SN75C3243 包含三个线路驱动器、五个线路接收器和一个具有引脚对引脚 (串行端口连接引脚, 包括 GND) $\pm 15kV$ ESD 保护功能的双电荷泵电路。该器件可在异步通信控制器和串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。另外, 该器件包括一个始终有效同相输出 (ROUT2B), 这使得使用振铃指示的应用能够在器件断电的情况下发送数据。该器件以高达 1Mbit/s 的数据信号传输速率运行, 具有从 $24 V/\mu s$ 至 $150V/\mu s$ 的更高压摆率范围。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
SN65C3243 SN75C3243	SSOP (DB)	10.2 mm x 5.30 mm
	SOIC (DW)	17.9 mm x 7.50 mm
	TSSOP (PW)	9.70 mm x 4.40 mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



简化版电路



Table of Contents

1 特性	1	6.10 Switching Characteristics: Receiver.....	7
2 应用	1	6.11 Switching Characteristics: Auto-Powerdown.....	7
3 说明	1	7 Parameter Measurement Information	8
4 Revision History	2	8 Detailed Description	11
5 Pin Configuration and Functions	3	8.1 Overview.....	11
6 Specifications	4	8.2 Device Functional Modes.....	11
6.1 Absolute Maximum Ratings.....	4	9 Device and Documentation Support	13
6.2 ESD Ratings.....	4	9.1 Device Support.....	13
6.3 Recommended Operating Conditions.....	4	9.2 接收文档更新通知.....	13
6.4 Thermal Information.....	5	9.3 支持资源.....	13
6.5 Electrical Characteristics.....	5	9.4 Trademarks.....	13
6.6 Electrical Characteristics, Driver Section.....	5	9.5 静电放电警告.....	13
6.7 Electrical Characteristics, Receiver Section.....	6	9.6 术语表.....	13
6.8 Electrical Characteristics, Auto-Powerdown Section.....	6	10 Mechanical, Packaging, and Orderable Information	13
6.9 Switching Characteristics: Driver.....	7		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (September 2008) to Revision I (October 2022)	Page
• 添加了器件信息表、引脚配置和功能部分、ESD 等级表、热性能信息表、详细说明部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Changed the I _{CC} Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the <i>Electrical Characteristics</i>	5

5 Pin Configuration and Functions

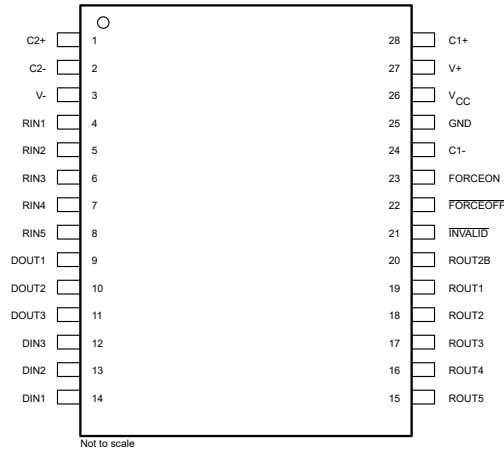


图 5-1. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP)
(Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-	—	Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	INVALID	O	Invalid Output Pin
22	FORCEOFF	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V _{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	- 0.3	6	V
V+	Positive-output supply voltage range ⁽²⁾	- 0.3	7	V
V-	Negative-output supply voltage range ⁽²⁾	0.3	- 7	V
V+ - V-	Supply voltage difference ⁽²⁾		13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON)		V
		Receiver		
V _O	Output voltage range	- 13.2	13.2	V
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 on RS-232 bus pins DOUT1/2/3, RIN1/2/3/4/5 ⁽¹⁾	±15 kV

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

see 图 7-6 ⁽¹⁾

		MIN	NOM	MAX	UNIT	
Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V	
	V _{CC} = 5 V	4.5	5	5.5		
V _{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON		V		
		V _{CC} = 3.3 V	2			
		V _{CC} = 5 V	2.4			
V _{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON		0.8	V	
V _I	Driver and control input voltage	DIN, FORCEOFF, FORCEON		0	5.5	V
V _I	Receiver input voltage	- 25		25	V	
T _A	Operating free-air temperature	SN65C3243	- 40	85	°C	
		SN75C3243	0	70		

- (1) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DB (SSOP)	DW (SOIC)	PW (TSSOP)	UNIT
		28 PINS	28 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.1	59.0	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	28.8	21.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	30.3	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	7.8	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.0	30.0	28.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I_I	Input leakage current	FORCEOFF, FORCEON		±0.01	±1	μA
I_{CC}	Supply current	Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V_{CC} For DB and PW package	0.3	1.2	mA
		Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V_{CC} For DW package	0.3	1	mA
		Powered off	No load, FORCEOFF = GND	1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF = V_{CC} , FORCEON = GND, All RIN are open or grounded, All DIN are grounded	1	10	

- (1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

- (2) Test conditions are C1 - C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF, C2 - C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.6 Electrical Characteristics, Driver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))

PARAMETER	TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at $R_L = 3\text{ k}\Omega$ to GND	5	5.4	V
V_{OL}	Low-level output voltage	All DOUT at $R_L = 3\text{ k}\Omega$ to GND	-5	-5.4	V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC} , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5		V
I_{IH}	High-level input current	$V_I = V_{CC}$	±0.01	±1	μA
I_{IL}	Low-level input current	$V_I = \text{GND}$	±0.01	±1	μA
I_{OS}	Short-circuit output current ⁽²⁾	$V_{CC} = 3.6\text{ V}$, $V_O = 0\text{ V}$	±35	±60	mA
		$V_{CC} = 5.5\text{ V}$, $V_O = 0\text{ V}$	±35	±90	
r_o	Output resistance	V_{CC} , V+, and V- = 0 V, $V_O = \pm 2\text{ V}$	300	10M	Ω
I_{off}	Output leakage current	FORCEOFF = GND	$V_O = \pm 12\text{ V}$, $V_{CC} = 3\text{ V to } 3.6\text{ V}$	±25	μA
			$V_O = \pm 10\text{ V}$, $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	±25	

- (1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

- (2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

- (3) Test conditions are C1 - C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF, C2 - C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.7 Electrical Characteristics, Receiver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.8 Electrical Characteristics, Auto-Powerdown Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{T+(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}		2.7	V
V _{T-(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-2.7		V
V _{T(invalid)}	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-0.3	0.3	V
V _{OH}	INVALID high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} - 0.6		V
V _{OL}	INVALID low-level output voltage	I _{OL} = 1.6 mA, FORCEON = GND, FORCEOFF = V _{CC}		0.4	V

6.9 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 7-6](#))

PARAMETER	TEST CONDITIONS ⁽³⁾		MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate (see 图 7-1)	R _L = 3 kΩ, One DOUT switching	C _L = 1000 pF		250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V		1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V		1000		
t _{sk(p)} Pulse skew ⁽²⁾	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See 图 7-2			25		ns
SR(tr) Slew rate, transition region (see 图 7-1)	C _L = 150 pF to 1000 pF, R _L = 3 kΩ to 7 kΩ, V _{CC} = 3.3 V			18	150	V/μs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

(3) Test conditions are C₁ - C₄ = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C₁ = 0.047 μF, C₂ - C₄ = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽³⁾	TYP ⁽¹⁾	UNIT
t _{PLH} Propagation delay time, low- to high-level output	C _L = 150 pF, See 图 7-3	150	ns
t _{PHL} Propagation delay time, high- to low-level output	C _L = 150 pF, See 图 7-3	150	ns
t _{en} Output enable time	C _L = 150 pF, R _L = 3 kΩ, See 图 7-4	200	ns
t _{dis} Output disable time	C _L = 150 pF, R _L = 3 kΩ, See 图 7-4	200	ns
t _{sk(p)} Pulse skew ⁽²⁾	See 图 7-3	50	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

(3) Test conditions are C₁ - C₄ = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C₁ = 0.047 μF, C₂ - C₄ = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

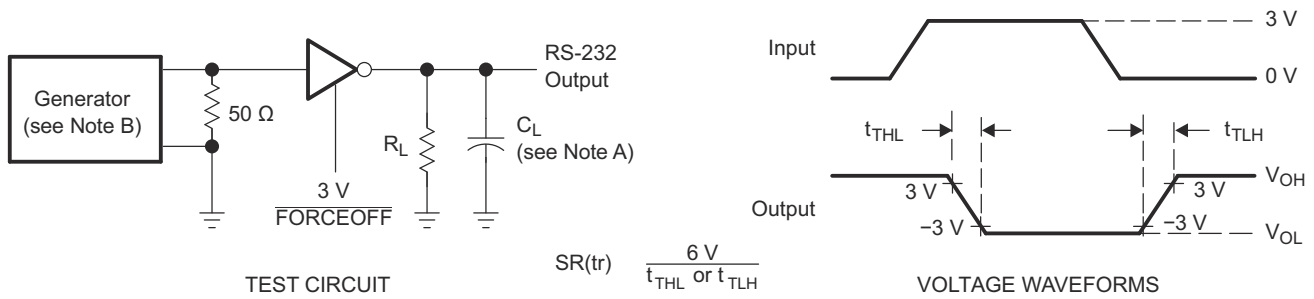
6.11 Switching Characteristics: Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 7-5](#))

PARAMETER	TYP ⁽¹⁾	UNIT
t _{valid} Propagation delay time, low- to high-level output	1	μs
t _{invalid} Propagation delay time, high- to low-level output	30	μs
t _{en} Supply enable time	100	μs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

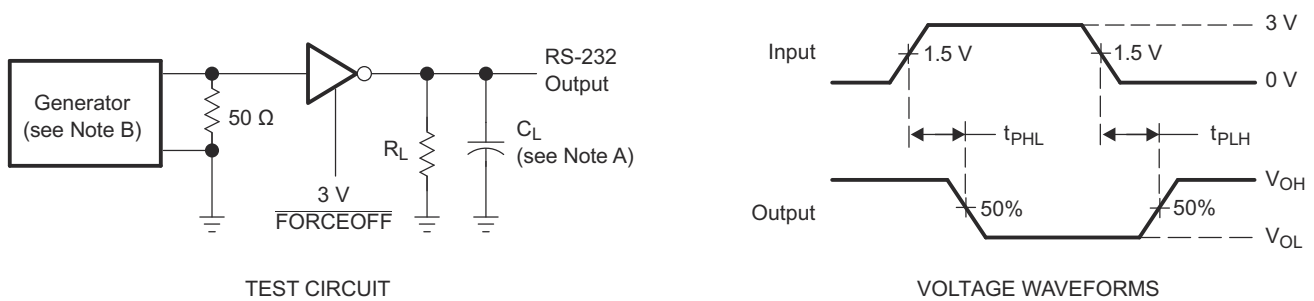
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 1 Mbps, $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

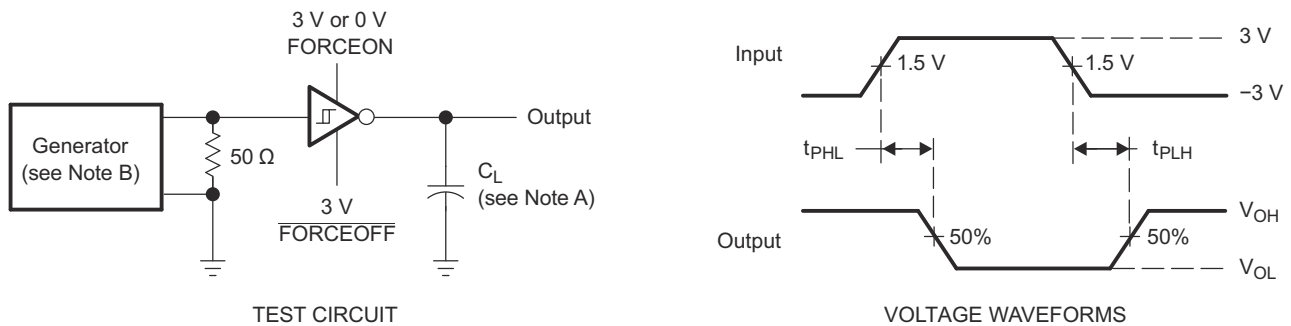
图 7-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 1 Mbps, $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

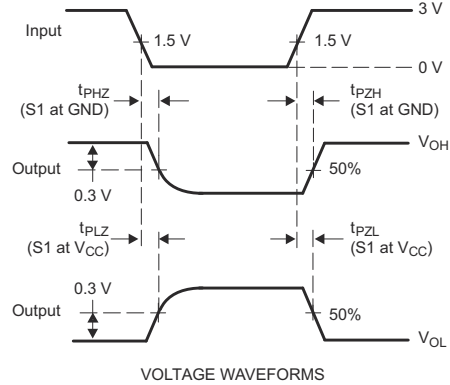
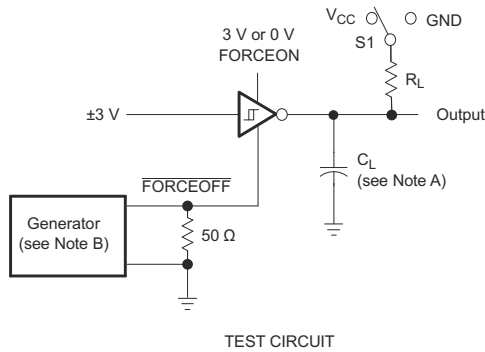
图 7-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance.

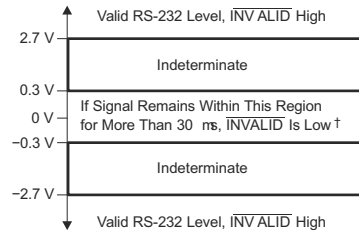
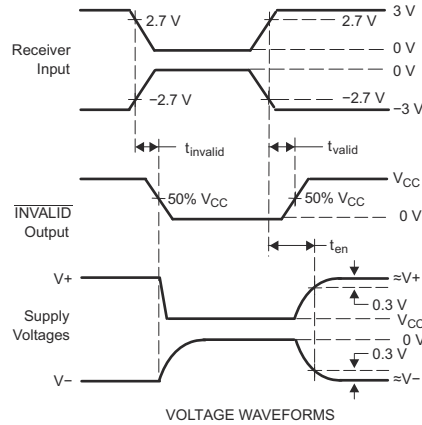
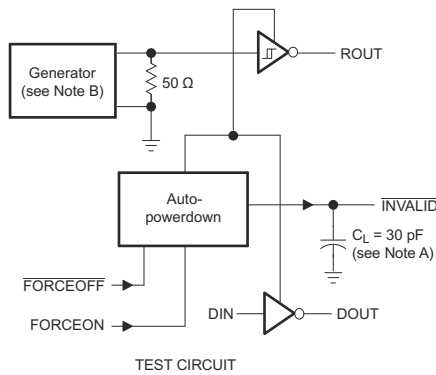
B. The pulse generator has the following characteristics: $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-3. Receiver Propagation Delay Times



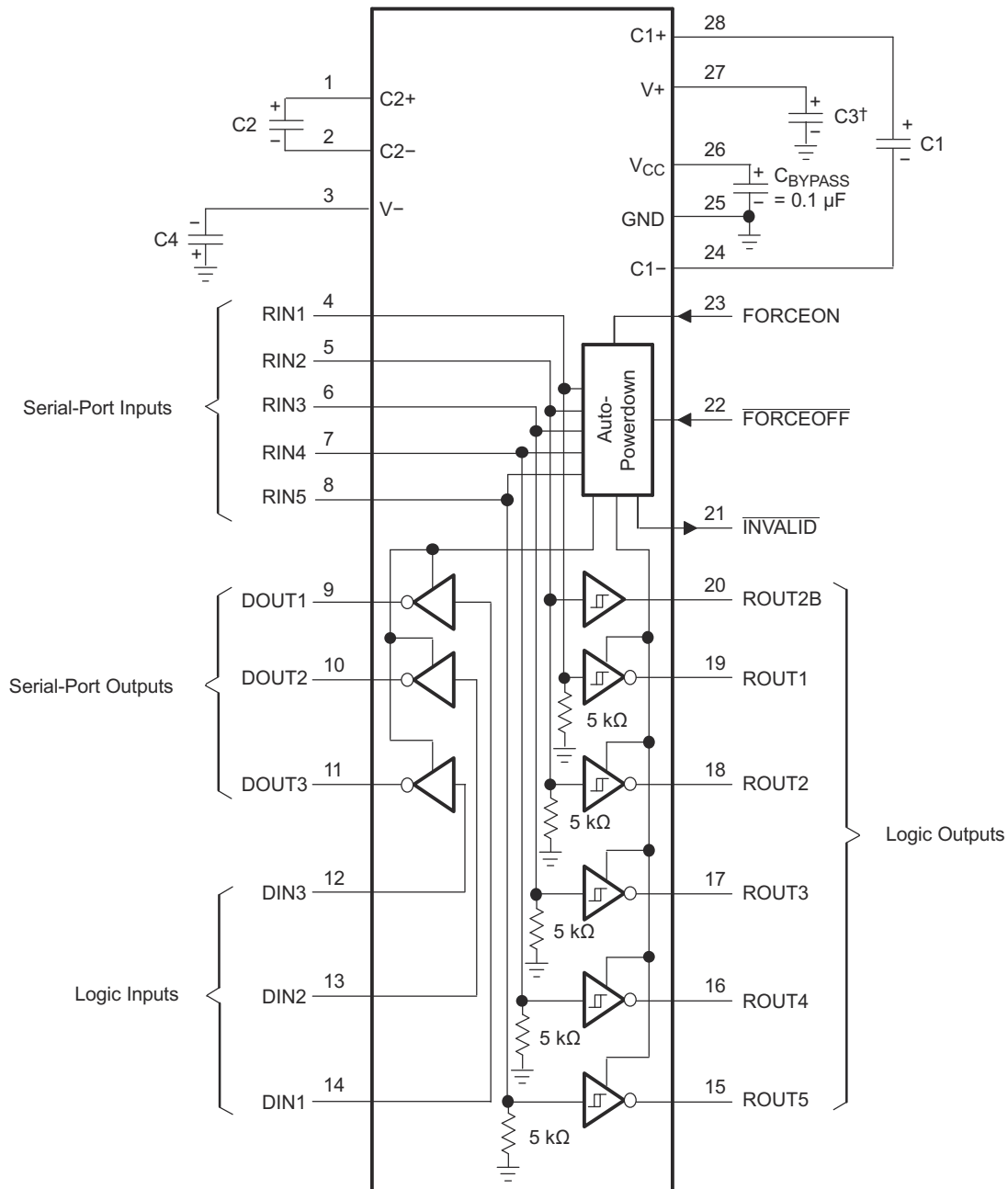
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

图 7-4. Receiver Enable and Disable Times



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 5 Mbits, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 7-5. INVALID Propagation Delay Times and Supply Enabling Time



† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

图 7-6. Typical Operating Circuit and Capacitor Values

表 7-1. V_{CC} vs Capacitor Values

V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

8 Detailed Description

8.1 Overview

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and FORCEOFF are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to [Figure 7-5](#) for receiver input levels.

8.2 Device Functional Modes

8.2.1 Function Tables

Each Driver, DIN⁽¹⁾

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver, RIN⁽¹⁾

INPUTS				OUTPUTS			RECEIVER STATUS
RIN2	RIN1, RIN3 - RIN5	FORCEOFF	VALID RIN RS-232 LEVEL	ROUT2B	ROUT2	ROUT1, ROUT3 - 5	
L	X	L	X	L	Z	Z	Powered off while ROUT2B is active
H	X	L	X	H	Z	Z	
L	L	H	YES	L	H	H	Normal operation with auto-powerdown disabled/enabled
L	H	H	YES	L	L	L	
H	L	H	YES	H	H	H	
H	H	H	YES	H	L	L	
Open	Open	H	YES	L	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

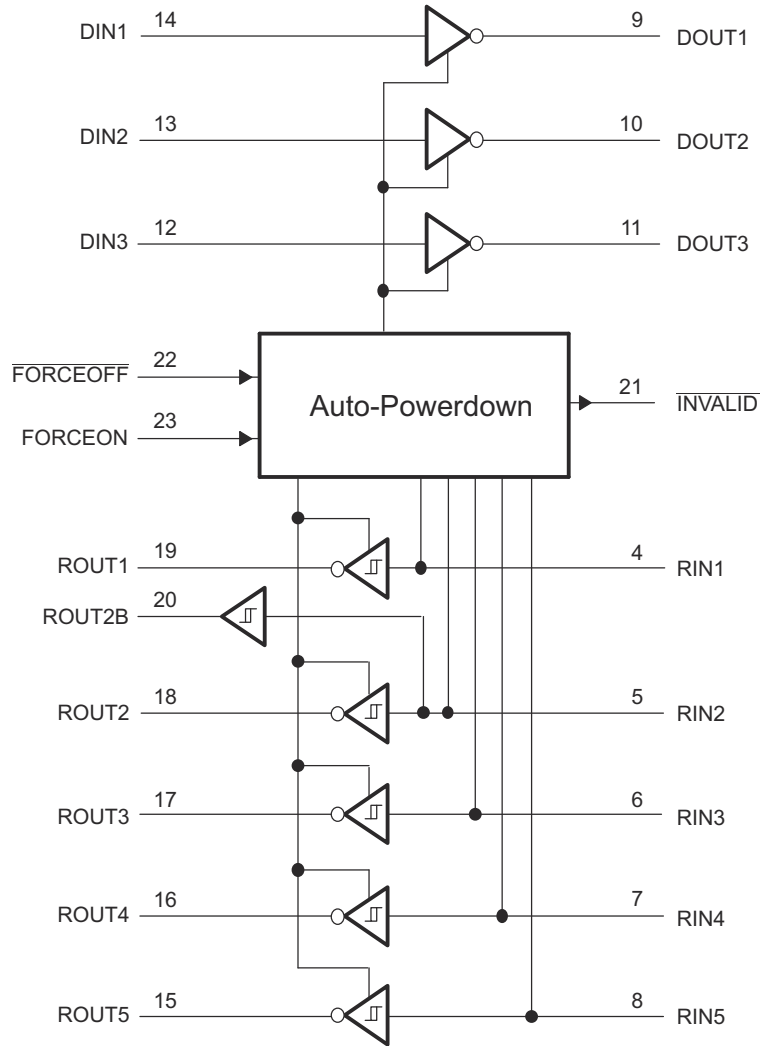


图 8-1. Logic Diagram (Positive Logic)

9 Device and Documentation Support

9.1 Device Support

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C3243DBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DW	NRND	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	
SN65C3243DWR	NRND	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	
SN65C3243PW	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	
SN65C3243PWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	Samples
SN75C3243DBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243DW	NRND	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	
SN75C3243DWR	NRND	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	
SN75C3243PW	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	
SN75C3243PWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN65C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN75C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN75C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3243DBR	SSOP	DB	28	2000	356.0	356.0	35.0
SN65C3243DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN65C3243PWR	TSSOP	PW	28	2000	356.0	356.0	35.0
SN75C3243DBR	SSOP	DB	28	2000	356.0	356.0	35.0
SN75C3243DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN75C3243PWR	TSSOP	PW	28	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C3243DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN65C3243PW	PW	TSSOP	28	50	530	10.2	3600	3.5
SN65C3243PW	PW	TSSOP	28	50	530	10.2	3600	3.5
SN75C3243DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN75C3243PW	PW	TSSOP	28	50	530	10.2	3600	3.5
SN75C3243PW	PW	TSSOP	28	50	530	10.2	3600	3.5

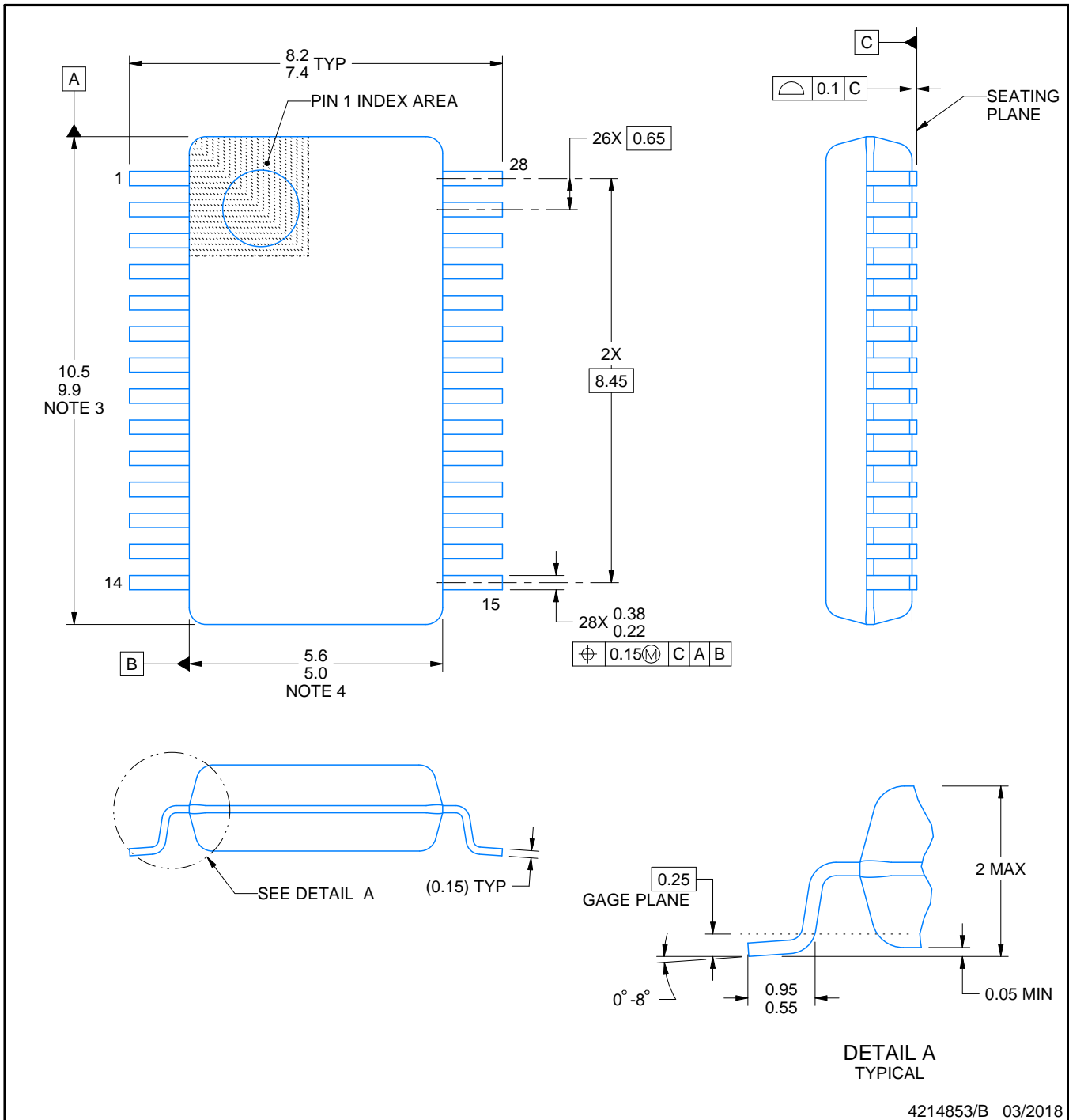
DB0028A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

NOTES:

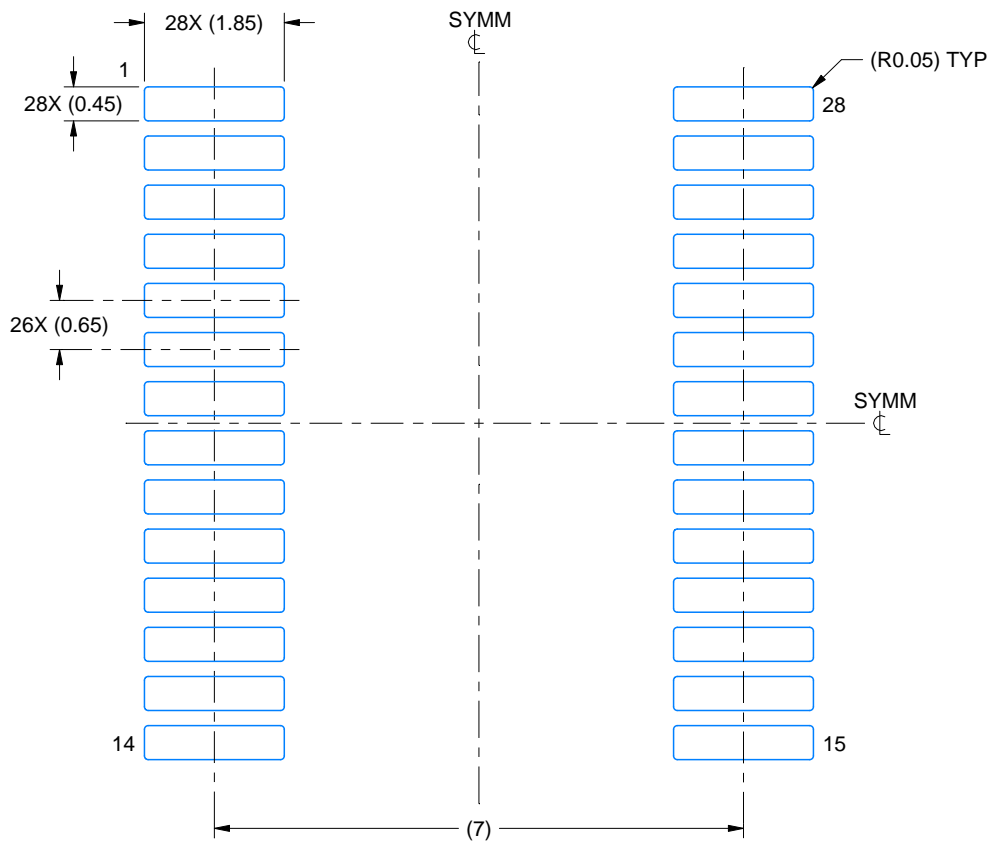
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214853/B 03/2018

NOTES: (continued)

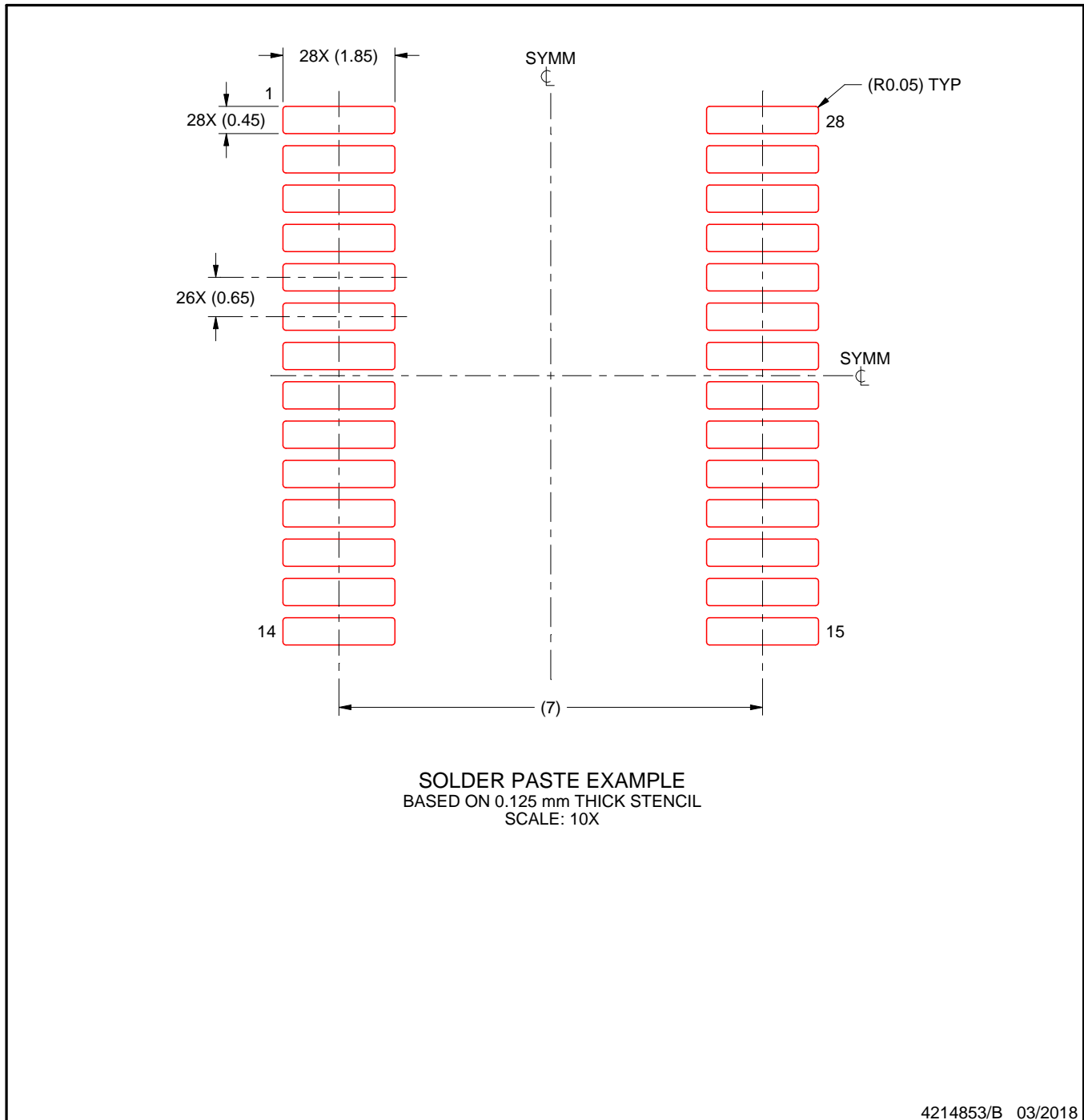
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

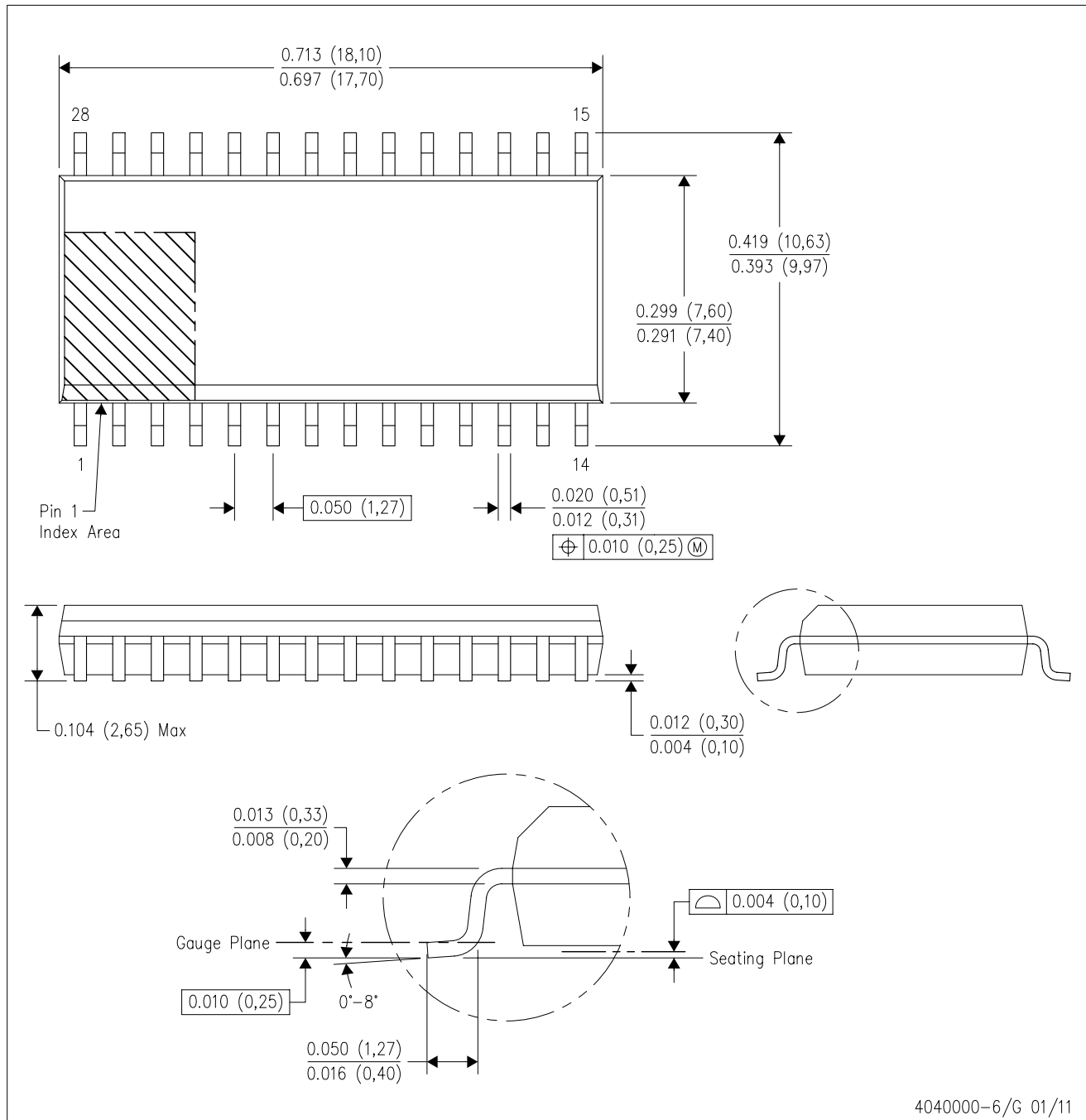


NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G28)

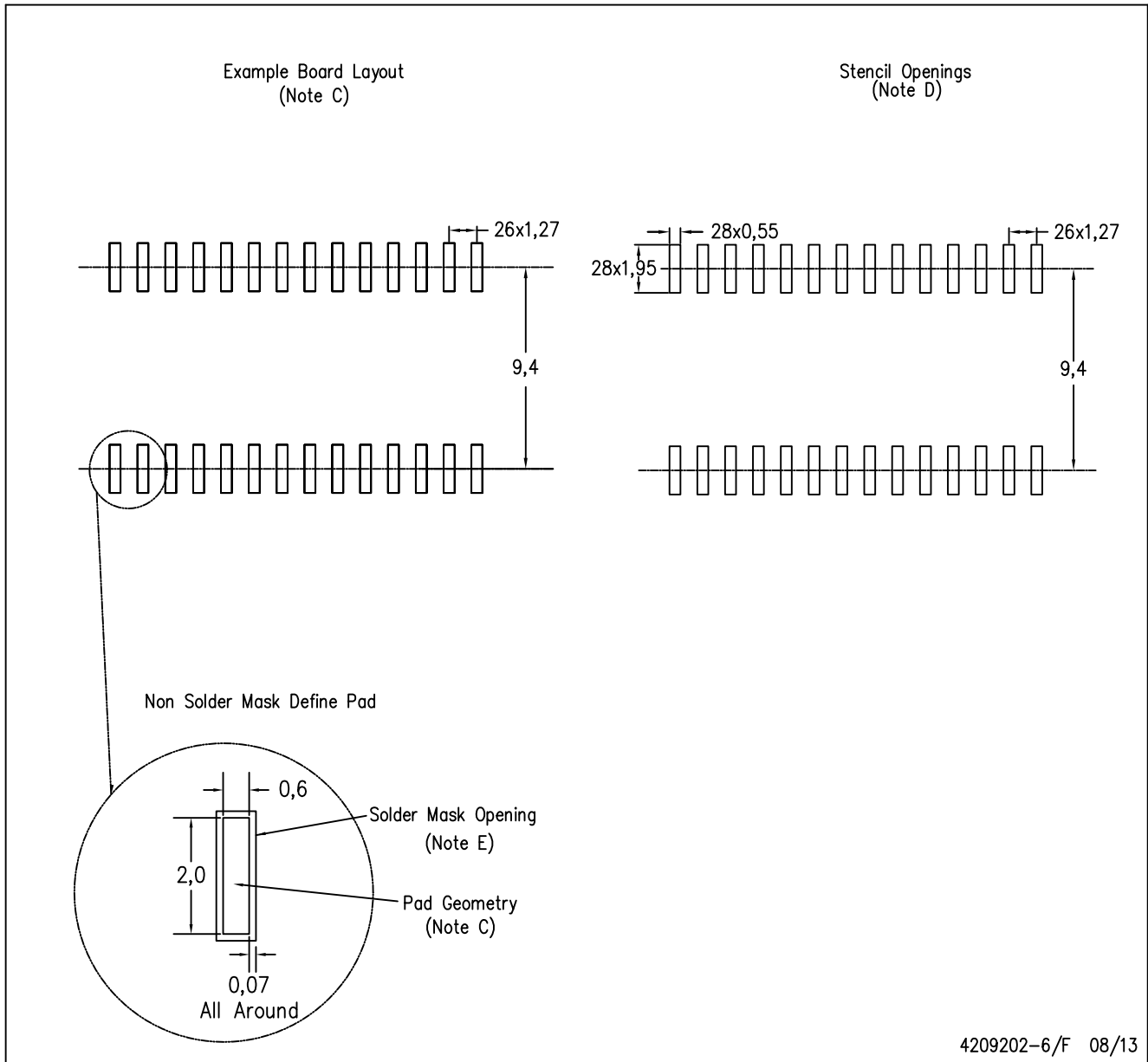
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

DW (R-PDSO-G28)

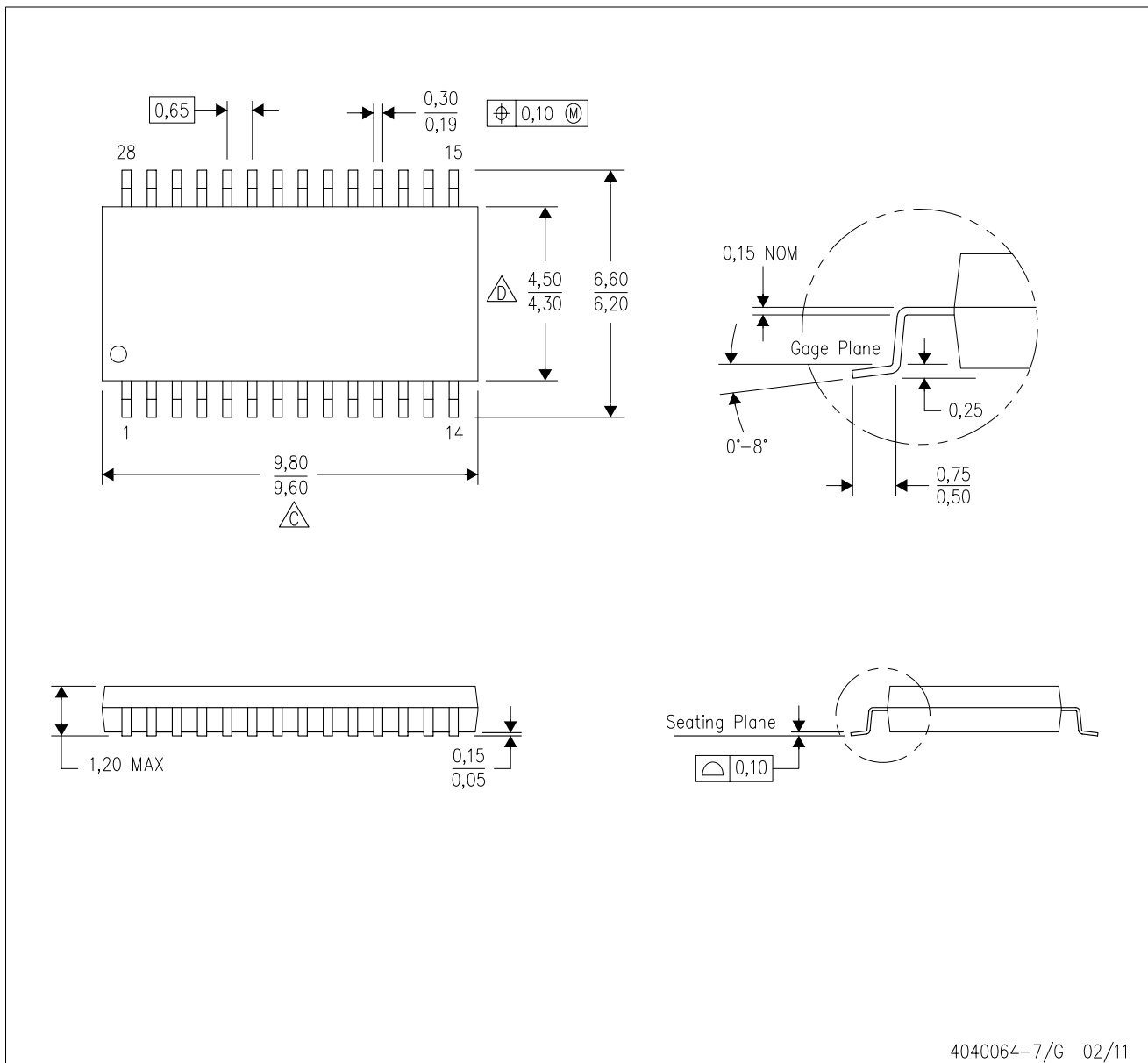
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

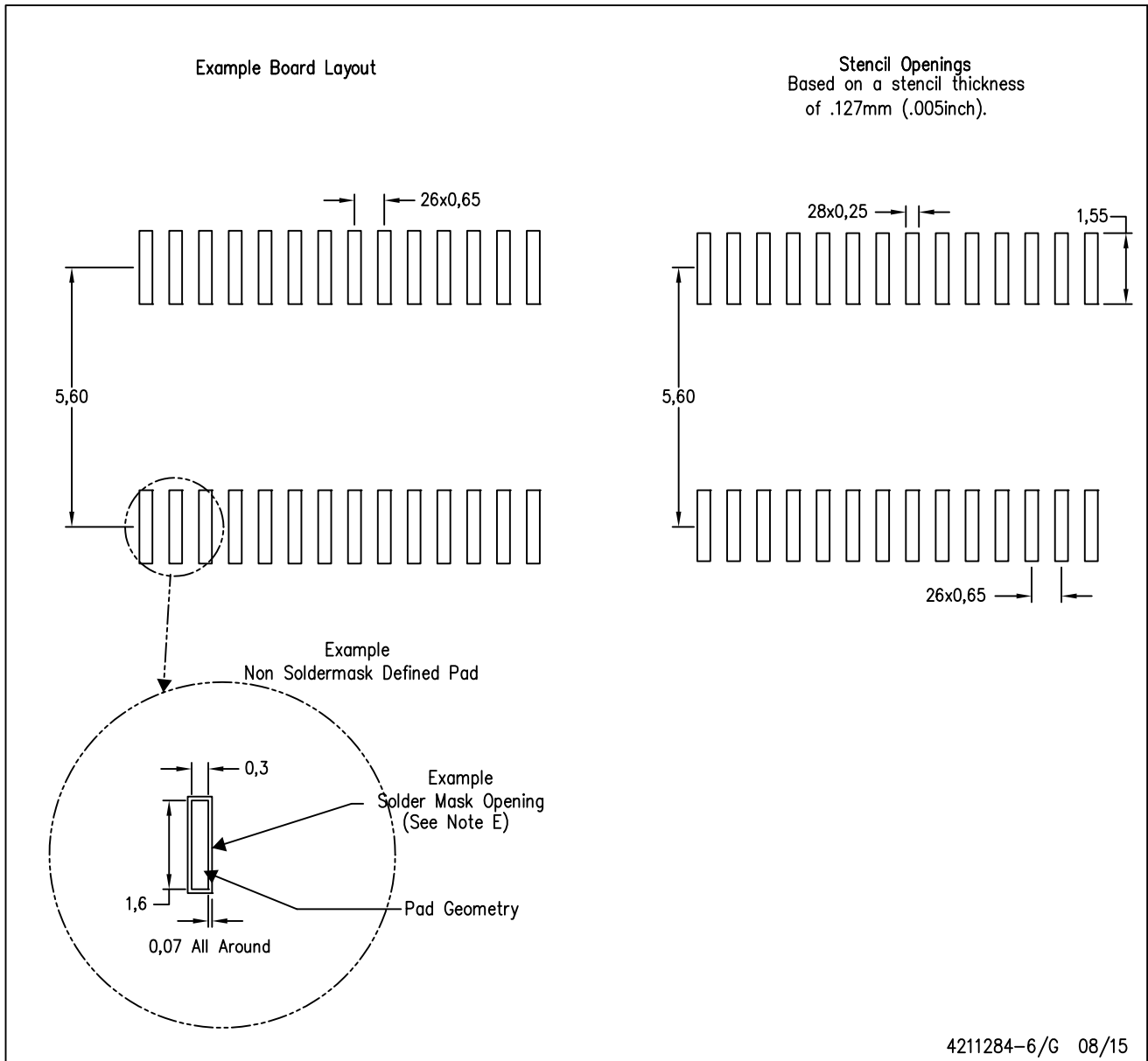


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司