

# 具有故障保护功能的 TCAN1057A-Q1 和 TCAN1057AV-Q1 汽车类 CAN FD 收发器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 (1 级) 标准
- 符合 ISO 11898-2:2016 物理层标准要求
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 支持传统 CAN 和经优化的 CAN FD 性能 (数据速率为 2、5 和 8Mbps)
  - 具有较短的对称传播延迟时间, 可增加时序裕量
- TCAN1057AV I/O 电压范围支持 1.7V 至 5.5V
- 支持 12V 和 24V 电池应用
- 接收器共模输入电压:  $\pm 12V$
- 保护特性:
  - 总线故障保护:  $\pm 58V$
  - 欠压保护
  - TXD 显性超时 (DTO)
    - 数据速率低至 9.2kbps
  - 热关断保护 (TSD)
- 工作模式:
  - 正常模式
  - 静音模式
- 优化了未上电时的性能
  - 总线和逻辑引脚为高阻抗 (运行总线或应用上无负载)
  - 支持热插拔: 在总线和 RXD 输出上可实现上电/断电无干扰运行
- 结温范围:  $-40^{\circ}C$  至  $150^{\circ}C$
- 采用 SOIC (8)、SOT-23 (8) 和无引线 VSON (8) 封装, 具有改善的自动光学检测 (AOI) 功能

## 2 应用

- 汽车和运输
  - 车身控制模块
  - 汽车网关
  - 高级驾驶辅助系统 (ADAS)
  - 信息娱乐系统

## 3 说明

TCAN1057A-Q1 和 TCAN1057AV-Q1 是高速控制器局域网 (CAN) 收发器, 满足 ISO 11898-2:2016 高速 CAN 规范的物理层要求。

此类收发器具有经过认证的电磁兼容性 (EMC), 是数据速率高达 5 兆位/秒 (Mbps) 的传统 CAN 和 CAN FD 网络的理想选择。这些器件可以在更简单的网络中实现高达 8Mbps 的运行速度。收发器支持两种工作模式: 正常模式和静音模式。这些收发器还具有很多保护和诊断功能, 包括热关断 (TSD)、TXD 显性超时 (DTO) 和高达  $\pm 58V$  的总线故障保护, 并且定义了电源欠压或引脚悬空情况下的失效防护行为。

收发器具有通过  $V_{IO}$  引脚实现的集成电平转换器, 该电平转换器提供内部逻辑电平转换功能, 允许将收发器 I/O 直接连接到 1.8V、2.5V、3.3V 或 5V 逻辑电平。

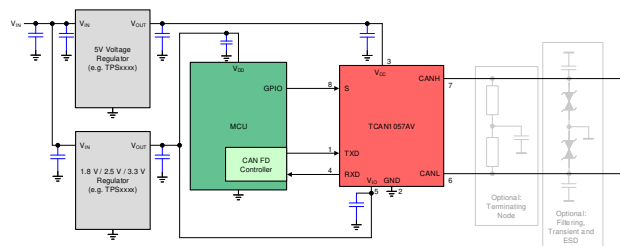
### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
TCAN1057A-Q1 TCAN1057AV-Q1	SOT-23 (DDF) (8)	2.90mm x 1.60mm
	VSON (DRB) (8)	3.00mm x 3.00mm
	SOIC (D) (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

表 3-1. 器件比较表

器件型号	引脚 5 上支持低电压 I/O 逻辑	引脚 8 模式选择
TCAN1057A-Q1	否	静音模式
TCAN1057AV-Q1	有	静音模式



简化版原理图



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

### Changes from Revision A (May 2021) to Revision B (November 2021) Page

- 删除了 *器件信息* 表中 DFF 和 D 封装的产品预发布..... 1

### Changes from Revision \* (February 2021) to Revision A (May 2021) Page

- 将文档状态从：*预告信息* 更改为*量产数据*..... 1

## 5 Pin Configuration and Functions

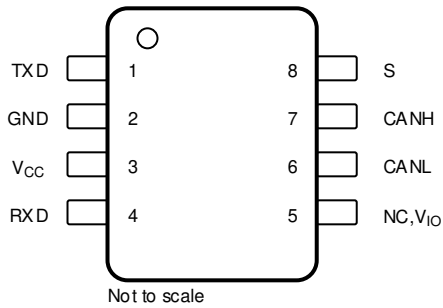


图 5-1. DDF Package, 8-Pin SOT, Top View

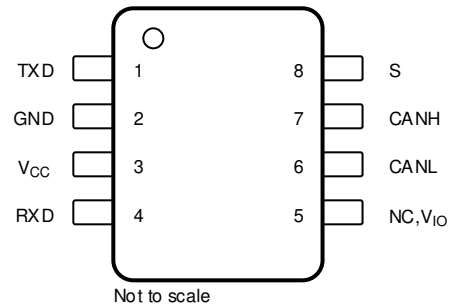


图 5-2. D Package, 8-Pin SOIC, Top View

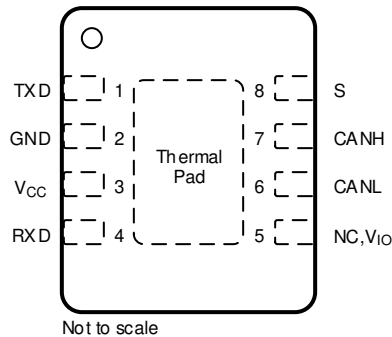


图 5-3. DRB Package, 8-Pin VSON, Top View

表 5-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD	1	Digital Input	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V <sub>CC</sub>	3	Supply	5-V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-state when powered off
NC	5	—	No connect (not internally connected); devices without V <sub>IO</sub>
V <sub>IO</sub>		Supply	I/O supply voltage
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
S	8	Digital Input	Silent mode control input, integrated pull-up
Thermal Pad (VSON only)		—	Connect the thermal pad to any internal PCB ground plane using multiple vias for optimal thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	- 0.3	6	V
V <sub>IO</sub>	Supply voltage I/O level shifter	- 0.3	6	V
V <sub>BUS</sub>	CAN Bus I/O voltage	- 58	58	V
V <sub>DIFF</sub>	Max differential voltage between CANH and CANL	- 45	45	V
V <sub>Logic_Input</sub>	Logic input terminal voltage	- 0.3	6	V
V <sub>RXD</sub>	RXD output terminal voltage range	- 0.3	6	V
I <sub>O(RXD)</sub>	RXD output current	- 8	8	mA
T <sub>J</sub>	Junction temperature	- 40	165	°C
T <sub>STG</sub>	Storage temperature	- 65	150	°C

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>ESD</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
			HBM classification level 3A for all pins	
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±10000
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins	±750	V

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 ESD Ratings Table — IEC Specifications

			VALUE	UNIT	
V <sub>ESD</sub>	System level Electrostatic discharge <sup>(1)</sup>	CAN bus terminals (CANH and CANL) to GND	Unpowered contact discharge per ISO10605 <sup>(1)</sup>	±8000	V
			SAE J2962-2 per ISO 10605 Powered Contact Discharge <sup>(2)</sup>	±8000	V
			SAE J2962-2 per ISO 10605 Powered Air Discharge <sup>(2)</sup>	±15000	V
V <sub>Tran</sub>	Transient voltage per ISO 7637-2 <sup>(3)</sup>		Pulse 1	- 100	V
			Pulse 2a	75	V
			Pulse 3a	- 150	V
			Pulse 3b	100	V
			Transient voltage per ISO 7637-3 <sup>(4)</sup>		
			DCC slow transient pulse	±30	V

- Tested according to IEC 62228-3:2019 CAN Transceivers.
- Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent third party, EMC report available upon request.
- Tested according to IEC 62228-3:2019 CAN Transceivers.
- Tested according to SAE J2962-2.

### 6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V

## 6.4 Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
V <sub>IO</sub>	Supply voltage for I/O level shifter	1.7		5.5	V
I <sub>OH(RXD)</sub>	RXD terminal high-level output current, Devices with V <sub>IO</sub>	- 1.5			mA
I <sub>OL(RXD)</sub>	RXD terminal low-level output current, Devices with V <sub>IO</sub>			1.5	mA
I <sub>OH(RXD)</sub>	RXD terminal high-level output current, Devices without V <sub>IO</sub>	- 2			mA
I <sub>OL(RXD)</sub>	RXD terminal low-level output current, Devices without V <sub>IO</sub>			2	mA
T <sub>J</sub>	Operating junction temperature	-40		150	°C

## 6.5 Thermal Characteristics

THERMAL METRIC <sup>(1)</sup>		TCAN1057Ax-Q1			UNIT
		D (SOIC)	DDF (SOT)	DRB (VSON)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	127.5	122	55.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	67.6	63	62.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	70.9	42.4	27.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	19.3	2.4	2.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	70.2	42.2	27.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	--	--	11.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Supply Characteristics

Over recommended operating conditions with T<sub>J</sub> = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I <sub>CC</sub>	Supply current Normal mode	Dominant	TXD = 0 V, S = 0 V, R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open; See <a href="#">Figure 7-1</a>		45	70	mA
			TXD = 0 V, S = 0 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = open; See <a href="#">Figure 7-1</a>		49	80	mA
		Recessive	TXD = V <sub>CC</sub> or V <sub>IO</sub> , S = 0 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = open; See <a href="#">Figure 7-1</a>		4.5	7.5	mA
		Dominant with bus fault	TXD = 0 V, S = 0 V, CANH = CANL = ±25 V, R <sub>L</sub> = open, C <sub>L</sub> = open; See <a href="#">Figure 7-1</a>			130	mA
	Supply current Silent mode		TXD = S = V <sub>CC</sub> or V <sub>IO</sub> , R <sub>L</sub> = 50 Ω, C <sub>L</sub> = open; See <a href="#">Figure 7-1</a>			2.1	mA
I <sub>IO</sub>	I/O supply current Normal mode, Devices with V <sub>IO</sub>	Dominant	S = 0 V, TXD = 0 V RXD floating		125	300	μA
		Recessive	TXD = V <sub>IO</sub> , S = 0 V RXD floating		25	48	μA
UV <sub>CC</sub>	Rising undervoltage detection on V <sub>CC</sub> for protected mode				4.2	4.4	V
	Falling undervoltage detection on V <sub>CC</sub> for protected mode			3.5	4	4.25	V
V <sub>HYS(UVCC)</sub>	Hysteresis voltage on UV <sub>CC</sub>				200		mV
UV <sub>VIO</sub>	Rising undervoltage detection on V <sub>IO</sub> (Devices with V <sub>IO</sub> )				1.56	1.65	V
	Falling undervoltage detection on V <sub>IO</sub> (Devices with V <sub>IO</sub> )			1.4	1.51	1.59	V
V <sub>HYS(UVIO)</sub>	Hysteresis voltage on UV <sub>IO</sub>				40		mV

## 6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub>	Average power dissipation Normal mode	V <sub>CC</sub> = 5 V, V <sub>IO</sub> = 1.8 V, T <sub>J</sub> = 27°C, R <sub>L</sub> = 60 Ω, TXD input = 250 kHz 50% duty cycle square wave, C <sub>L_RXD</sub> = 15 pF		95		mW
		V <sub>CC</sub> = 5 V, V <sub>IO</sub> = 3.3 V, T <sub>J</sub> = 27°C, R <sub>L</sub> = 60 Ω, TXD input = 250 kHz 50% duty cycle square wave, C <sub>L_RXD</sub> = 15 pF		95		mW
		V <sub>CC</sub> = 5 V, V <sub>IO</sub> = 5 V, T <sub>J</sub> = 27°C, R <sub>L</sub> = 60 Ω, TXD input = 250 kHz 50% duty cycle square wave, C <sub>L_RXD</sub> = 15 pF		95		mW
		V <sub>CC</sub> = 5.5 V, V <sub>IO</sub> = 1.8 V, T <sub>A</sub> = 150°C, R <sub>L</sub> = 60 Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C <sub>L_RXD</sub> = 15 pF		120		mW
		V <sub>CC</sub> = 5.5 V, V <sub>IO</sub> = 3.3 V, T <sub>A</sub> = 150°C, R <sub>L</sub> = 60 Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C <sub>L_RXD</sub> = 15 pF		120		mW
		V <sub>CC</sub> = 5.5 V, V <sub>IO</sub> = 5 V, T <sub>A</sub> = 150°C, R <sub>L</sub> = 60 Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C <sub>L_RXD</sub> = 15 pF		120		mW
T <sub>TSD</sub>	Thermal shutdown temperature		175	195	210	°C
T <sub>TSD(HYS)</sub>	Thermal shutdown hysteresis			12		

## 6.8 Electrical Characteristics

Over recommended operating conditions with T<sub>J</sub> = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>Driver Electrical Characteristics</b>								
V <sub>O(DOM)</sub>	Dominant output voltage Normal mode	CANH	S = 0 V, TXD = 0 V		2.75	4.5	V	
		CANL	50 Ω ≤ R <sub>L</sub> ≤ 65 Ω, C <sub>L</sub> = open, R <sub>CM</sub> = open; See <a href="#">Fig 7-2</a>		0.5	2.25	V	
V <sub>O(REC)</sub>	Recessive output voltage Normal or silent mode	CANH and CANL	S = 0 V, TXD = V <sub>IO</sub> R <sub>L</sub> = open (no load), R <sub>CM</sub> = open See <a href="#">Fig 7-2</a>		2	0.5 V <sub>CC</sub>	3	V
V <sub>SYM</sub>	Driver symmetry (V <sub>O(CANH)</sub> + V <sub>O(CANL)</sub> )/V <sub>CC</sub>		S = 0 V, TXD = 250 kHz, 1 MHz, 2.5 MHz R <sub>L</sub> = 60 Ω, C <sub>SPLIT</sub> = 4.7 nF, C <sub>L</sub> = open, R <sub>CM</sub> = open; See <a href="#">Fig 7-2</a> and <a href="#">Fig 9-2</a>		0.9		1.1	V/V
V <sub>SYM_DC</sub>	DC output symmetry (V <sub>CC</sub> - V <sub>O(CANH)</sub> - V <sub>O(CANL)</sub> )		S = 0 V R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open; See <a href="#">Fig 7-2</a>		-400		400	mV
V <sub>OD(DOM)</sub>	Differential output voltage Normal mode Dominant	CANH - CANL	S = 0 V, TXD = 0 V 50 Ω ≤ R <sub>L</sub> ≤ 65 Ω, C <sub>L</sub> = open; See <a href="#">Fig 7-2</a>		1.5		3	V
			S = 0 V, TXD = 0 V 45 Ω ≤ R <sub>L</sub> ≤ 70 Ω, C <sub>L</sub> = open; See <a href="#">Fig 7-2</a>		1.4		3.3	V
			S = 0 V, TXD = 0 V R <sub>L</sub> = 2240 Ω, C <sub>L</sub> = open; See <a href="#">Fig 7-2</a>		1.5		5	V
V <sub>OD(REC)</sub>	Differential output voltage Normal mode Recessive	CANH - CANL	S = 0 V, TXD = V <sub>IO</sub> R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open; See <a href="#">Fig 7-2</a>		-120		12	mV
			S = 0 V, TXD = V <sub>IO</sub> R <sub>L</sub> = open, C <sub>L</sub> = open; See <a href="#">Fig 7-2</a>		-50		50	mV
I <sub>OS(SS_DOM)</sub>	Short-circuit steady-state output current, dominant Normal mode		S = 0 V, TXD = 0 V V <sub>(CANH)</sub> = -15 V to 40 V, CANL = open; See <a href="#">Fig 7-7</a>		-115			mA
			S = 0 V, TXD = 0 V V <sub>(CANL)</sub> = -15 V to 40 V, CANH = open; See <a href="#">Fig 7-7</a>				115	mA

## 6.8 Electrical Characteristics (continued)

 Over recommended operating conditions with  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive Normal mode	$S = 0\text{ V}$ , $TXD = V_{IO}$ $-27\text{ V} \leq V_{BUS} \leq 32\text{ V}$ , where $V_{BUS} =$ $CANH = CANL$ ; See <a href="#">图 7-7</a>	-5		5	mA
<b>Receiver Electrical Characteristics</b>						
$V_{IT}$	Input threshold voltage Normal and silent mode	$S = 0\text{ V}$ , $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ ; See <a href="#">图 7-3</a> and <a href="#">表 8-6</a>	500		900	mV
$V_{DOM}$	Dominant state differential input voltage range Normal and silent mode	$S = 0\text{ V}$ , $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ ; See <a href="#">图 7-3</a> and <a href="#">表 8-6</a>	0.9		9	V
$V_{REC}$	Recessive state differential input voltage range Normal and silent mode	$S = 0\text{ V}$ , $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ ; See <a href="#">图 7-3</a> and <a href="#">表 8-6</a>	-4		0.5	V
$V_{HYS}$	Hysteresis voltage for input threshold Normal mode	$S = 0\text{ V}$ , $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ ; See <a href="#">图 7-3</a> and <a href="#">表 8-6</a>		115		mV
$V_{CM}$	Common-mode range Normal and silent mode	See <a href="#">图 7-3</a> and <a href="#">表 8-6</a>	-12		12	V
$I_{LKG(OFF)}$	Unpowered bus input leakage current	$CANH = CANL = 5\text{ V}$ , $V_{CC} = V_{IO} = \text{GND}$			5	$\mu\text{A}$
$C_I$	Input capacitance to ground (CANH or CANL)	$TXD = V_{IO}$ <sup>(1)</sup>			20	pF
$C_{ID}$	Differential input capacitance				10	pF
$R_{ID}$	Differential input resistance	$TXD = V_{IO}$ <sup>(1)</sup> , $S = 0\text{ V}$ , $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$	40		90	k $\Omega$
$R_{IN}$	Single-ended input resistance (CANH or CANL)		20		45	k $\Omega$
$R_{IN(M)}$	Input resistance matching $[1 - (R_{IN(CANH)} / R_{IN(CANL)})] \times 100\%$	$V_{(CAN\_H)} = V_{(CAN\_L)} = 5\text{ V}$	-1		1	%
<b>TXD Terminal (CAN Transmit Data Input)</b>						
$V_{IH}$	High-level input voltage	Devices without $V_{IO}$	0.7 $V_{CC}$			V
$V_{IH}$	High-level input voltage	Devices with $V_{IO}$	0.7 $V_{IO}$			V
$V_{IL}$	Low-level input voltage	Devices without $V_{IO}$			0.3 $V_{CC}$	V
$V_{IL}$	Low-level input voltage	Devices with $V_{IO}$			0.3 $V_{IO}$	V
$I_{IH}$	High-level input leakage current	$TXD = V_{CC} = V_{IO} = 5.5\text{ V}$	-2.5	0	1	$\mu\text{A}$
$I_{IL}$	Low-level input leakage current	$TXD = 0\text{ V}$ $V_{CC} = V_{IO} = 5.5\text{ V}$	-200	-100	-20	$\mu\text{A}$
$I_{LKG(OFF)}$	Unpowered leakage current	$TXD = 5.5\text{ V}$ $V_{CC} = V_{IO} = 0\text{ V}$	-1	0	1	$\mu\text{A}$
$C_I$	Input capacitance	$V_{IN} = 0.4 \times \sin(2\pi \times 2 \times 10^6 \times t) + 2.5\text{ V}$		5		pF
<b>RXD Terminal (CAN Receive Data Output)</b>						
$V_{OH}$	High-level output voltage	$I_O = -2\text{ mA}$ Devices without $V_{IO}$ ; See <a href="#">图 7-3</a>	0.8 $V_{CC}$			V
$V_{OH}$	High-level output voltage	$I_O = -1.5\text{ mA}$ Devices with $V_{IO}$ ; See <a href="#">图 7-3</a>	0.8 $V_{IO}$			V
$V_{OL}$	Low-level output voltage	$I_O = 2\text{ mA}$ Devices without $V_{IO}$ ; See <a href="#">图 7-3</a>			0.2 $V_{CC}$	V
$V_{OL}$	Low-level output voltage	$I_O = 1.5\text{ mA}$ Devices with $V_{IO}$ ; See <a href="#">图 7-3</a>			0.2 $V_{IO}$	V
$I_{LKG(OFF)}$	Unpowered leakage current	$RXD = 5.5\text{ V}$ $V_{CC} = V_{IO} = 0\text{ V}$	-1	0	1	$\mu\text{A}$
<b>S Terminal (Silent Mode Input)</b>						
$V_{IH}$	High-level input voltage	Devices without $V_{IO}$	0.7 $V_{CC}$			V
$V_{IH}$	High-level input voltage	Devices with $V_{IO}$	0.7 $V_{IO}$			V
$V_{IL}$	Low-level input voltage	Devices without $V_{IO}$			0.3 $V_{CC}$	V
$V_{IL}$	Low-level input voltage	Devices with $V_{IO}$			0.3 $V_{IO}$	V

## 6.8 Electrical Characteristics (continued)

Over recommended operating conditions with  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH}$	High-level input leakage current	$V_{CC} = V_{IO} = S = 5.5\text{ V}$	-2		2	$\mu\text{A}$
$I_{IL}$	Low-level input leakage current	$S = 0\text{ V}$ $V_{CC} = V_{IO} = 5.5\text{ V}$ ,	-20		-2	$\mu\text{A}$
$I_{LKG(OFF)}$	Unpowered leakage current	$S = 5.5\text{ V}$ $V_{CC} = V_{IO} = 0\text{ V}$	-1	0	1	$\mu\text{A}$

(1)  $V_{IO} = V_{CC}$  in non-V variants of device

## 6.9 Switching Characteristics

Over recommended operating conditions with  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Device Switching Characteristics</b>						
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	$S = 0\text{ V}$ , $V_{IO} = 2.8\text{ V}$ to $5.5\text{ V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{ pF}$ , $C_{L(RXD)} = 15\text{ pF}$ ; See <a href="#">图 7-4</a>		125	210	ns
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	$S = 0\text{ V}$ , $V_{IO} = 1.7\text{ V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{ pF}$ , $C_{L(RXD)} = 15\text{ pF}$ ; See <a href="#">图 7-4</a>		165	255	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	$S = 0\text{ V}$ , $V_{IO} = 2.8\text{ V}$ to $5.5\text{ V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{ pF}$ , $C_{L(RXD)} = 15\text{ pF}$ ; See <a href="#">图 7-4</a>		150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	$S = 0\text{ V}$ , $V_{IO} = 1.7\text{ V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{ pF}$ , $C_{L(RXD)} = 15\text{ pF}$ ; See <a href="#">图 7-4</a>		180	255	ns
$t_{MODE}$	Mode change time, from normal to standby or from standby to normal	See <a href="#">图 7-5</a>			20	$\mu\text{s}$
<b>Driver Switching Characteristics</b>						
$t_{pHR}$	Propagation delay time, high TXD to driver recessive (dominant to recessive)	$S = 0\text{ V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{ pF}$ ; See <a href="#">图 7-2</a>		80		ns
$t_{pLD}$	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
$t_{sk(p)}$	Pulse skew ( $ t_{pHR} - t_{pLD} $ )			14		ns
$t_R$	Differential output signal rise time			25		ns
$t_F$	Differential output signal fall time			50		ns
$t_{TXD\_DTO}$	Dominant timeout	$S = 0\text{ V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{ pF}$ ; See <a href="#">图 7-6</a>	1.2		4.0	ms
<b>Receiver Switching Characteristics</b>						
$t_{pRH}$	Propagation delay time, bus recessive input to high output (dominant to recessive)	$S = 0\text{ V}$ $C_{L(RXD)} = 15\text{ pF}$ ; See <a href="#">图 7-3</a>		81		ns
$t_{pDL}$	Propagation delay time, bus dominant input to low output (recessive to dominant)			66		ns
$t_R$	RXD output signal rise time			10		ns
$t_F$	RXD output signal fall time			10		ns
<b>FD Timing Characteristics</b>						



## 6.9 Switching Characteristics (continued)

Over recommended operating conditions with  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{BIT(BUS)}}$	Bit time on CAN bus output pins $t_{\text{BIT(TXD)}} = 500 \text{ ns}$	$S = 0 \text{ V}$ $R_L = 60 \Omega, C_L = 100 \text{ pF}, C_{L(\text{RXD})} = 15 \text{ pF}$ $\Delta t_{\text{REC}} = t_{\text{BIT(RXD)}} - t_{\text{BIT(BUS)}}$ ; See <a href="#">图 7-4</a>	450		525	ns
	Bit time on CAN bus output pins $t_{\text{BIT(TXD)}} = 200 \text{ ns}$		160		205	ns
	Bit time on CAN bus output pins $t_{\text{BIT(TXD)}} = 125 \text{ ns}^{(1)}$		85		130	ns
$t_{\text{BIT(RXD)}}$	Bit time on RXD output pins $t_{\text{BIT(TXD)}} = 500 \text{ ns}$		410		540	ns
	Bit time on RXD output pins $t_{\text{BIT(TXD)}} = 200 \text{ ns}$		130		210	ns
	Bit time on RXD output pins $t_{\text{BIT(TXD)}} = 125 \text{ ns}^{(1)}$		75		135	ns
$\Delta t_{\text{REC}}$	Receiver timing symmetry $t_{\text{BIT(TXD)}} = 500 \text{ ns}$		-50		20	ns
	Receiver timing symmetry $t_{\text{BIT(TXD)}} = 200 \text{ ns}$		-40		10	ns
	Receiver timing symmetry $t_{\text{BIT(TXD)}} = 125 \text{ ns}^{(1)}$		-40		10	ns

(1) Measured during characterization and not an ISO 11898-2:2016 parameter.

## 7 Parameter Measurement Information

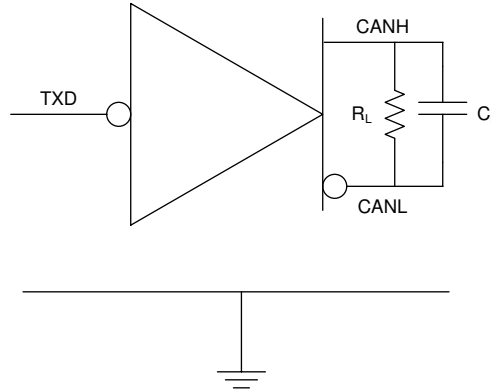


图 7-1.  $I_{CC}$  Test Circuit

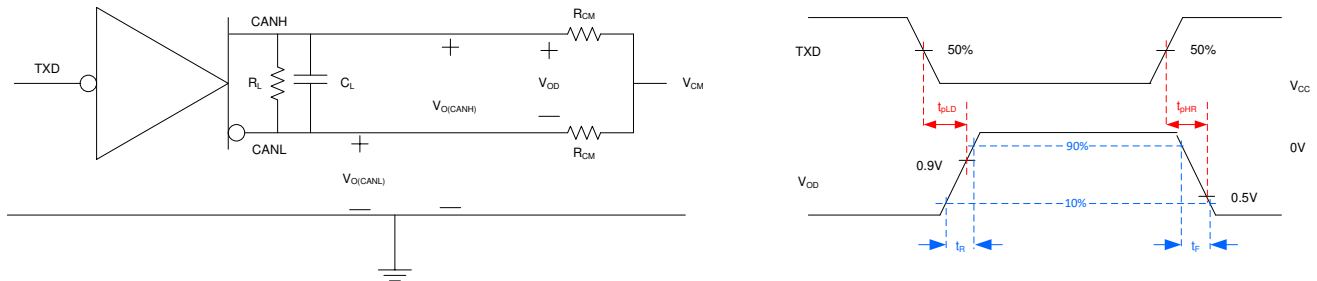


图 7-2. Driver Test Circuit and Measurement

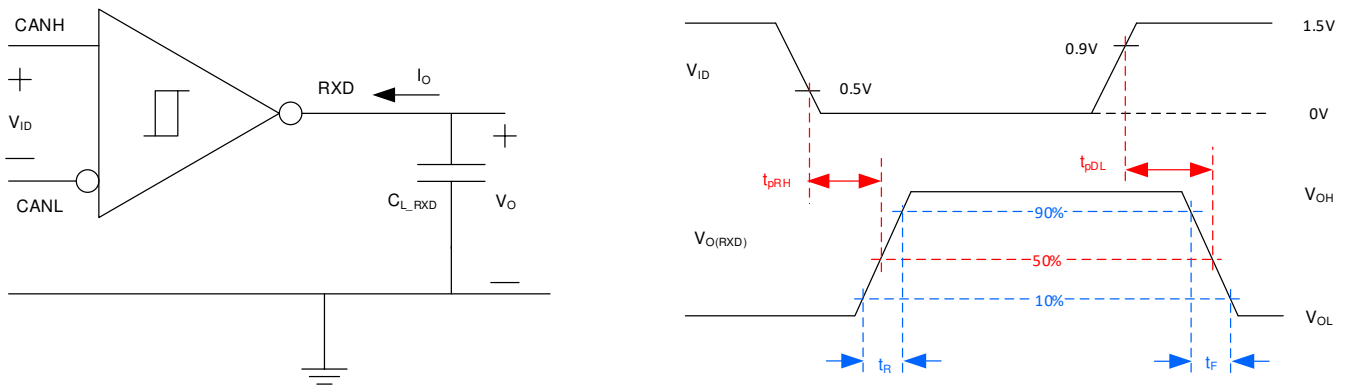
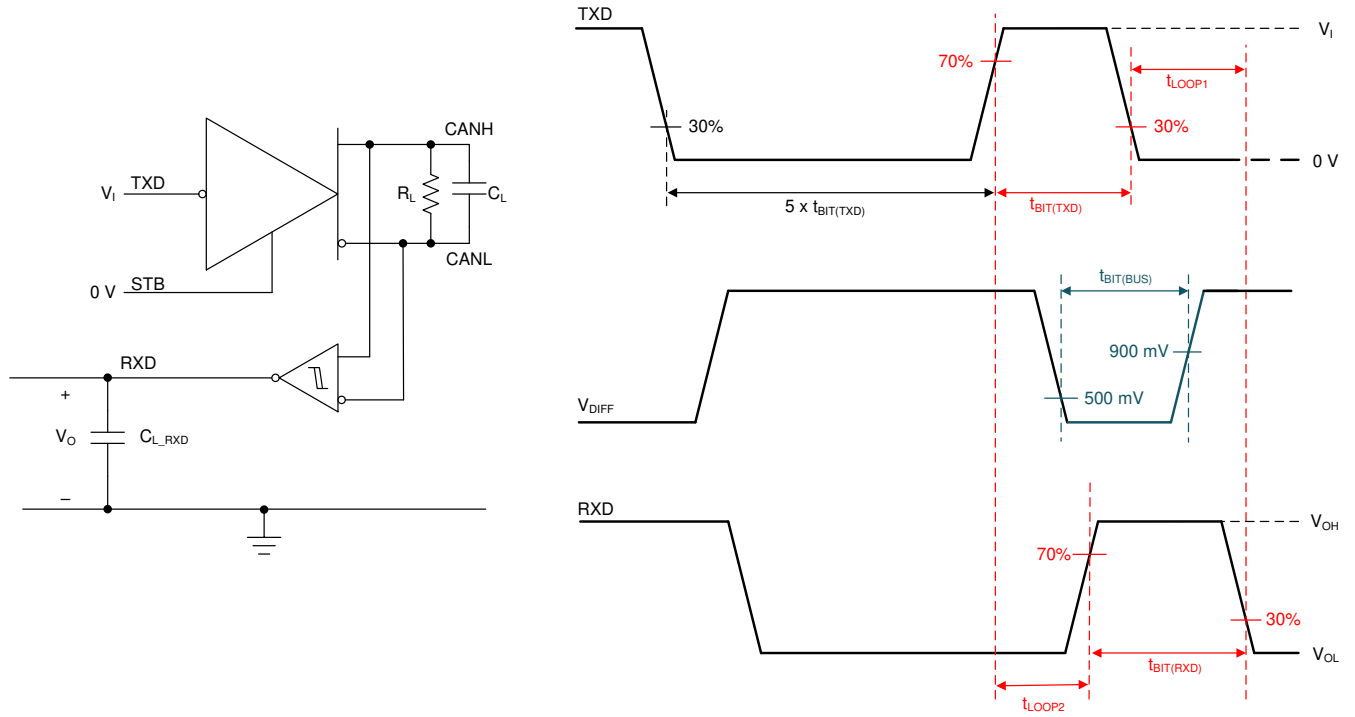
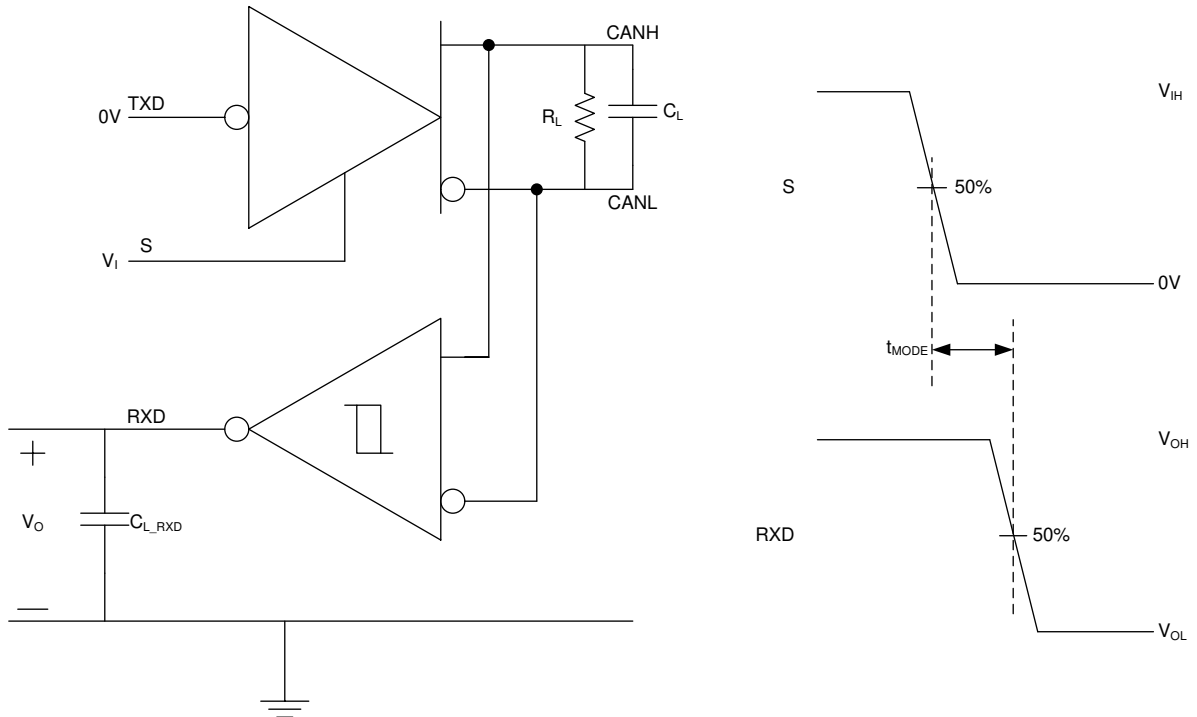


图 7-3. Receiver Test Circuit and Measurement



**图 7-4. Transmitter and Receiver Timing Test Circuit and Measurement**



**图 7-5.  $t_{MODE}$  Test Circuit and Measurement**

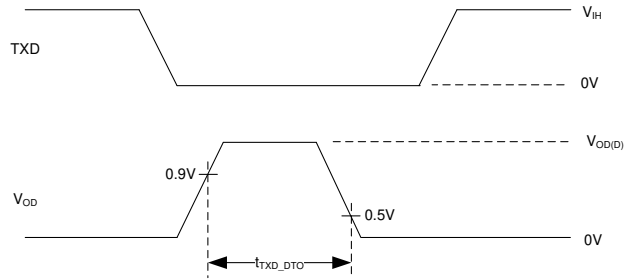
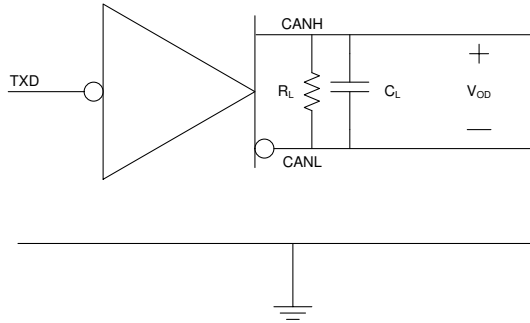


图 7-6. TXD Dominant Timeout Test Circuit and Measurement

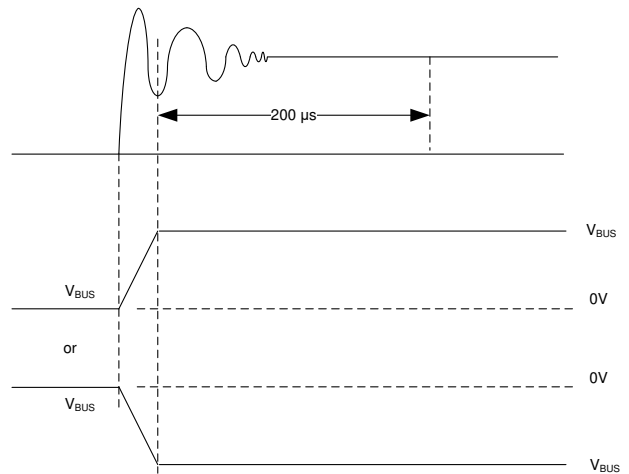
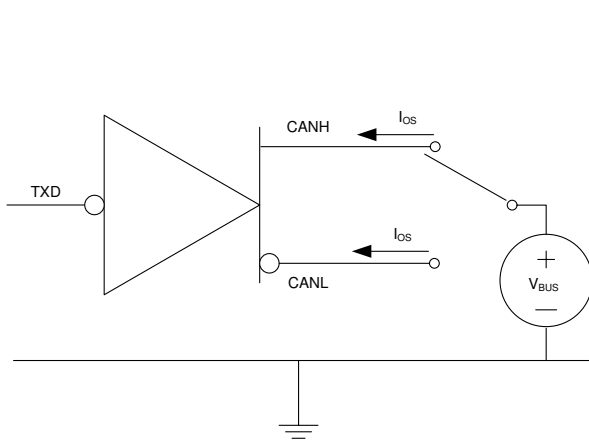


图 7-7. Driver Short-Circuit Current Test and Measurement

## 8 Detailed Description

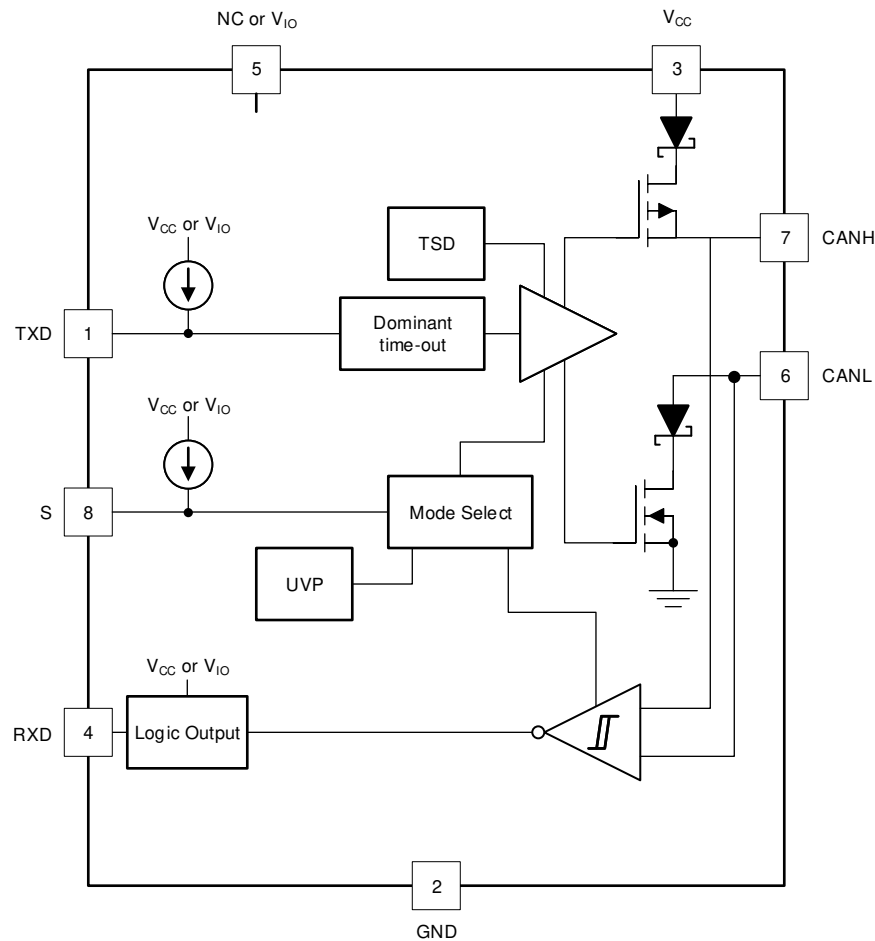
### 8.1 Overview

The TCAN1057A(V)-Q1 devices meet or exceed the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8 Mbps.

The devices support the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2016 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125 kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 2 Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 5 Mbps
- EMC requirements:
  - IEC 62228-3 EMC evaluation of transceivers - CAN transceivers
  - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance Test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Pin Description

#### 8.3.1.1 TXD

The TXD input is a logic-level signal, referenced to either  $V_{CC}$  or  $V_{IO}$  from a CAN controller to the transceivers.

#### 8.3.1.2 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

#### 8.3.1.3 $V_{CC}$

$V_{CC}$  provides the 5-V power supply to the CAN transceiver.

#### 8.3.1.4 RXD

The RXD output is a logic-level signal, referenced to either  $V_{CC}$  or  $V_{IO}$ , from the transceivers to the CAN controller. RXD is only driven once  $V_{IO}$  is present.

#### 8.3.1.5 $V_{IO}$

The  $V_{IO}$  pin is the input source for the integrated level shifter which provides the transceiver I/O voltage. The  $V_{IO}$  pin should be connected to the controller's I/O voltage source.

#### 8.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transmitter and receiver internally.

### 8.3.1.7 S (Silent)

The S pin is an input pin used for silent mode control of the transceiver. The S pin can be supplied from either the controller or from a static system voltage source. If normal mode is the only intended mode of operation than the S pin can be tied directly to system GND using a pull-down resistor. If silent mode is the only intended mode of operation than the S pin can be tied directly to a static system voltage source using a pull-up resistor.

### 8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See 图 8-1.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to  $V_{CC}/2$  via the high-resistance internal input resistors  $R_{IN}$  of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

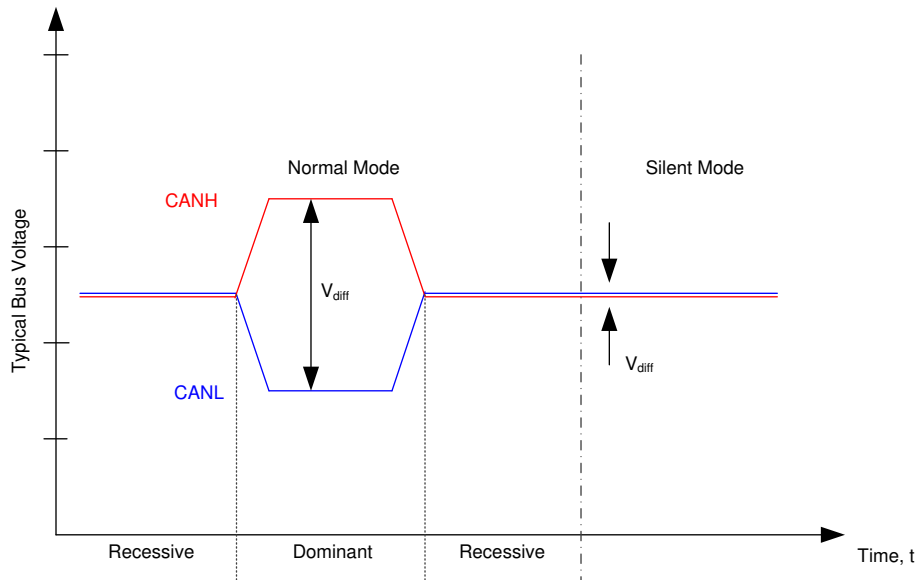


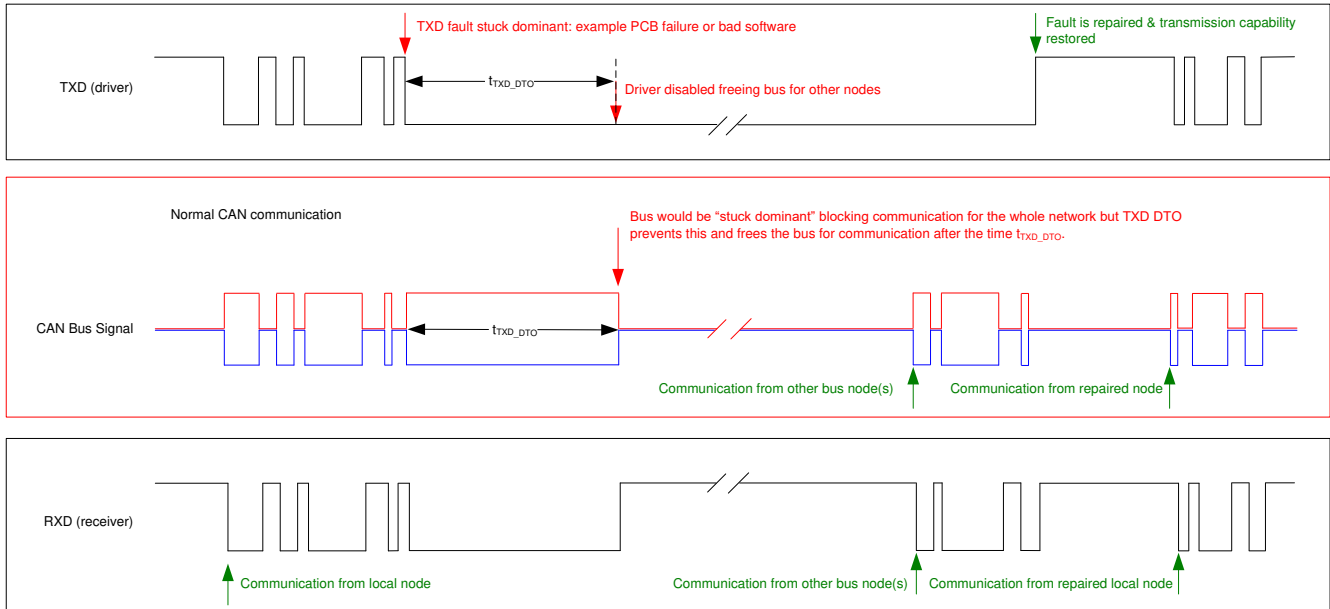
图 8-1. Bus States

### 8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period  $t_{TXD\_DTO}$ . The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit,  $t_{TXD\_DTO}$ , the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to  $V_{CC}/2$  and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using 方程式 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$



**图 8-2. Example Timing Diagram for TXD Dominant Timeout**

### 8.3.4 CAN Bus short-circuit current limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating,  $I_{OS(AVG)}$ , should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using [方程式 2](#).

$$I_{OS(AVG)} = \% \text{ Transmit} \times [(\% \text{ REC\_Bits} \times I_{OS(SS)\_REC}) + (\% \text{ DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\% \text{ Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$  is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC\_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM\_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$  is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$  is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers  $V_{CC}$  supply.



### 8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold,  $T_{TSD}$ , the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below  $T_{TSD}$ . The CAN bus pins are biased to  $V_{CC}/2$  during a TSD fault and the receiver to RXD path remains operational. The device TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

### 8.3.6 Undervoltage Lockout

The supply pins,  $V_{CC}$  and  $V_{IO}$ , have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

**表 8-1. Undervoltage Lockout - TCAN1057A-Q1**

$V_{CC}$	DEVICE STATE	BUS	RXD PIN
$> UV_{VCC}$	Normal	Per TXD	Mirrors bus
$< UV_{VCC}$	Protected	High impedance Weak pull-down to ground <sup>(1)</sup>	High impedance

(1)  $V_{CC} = GND$ , see  $I_{LKG(OFF)}$

**表 8-2.  $V_{IO}$  Undervoltage Lockout - TCAN1057AV-Q1**

$V_{CC}$	$V_{IO}$	DEVICE STATE	BUS	RXD PIN
$> UV_{VCC}$	$> UV_{VIO}$	Normal	Per TXD	Mirrors bus
$< UV_{VCC}$	$> UV_{VIO}$	$S = V_{IO}$ : Silent mode	High impedance Weak pull-down to ground <sup>(1)</sup>	Recessive
		$S = GND$ : Protected mode		High impedance
$> UV_{VCC}$	$< UV_{VIO}$	Protected		High impedance
$< UV_{VCC}$	$< UV_{VIO}$	Protected		High impedance

(1)  $V_{CC} = GND$ , see  $I_{LKG(OFF)}$

Once the undervoltage condition is cleared and  $t_{MODE}$  has expired the device transitions to normal mode and the host controller can send and receive CAN traffic again.

### 8.3.7 Unpowered Device

The device is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

### 8.3.8 Floating pins

The device has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See [表 8-3](#) for details on pin bias conditions.

**表 8-3. Pin Bias**

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
S	Pull-up	Weakly biases S towards low-power silent mode to prevent excessive system power

## 8.4 Device Functional Modes

### 8.4.1 Operating Modes

The device has two main operating modes; normal mode and silent mode. Operating mode selection is made by applying a high or low level to the S pin.

表 8-4. Operating Modes

S	Device Mode	Driver	Receiver	RXD Pin
High	Silent mode	Disabled	Enabled	Mirrors bus state
Low	Normal Mode	Enabled	Enabled	

### 8.4.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

### 8.4.3 Silent Mode

In silent mode the CAN driver is disabled and the high-speed CAN receiver is enabled. CAN communication is unidirectional into the device where the receiver is translating the differential signal from CANH and CANL to a digital output on RXD. The power consumption of the TCAN1057A(V)-Q1 is reduced in silent mode due to the CAN driver being disabled.

### 8.4.4 Driver and Receiver Function

The digital input and output levels for the device are CMOS levels with respect to either  $V_{CC}$  or  $V_{IO}$ .

表 8-5. Driver Function Table

Device Mode	TXD Input <sup>(1)</sup>	Bus Outputs		Driven Bus State <sup>(2)</sup>
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Silent	X	High impedance	High impedance	Biased recessive

(1) X = irrelevant

(2) For bus state see [图 8-1](#)

表 8-6. Receiver Function Table Normal and Silent Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal or Silent	$V_{ID} \geq 0.9 \text{ V}$	Dominant	Low
	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	Undefined	Undefined
	$V_{ID} \leq 0.5 \text{ V}$	Recessive	High
Any	Open ( $V_{ID} \approx 0 \text{ V}$ )	Open	High

## 9 Application Information Disclaimer

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

### 9.2 Typical Application

图 9-1 shows a typical configuration for 5 V system using the device. The bus termination is shown for illustrative purposes.

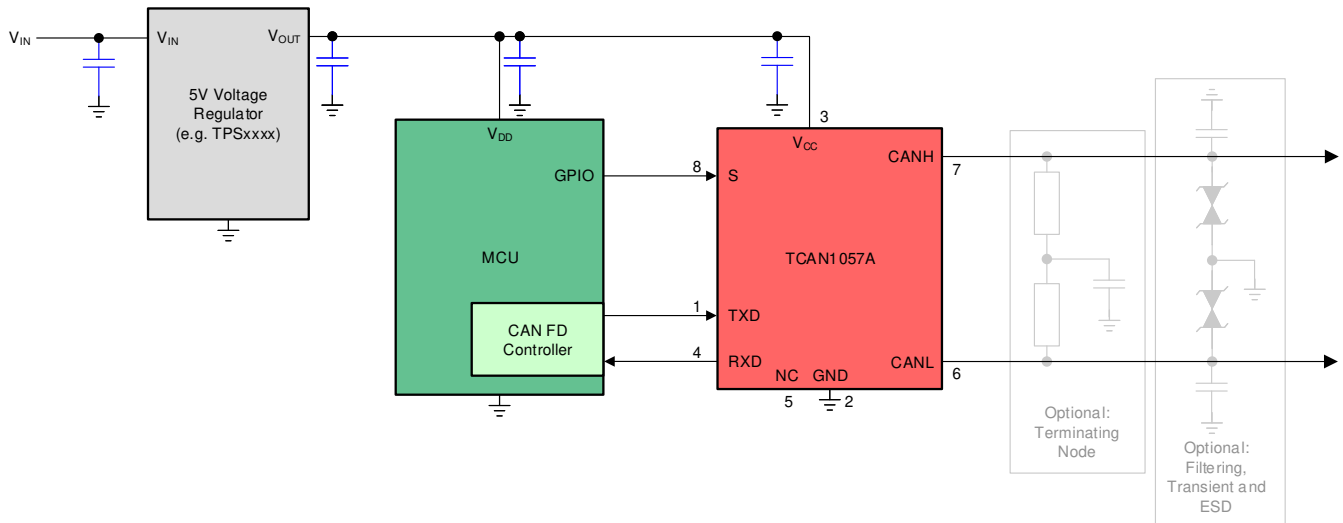


图 9-1. Transceiver Application Using 5 V I/O Connections

## 9.2.1 Design Requirements

### 9.2.1.1 CAN Termination

Termination may be a single  $120\text{-}\Omega$  resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see [Figure 9-2](#). Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

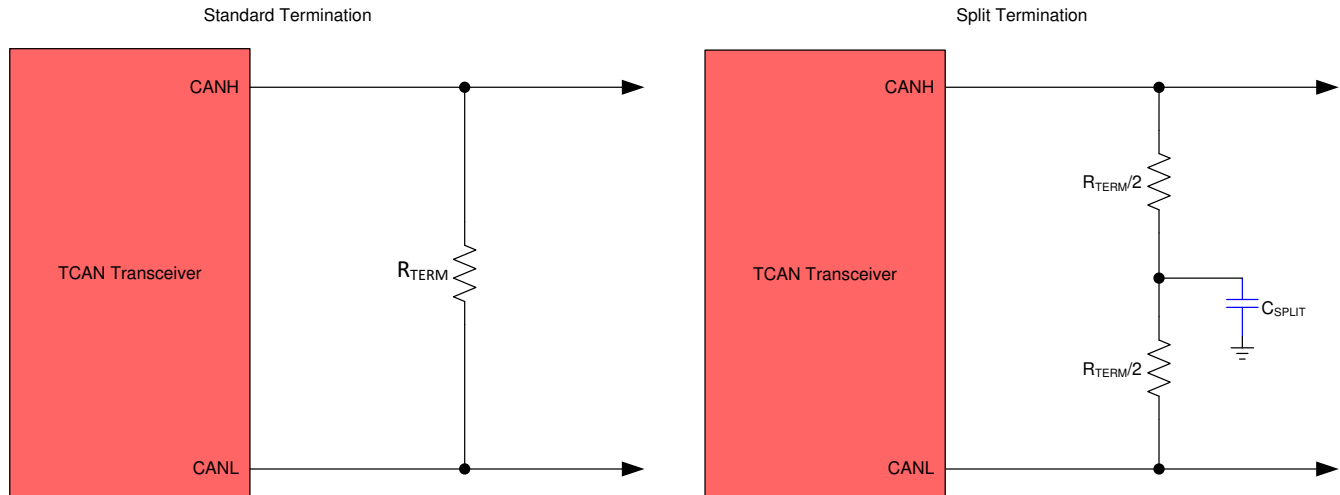


图 9-2. CAN Bus Termination Concepts

## 9.2.2 Detailed Design Procedures

### 9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 meters. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1057A(V)-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from  $50\ \Omega$  to  $65\ \Omega$  where the differential output must be greater than 1.5 V. The TCAN1057A(V)-Q1 family is specified to meet the 1.5-V requirement down to  $50\ \Omega$  and is specified to meet 1.4-V differential output at  $45\ \Omega$  bus load. The differential input resistance of the transceiver is a minimum of  $40\ \text{k}\Omega$ . If 100 transceivers are in parallel on a bus, this is equivalent to a  $400\text{-}\Omega$  differential load in parallel with the nominal  $60\ \Omega$  bus termination which gives a total bus load of approximately  $52\ \Omega$ . Therefore, the TCAN1057A(V)-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

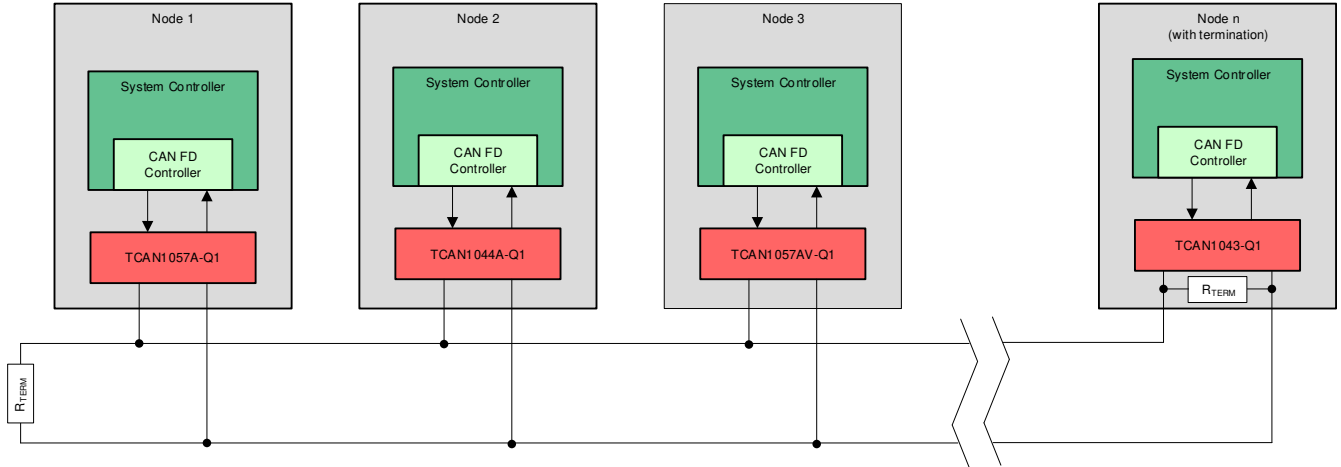


图 9-3. Typical CAN Bus

### 9.2.3 Application Curves

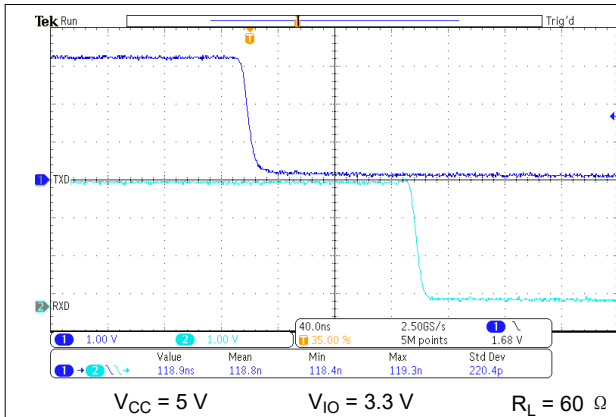


图 9-4.  $t_{PROP(LOOP1)}$

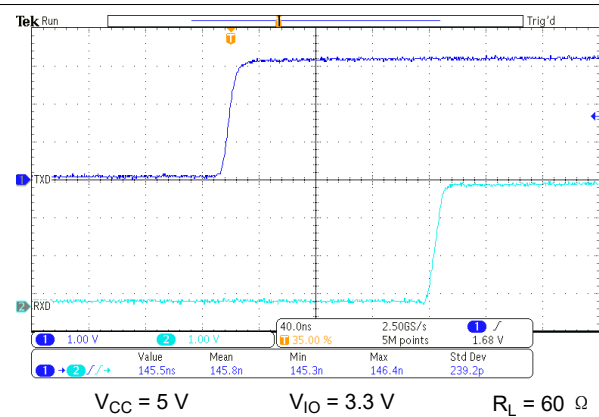


图 9-5.  $t_{PROP(LOOP2)}$

## 9.2.4 System Examples

图 9-6 shows a typical configuration for 1.8 V, 2.5 V, or 3.3 V systems using the TCAN1057AV. The bus termination is shown for illustrative purposes.

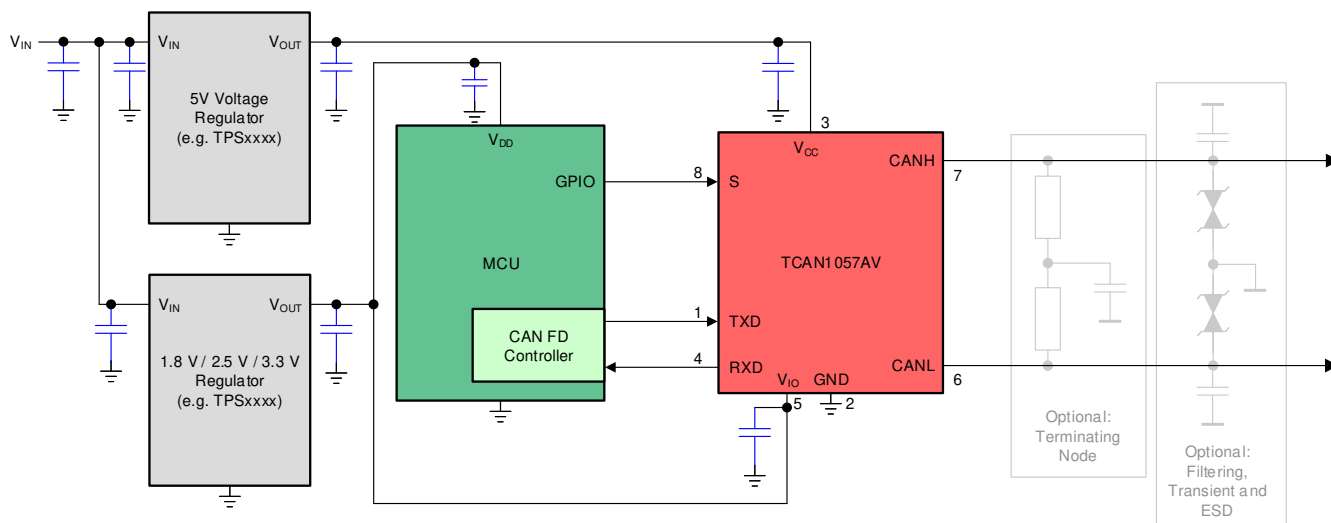


图 9-6. Typical Transceiver Application Using 1.8 V, 2.5 V, 3.3 V IO Connections

## 10 Power Supply Recommendations

The TCAN1057A transceiver is designed to operate with a main  $V_{CC}$  input voltage supply range between 4.5 V and 5.5 V. The TCAN1057AV implements an I/O level shifting supply input,  $V_{IO}$ , designed for a range between 1.7 V and 5.5 V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100 nF, should be placed near the CAN transceiver's main  $V_{CC}$  supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100 nF, should be placed near the CAN transceiver's  $V_{IO}$  supply pin in addition to bypass capacitors.

## Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

### 11.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins  $V_{CC}$  and  $V_{IO}$  of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

#### 备注

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R4 and R5, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common-mode filtering for the bus. See [CAN Termination](#), [CAN Bus Short Circuit Current Limiting](#), and [方程式 2](#) for information on termination concepts and power ratings needed for the termination resistor(s).

### 11.2 Layout Example

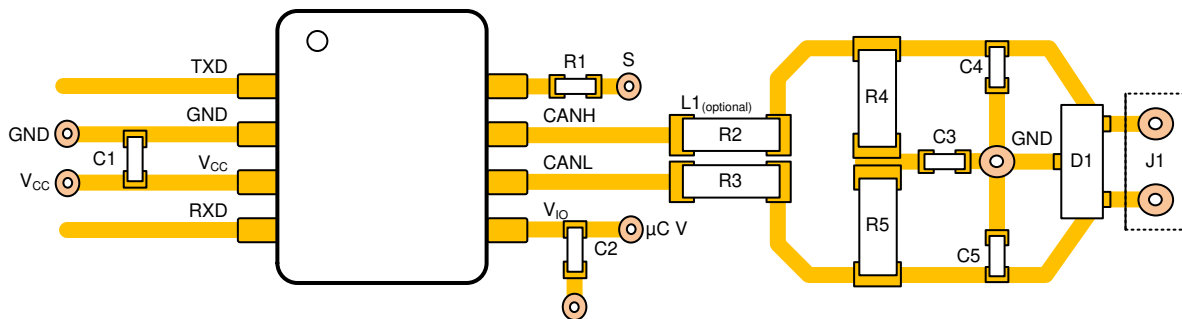


图 11-1. Layout Example

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 11.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

#### 11.4 Trademarks

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#### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1057ADDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2HEF	<a href="#">Samples</a>
TCAN1057ADRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1057A	<a href="#">Samples</a>
TCAN1057ADRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1057A	<a href="#">Samples</a>
TCAN1057AVDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2HFF	<a href="#">Samples</a>
TCAN1057AVDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1057AV	<a href="#">Samples</a>
TCAN1057AVDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1057AV	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1057ADDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN1057ADRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1057ADRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1057AVDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN1057AVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1057AVDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1057ADDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN1057ADRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1057ADRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TCAN1057AVDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN1057AVDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1057AVDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

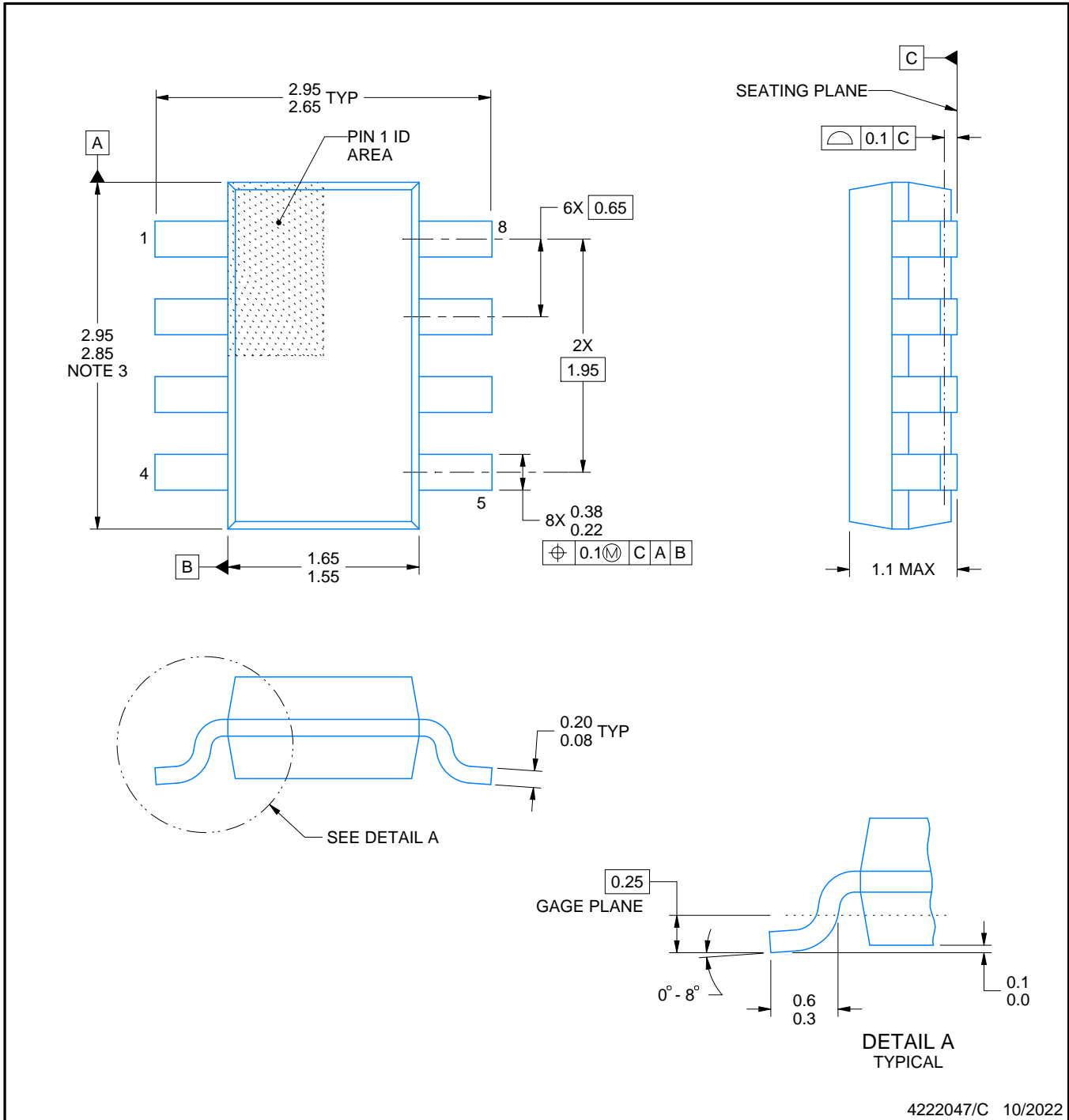
# DDF0008A



# PACKAGE OUTLINE

## SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/C 10/2022

**NOTES:**

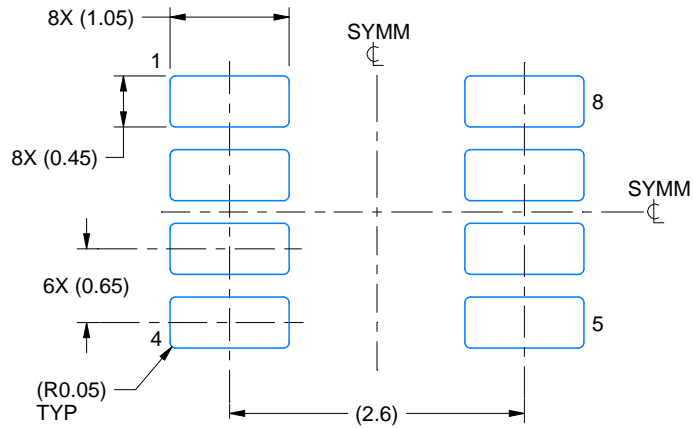
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

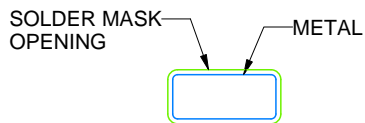
DDF0008A

SOT-23 - 1.1 mm max height

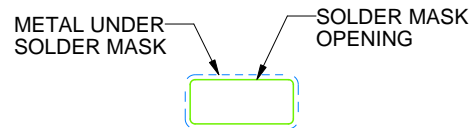
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

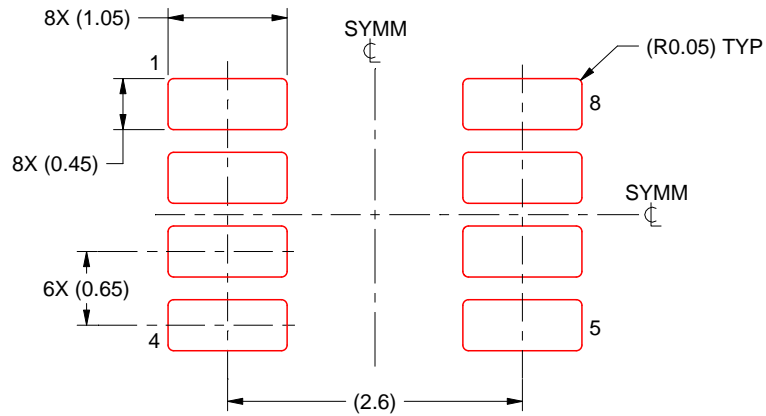
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

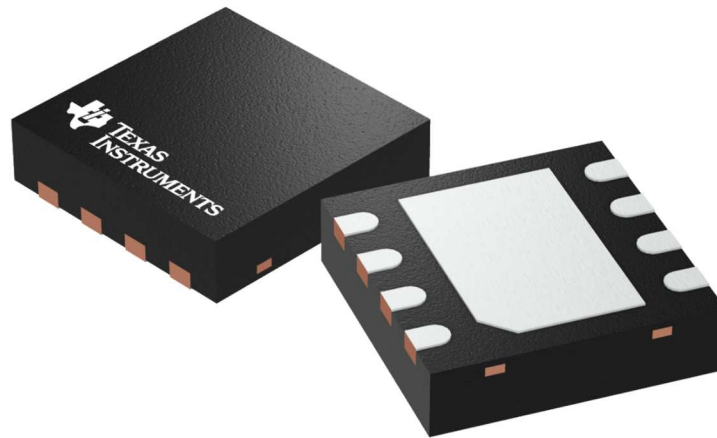


**DRB 8**

**GENERIC PACKAGE VIEW**

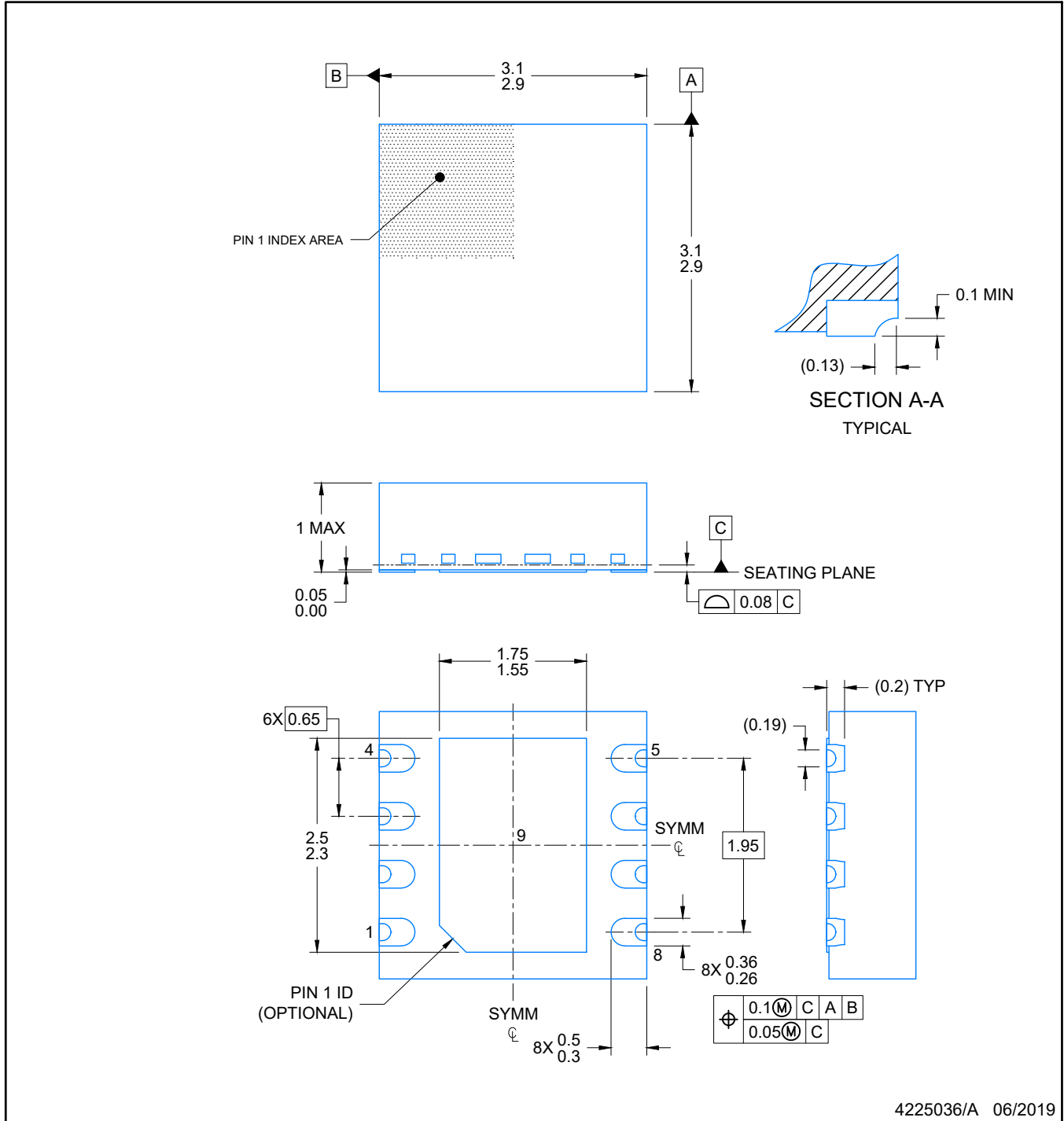
**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

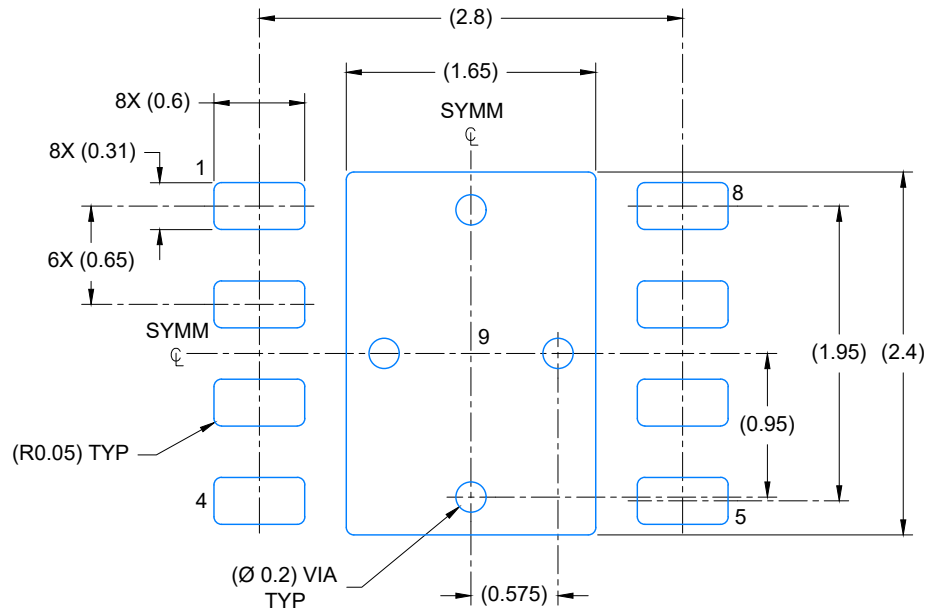
4203482/L



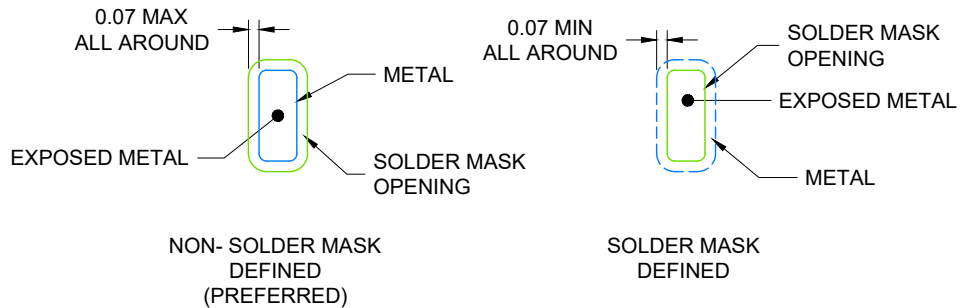
4225036/A 06/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

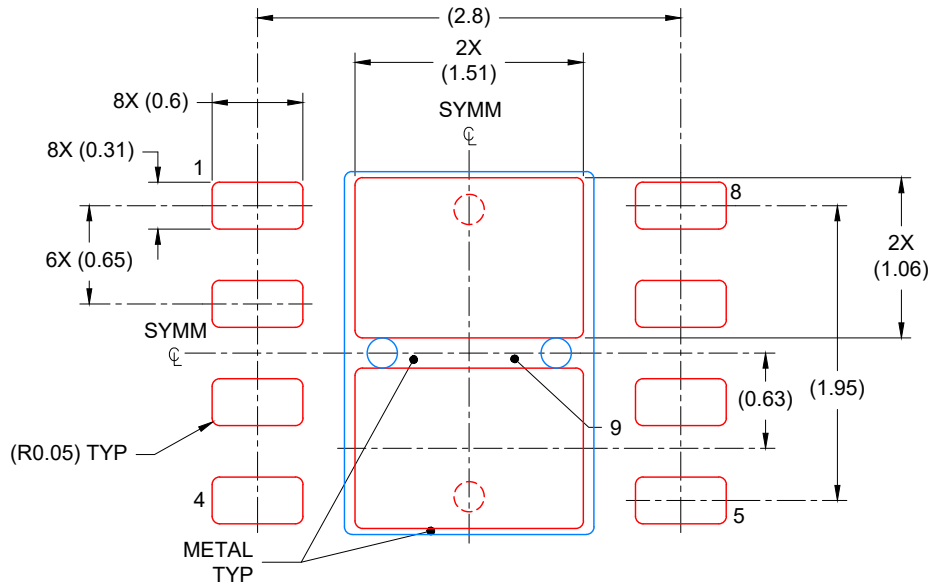


SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 81% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

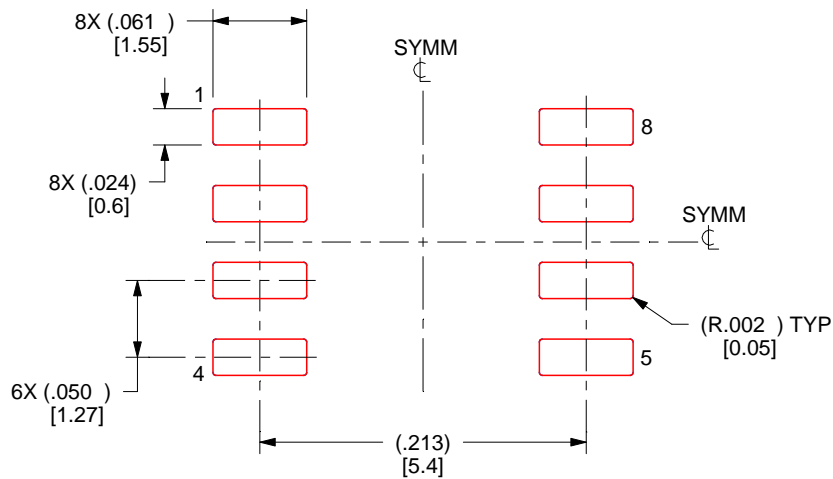
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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