TCAN340x-Q1 具有待机模式的 3.3V 汽车类 CAN FD 收发器

ADVANCE INFORMATION

1 特性

- 符合面向汽车应用的 AEC-Q100（1 级）标准
- 3.3 V 单电源工作
  - 无需使用 5V 稳压器，从而节省 BOM 成本并减小 PCB 空间
- 符合 ISO 11898-2:2016 物理层标准要求
- 支持传统 CAN 和经优化的 CAN FD 性能（数据速率为 2、5 和 8Mbps）
  - 具有较短的对称传播延迟时间，可增加时序裕量
- TCAN3403-Q1：I/O 电压范围支持：1.7V 至 3.6V
- 接收器共模输入电压：±12V
- 保护特性：
  - 欠压保护
  - TXD 显性超时 (DTO)
  - 热关断保护 (TSD)
- 工作模式：
  - 正常模式
  - 支持远程唤醒请求功能的低功耗待机模式
  - 超低功耗关断模式：仅限 TCAN3404-Q1
- 优化了未上电时的性能
  - 总线和逻辑引脚为高阻抗（运行总线或应用上无负载）
  - 支持热插拔：在总线和 RXD 输出上可实现上电和断电无干扰运行
- 具有可湿性侧面的小型 8 引脚 SOIC SOT-23 和无引线 VSON-8 封装，可实现自动光学检测 (AOI)

2 应用

- 汽车和运输
  - 车身控制模块
  - 汽车网关
  - 高级驾驶辅助系统 (ADAS)
  - 信息娱乐系统

3 说明

TCAN3403-Q1 和 TCAN3404-Q1 是满足 ISO 11898-2:2016 高速 CAN 规范中物理层要求的 3.3V 控制器局域网 (CAN) FD 收发器。

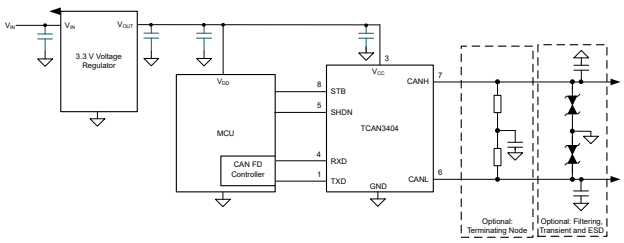
此类收发器具有经过认证的电磁兼容性 (EMC)，适用于数据速率高达 5 兆位/秒 (Mbps) 的传统 CAN 和 CAN FD 网络。这些器件可以在更简单的网络中实现高达 8Mbps 的运行速度。TCAN3403-Q1 包括通过 V_{IO} 引脚实现的内部逻辑电平转换功能，能够将收发器 I/O 直接连接到 1.8V、2.5V 或 3.3V 逻辑电平。TCAN3404-Q1 具有关断功能，可将所有块断电并使器件进入超低功耗模式。此类收发器支持低功耗待机模式，并且可通过符合 ISO 11898-2:2016 所定义唤醒模式 (WUP) 的 CAN 来唤醒。

此类收发器可进行热关断 (TSD)、TXD 显性超时 (DTO) 和电源欠压检测。这些器件定义了电源欠压或浮动引脚情况下的失效防护行为。这些器件采用业界通用的 SOIC-8、VSON-8 和节省空间的小尺寸 SOT-23 封装。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
TCAN3403-Q1 TCAN3404-Q1	SOIC (D)	4.90mm x 3.91mm
	VSON (DRB)	3.00mm x 3.00mm
	SOT-23 (DDF)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

Table of Contents

ADVANCE INFORMATION

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Device Comparison

Part Number	Pin 5	Pin 8
TCAN3404-Q1	Ultra-low power shutdown mode	Low Power Standby Mode with Remote Wake
TCAN3403-Q1	Low voltage I/O support	

6 Pin Configuration and Functions

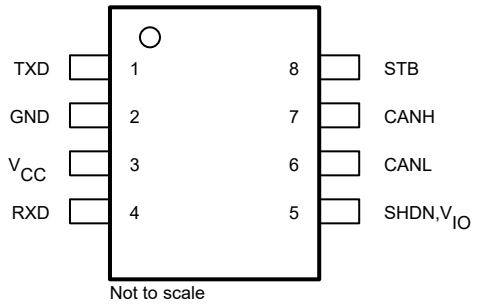


图 6-1. DDF Package, 8-Pin SOT-23 (Top View)

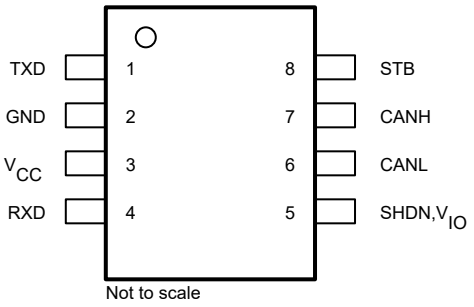


图 6-2. D Package, 8-Pin SOIC (Top View)

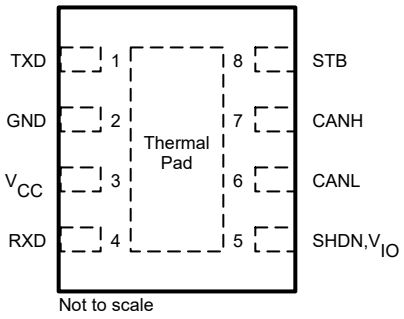


图 6-3. DRB Package, 8-Pin VSON (Top View)

表 6-1. Pin Functions

PINS		TYPE(1)	DESCRIPTION
NAME	NO.		
TXD	1	Digital Input	CAN transmit data input; integrated pull-up
GND	2	G	Ground connection
V_{CC}	3	Supply	3.3 V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-stated when device powered off
SHDN	5	Digital Input	Device in ultra-low power shutdown mode if pin is high; integrated pull-down (TCAN3404-Q1 only)
V_{IO}		Supply	I/O supply voltage (TCAN3403-Q1 only)
CANL	6	Bus I/O	Low-level CAN bus input/output line
CANH	7	Bus I/O	High-level CAN bus input/output line
STB	8	Digital Input	Standby input for mode control; integrated pull-up
Thermal Pad (VSON only)		—	Connect the thermal pad to any internal PCB ground plane using multiple vias for optimal thermal performance.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground.

ADVANCE INFORMATION

7 Device and Documentation Support

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

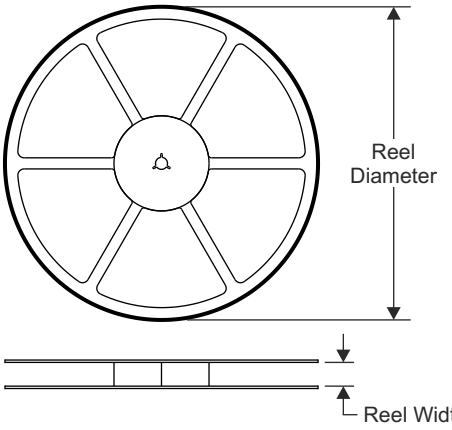
8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

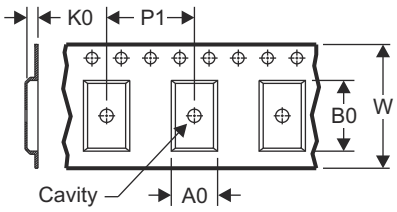
ADVANCE INFORMATION

8.1 Tape and Reel Information

REEL DIMENSIONS

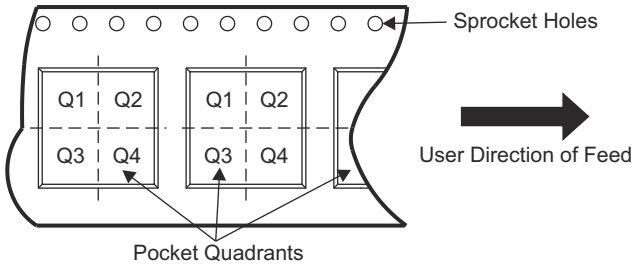


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

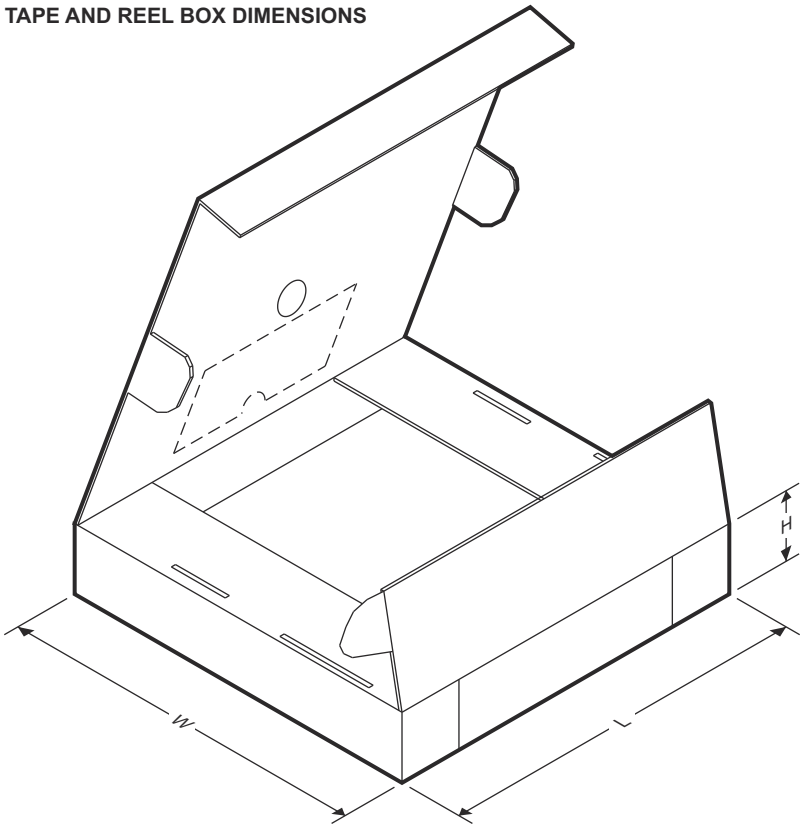


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTCAN3403DDFRQ1	SOT-23-THN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PTCAN3403DRBRQ1	VSON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
PTCAN3403DRBRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



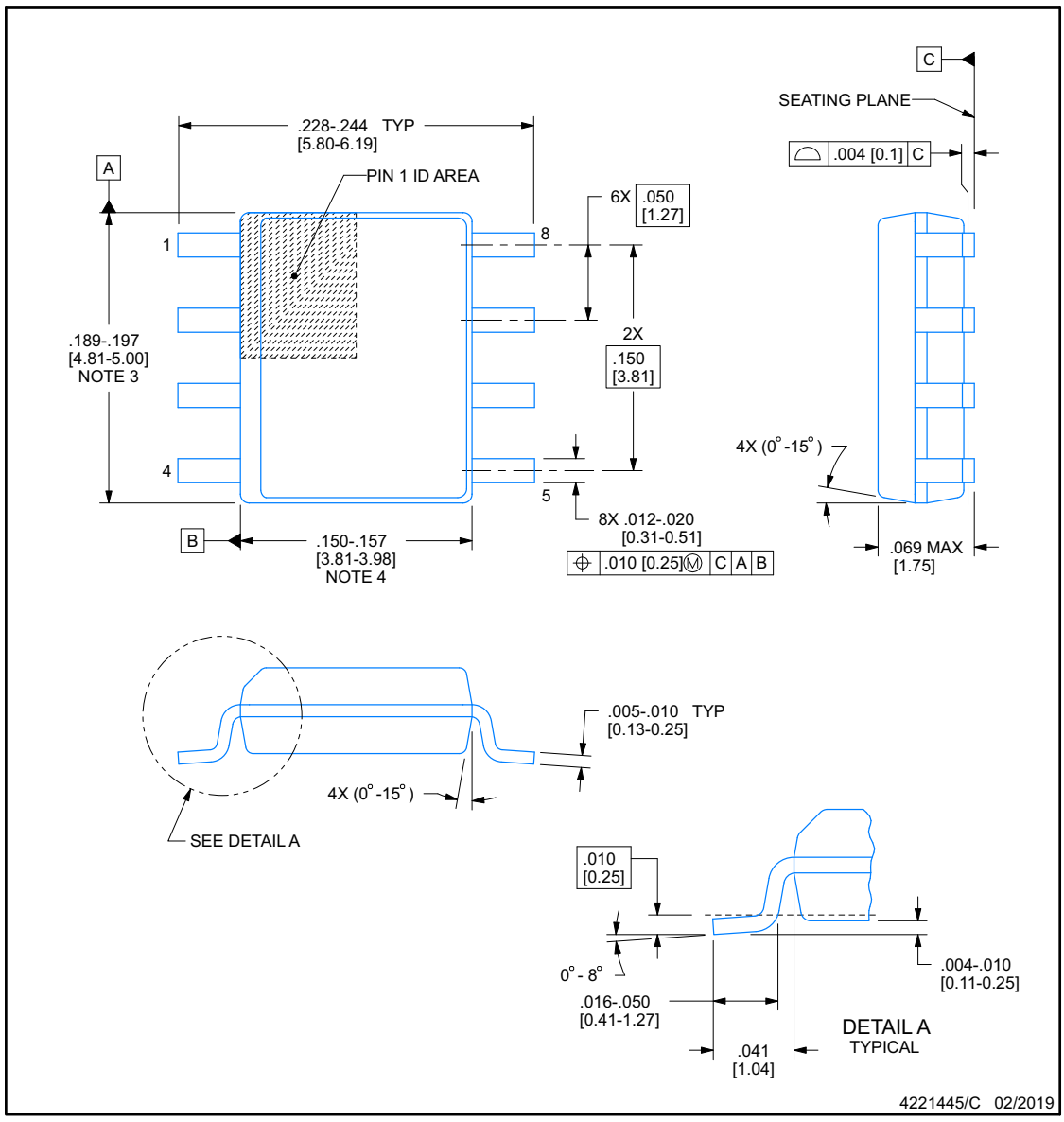
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTCAN3403DDFRQ1	SOT-23-THN	DDF	8	3000	210.0	185.0	35.0
PTCAN3403DRBRQ1	VSON	DRB	8	3000	367.0	367.0	35.0
PTCAN3403DRBRQ1	SOIC	D	8	2500	356.0	356.0	35.0

8.2 Mechanical Data

PACKAGE OUTLINE

D0008B — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

ADVANCE INFORMATION

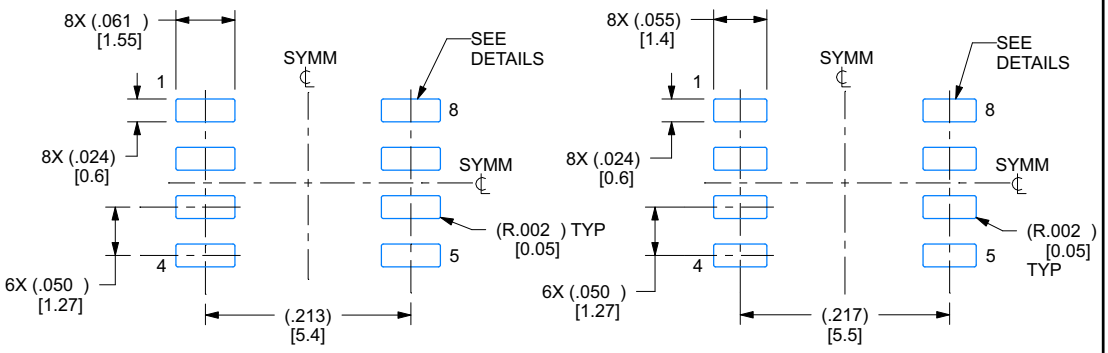
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

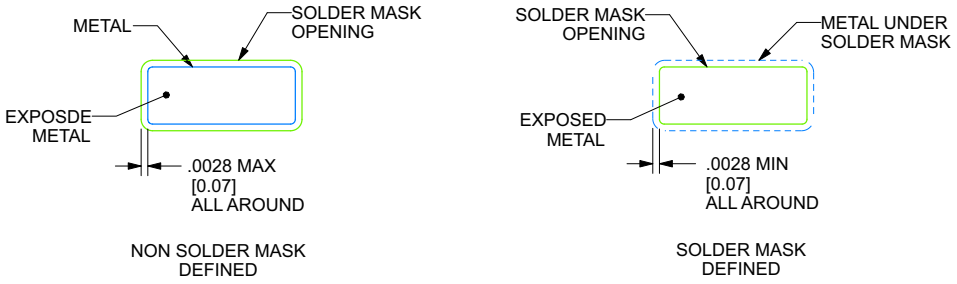
SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

NOTES: (continued)

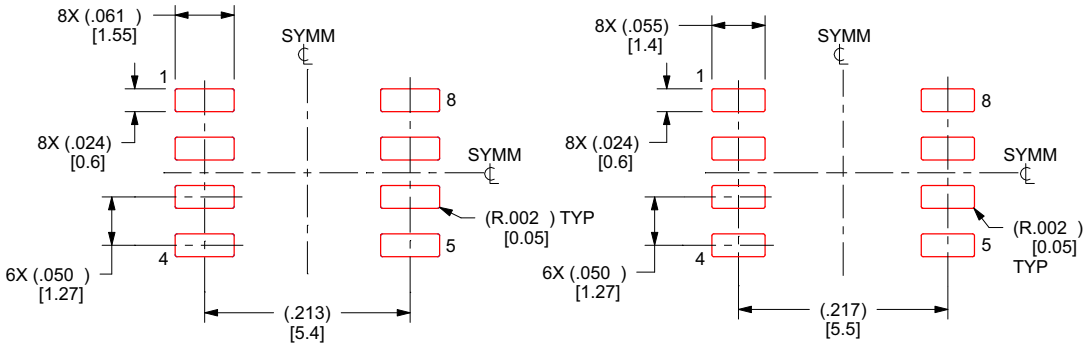
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

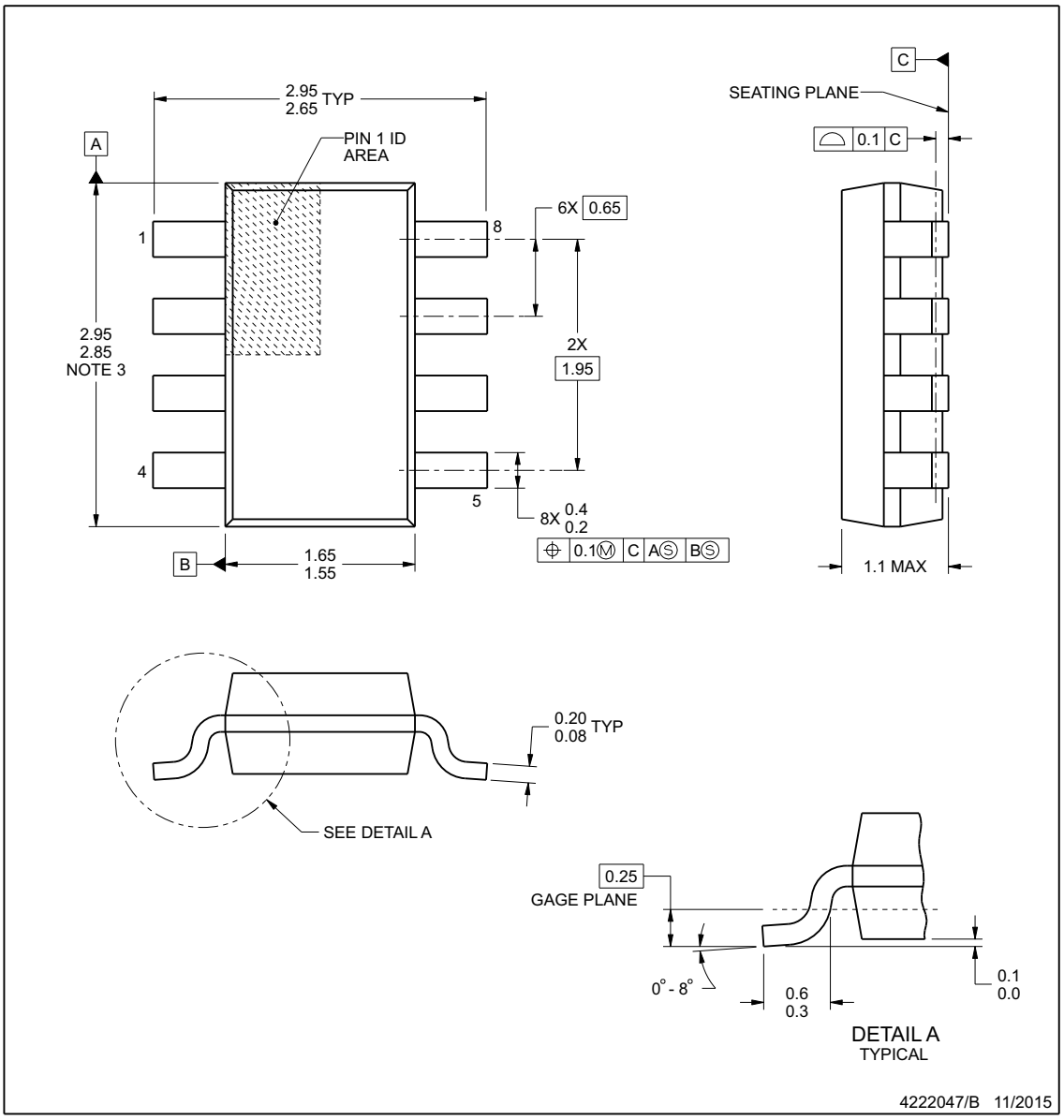
ADVANCE INFORMATION

PACKAGE OUTLINE

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

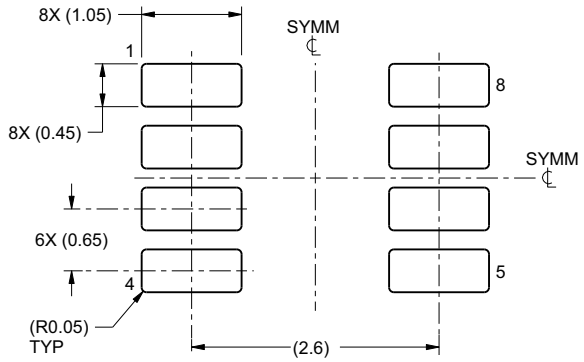
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

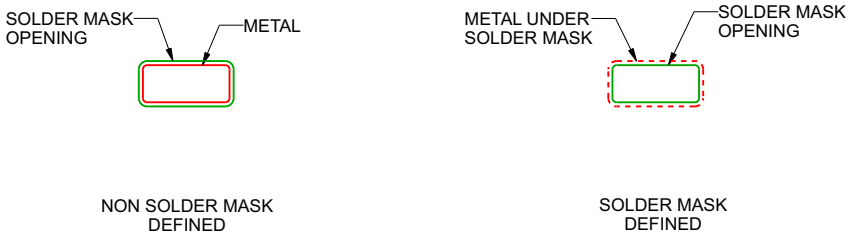
DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

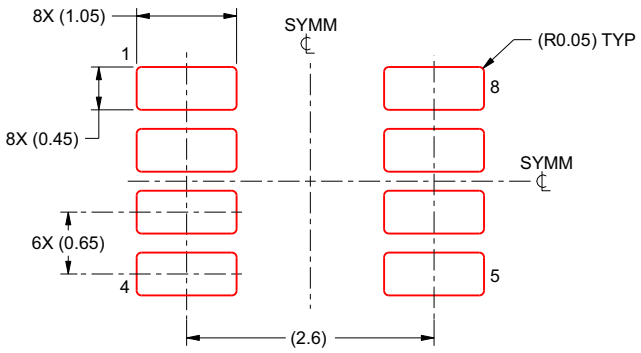
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DDF0008A — **SOT-23 - 1.1 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

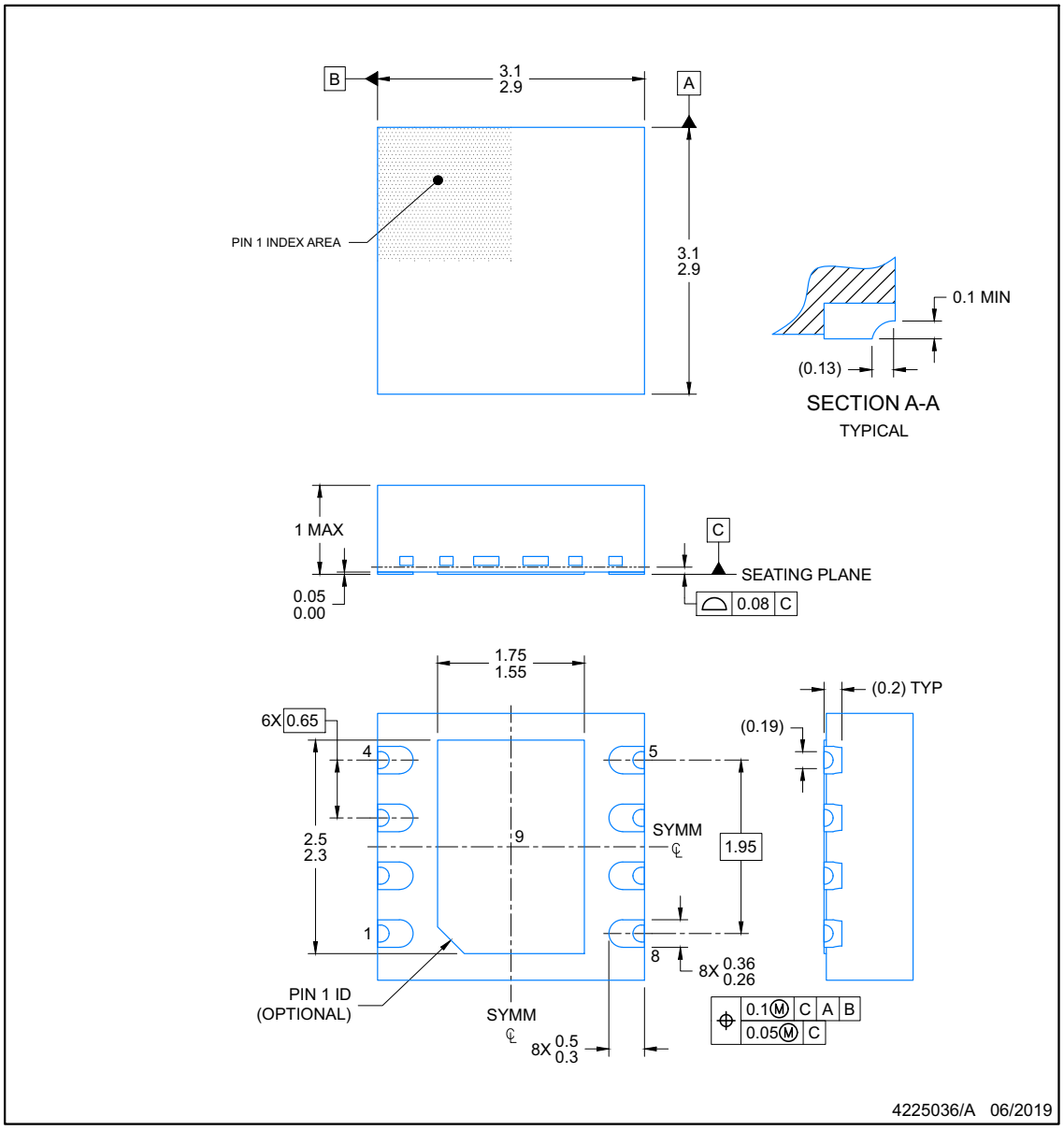
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRB0008J

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

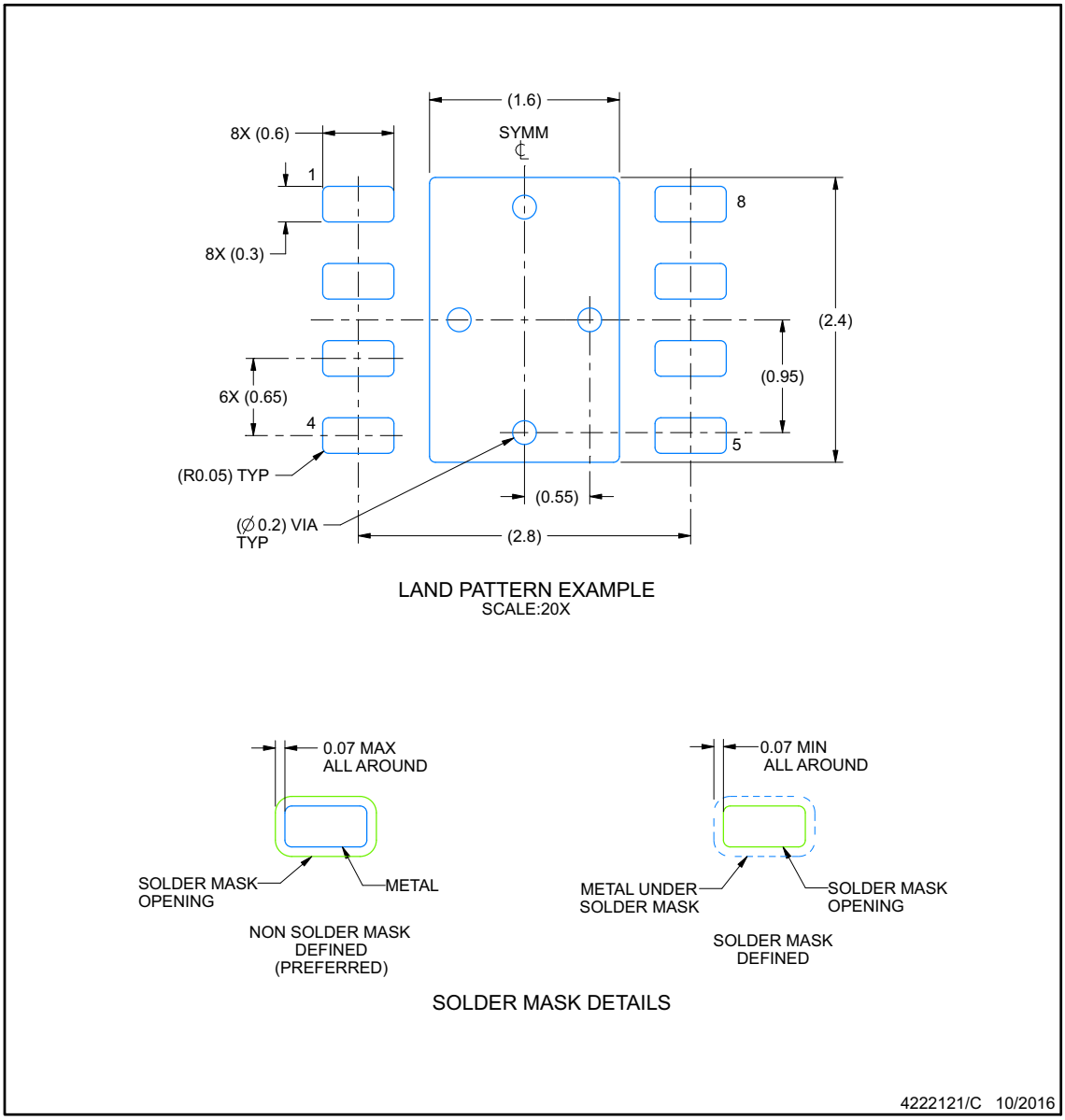
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DRB0008F — VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

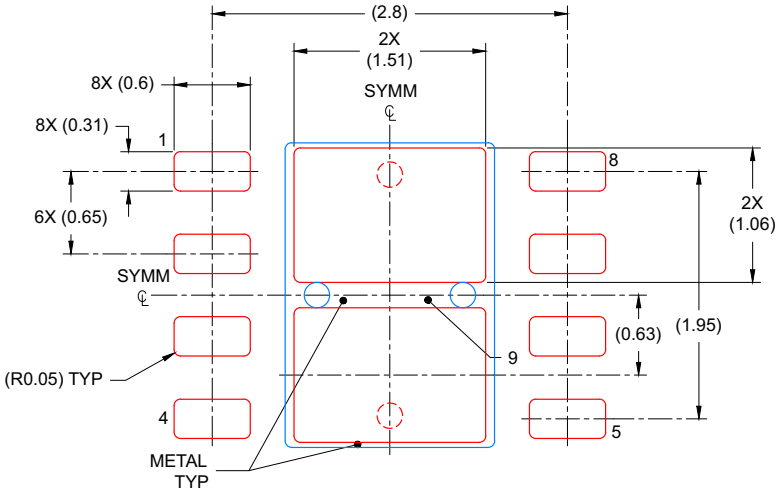
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008J

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTCAN3403DRBRQ1	ACTIVE	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 150		Samples
PTCAN3403DRQ1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 150		Samples
PTCAN3404DRBRQ1	ACTIVE	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 150		Samples
PTCAN3404DRQ1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

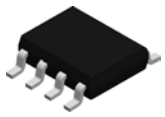
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

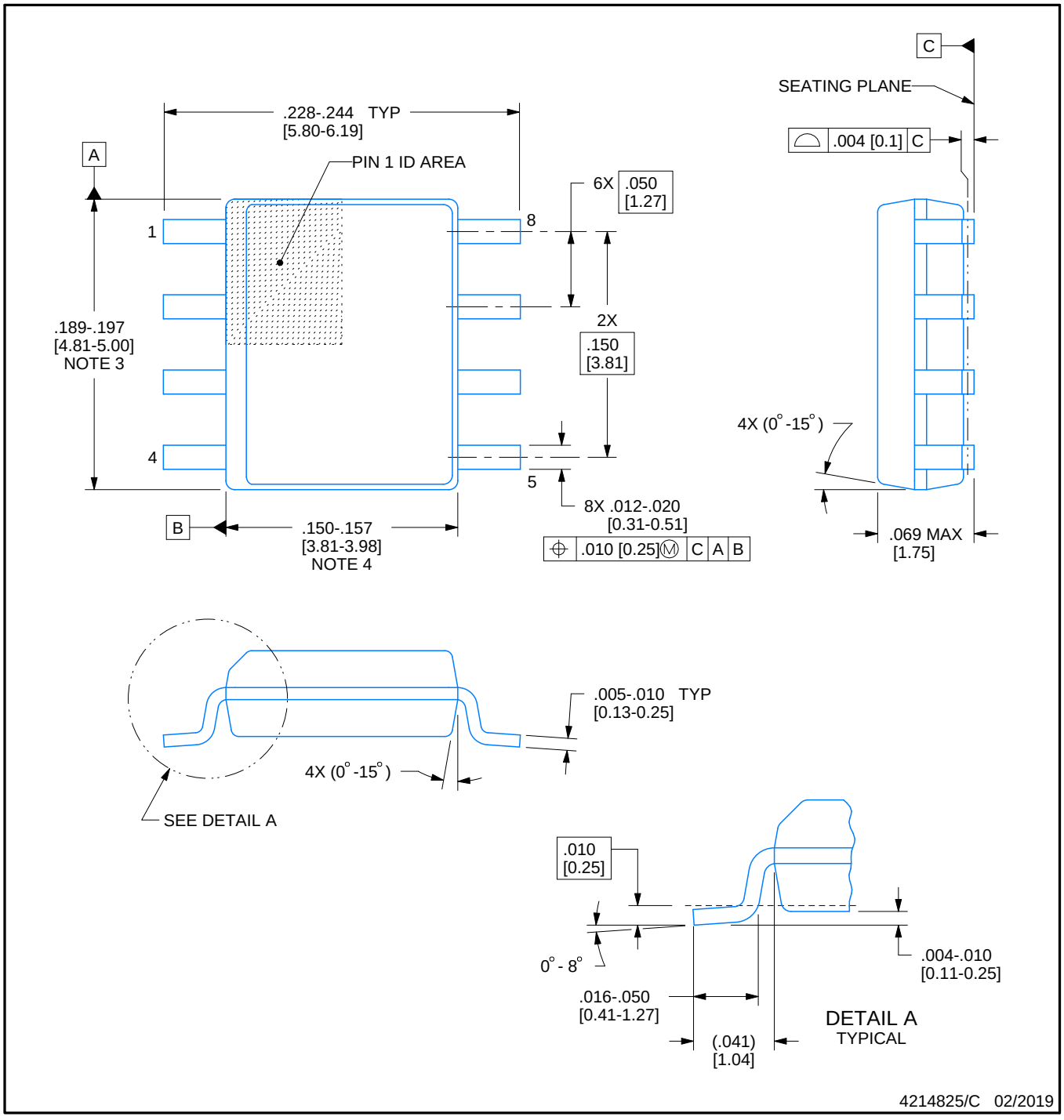


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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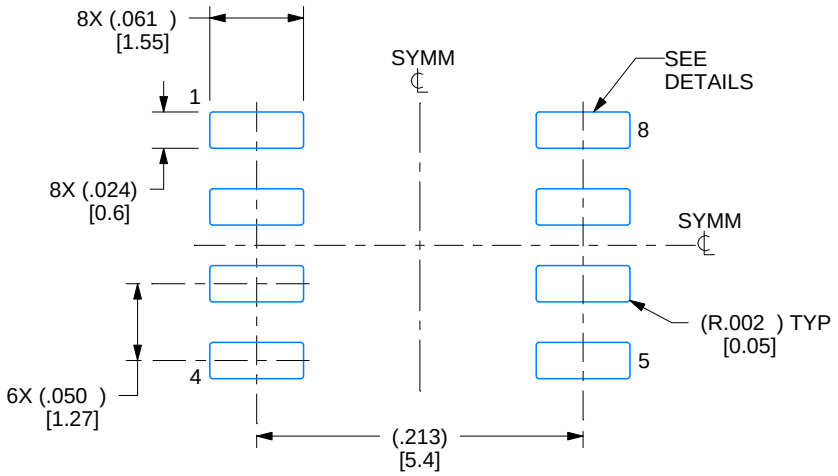
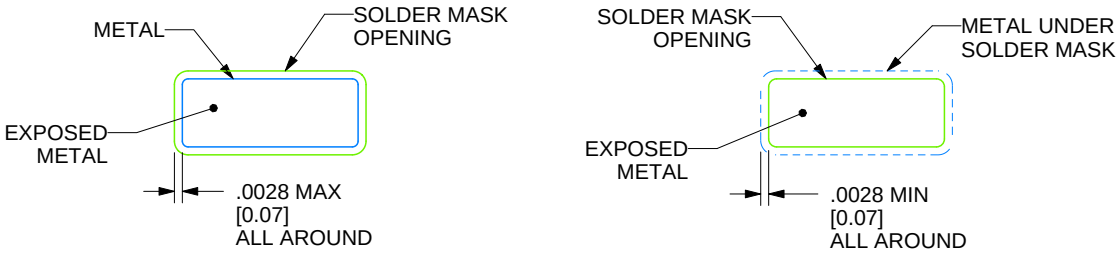
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

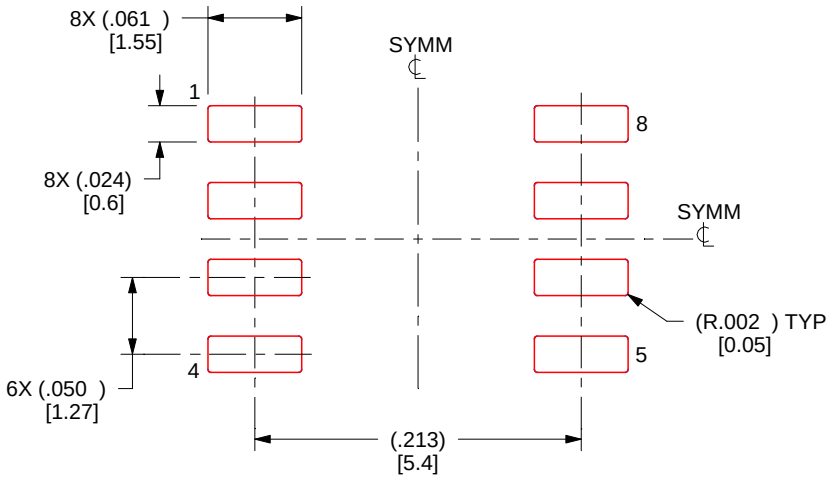
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

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