

## TL331B-Q1、TL391B-Q1 和 TL331-Q1 汽车单比较器

### 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 125°C 环境温度范围 (B 和 Q 版本)
  - 器件温度等级 3：-40°C 至 85°C 环境温度范围 (I 版本)
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C5
- 全新 [TL331B-Q1](#) 和 [TL391B-Q1](#)
- 宽电源电压范围，2V 至 36V
- 不受电源电压影响的低漏极电源电流：0.43mA 典型值 (B 版本)
- 低输入偏置电流，3.5nA 典型值 (B 版本)
- 低输入失调电压，0.37mV 典型值 (B 版本)
- 差分输入电压范围等于最大额定电源电压，±36V
- 输入范围包括接地电压
- [TL391B-Q1](#) 提供了 [替代引脚排列](#)
- 输出与 TTL、MOS 和 CMOS 兼容

### 2 应用

- [汽车](#)
- [HEV/EV 和动力总成](#)
- [信息娱乐系统与仪表组](#)
- [车身控制模块](#)

### 3 说明

[TL331B-Q1](#) 和 [TL391B-Q1](#) 器件是业界通用 [TL331-Q1](#) 比较器的下一代版本。下一代器件为成本敏感型应用提供了卓越的价值，其特性包括更低的失调电压、更高的电源电压能力、更低的电源电流、更低的输入偏置电流、更低的传播延迟、具有改进的负输入电压处理能力的专用 ESD 保护单元。[TL331B-Q1](#) 可直接替换 [TL331-Q1](#) “I” 和 “Q” 版本。[TL391B-Q1](#) 提供了 [TL331B-Q1](#) 的 [替代引脚排列](#)。

这个器件包含一个单电压比较器，此比较器被设计成在宽范围电压上由一个单电源供电运行。如果两个电源之间的电压差在 2V 和 36V 之间且  $V_{CC}$  比输入共模电压至少高 +1.5V，也可使用双电源供电运行。漏极电流不受电源电压的影响。为了实现线与关系，用户可将输出连接至另外一个集电极开路输出。

#### 器件信息

| 器件型号                                 | 封装 <sup>(1)</sup> | 封装尺寸 (标称值)      |
|--------------------------------------|-------------------|-----------------|
| TL331B-Q1、<br>TL391B-Q1、<br>TL331-Q1 | SOT-23 (5)        | 2.90mm × 1.60mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



## Family Comparison Table

| Specification                        | TL331B-Q1<br>TL391B-Q1 | TL331I-Q1 | TL331Q-Q1  | Units |
|--------------------------------------|------------------------|-----------|------------|-------|
| Supply Voltage                       | 2 to 36                | 2 to 36   | 2 to 36    | V     |
| Total Supply Current (5V to 36V max) | 0.43                   | 0.7       | 0.7        | mA    |
| Temperature Range                    | -40 to 125             | -40 to 85 | -40 to 125 | °C    |
| ESD (HBM)                            | 2000                   | 2000      | 2000       | V     |
| Offset Voltage (Max over temp)       | ± 4                    | ± 9       | ± 9        | mV    |
| Input Bias Current (typ / max)       | 3.5 / 25               | 25 / 250  | 25 / 250   | nA    |
| Response Time (typ)                  | 1                      | 1.3       | 1.3        | µsec  |

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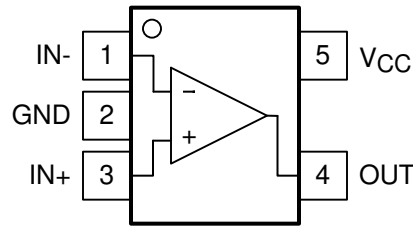
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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

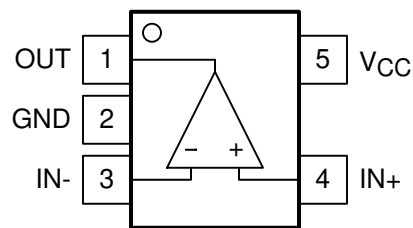
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| • 更正了首页链接文本以添加缺少的“B”.....  | 1           |
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| • 更新了整个文档中的表格、图和交叉参考的编号格式.....   | 1           |
| • 在整个数据表中将 TL331B-Q1 和 TL391B-Q1 建议的最小电源电压更改为 2V.....                              | 1           |
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| <b>Changes from Revision C (October 2013) to Revision D (June 2020)</b> .....      | <b>Page</b> |
| • 添加了 B 器件。更新为当前 TI 数据表格式。修改了首页文本以突出显示 B 版本。.....                                  | 1           |
| • Added Family Comparison Table.....   | 2           |
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| • Changed $V_{ICR}$ in the Electrical Characteristics.....                         | 8           |
| • Changed test conditions of $I_{OL}$ in the Electrical Characteristics.....       | 8           |
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| • Changed $V_{ICR}$ in the Electrical Characteristics.....                         | 8           |

## 5 Pin Configuration and Functions



Note reversed inputs compared to similar popular pinout

**图 5-1. TL331-Q1, TL331B-Q1 DBV Package  
5-Pin SOT-23  
Top View**



Note reversed inputs compared to similar popular pinout

**图 5-2. TL391B-Q1 DBV Package  
5-Pin SOT-23  
Top View**

**表 5-1. Pin Functions**

| NAME            | PIN                           |                  | TYPE | DESCRIPTION                 |
|-----------------|-------------------------------|------------------|------|-----------------------------|
|                 | TL331-Q1,<br>TL331B-Q1<br>NO. | TL391B-Q1<br>NO. |      |                             |
| IN+             | 3                             | 4                | I    | Positive Input              |
| IN -            | 1                             | 3                | I    | Negative Input              |
| OUT             | 4                             | 1                | O    | Open Collector/Drain Output |
| V <sub>CC</sub> | 5                             | 5                | —    | Power Supply Input          |
| GND             | 2                             | 2                | —    | Ground                      |

## 6 Specifications

### 6.1 Absolute Maximum Ratings, TL331-Q1

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|   | MIN       | MAX | UNIT |
|---|-----------|-----|------|
| V <sub>CC</sub> Supply voltage <sup>(2)</sup>             | 0         | 36  | V    |
| V <sub>ID</sub> Differential input voltage <sup>(3)</sup> | - 36      | 36  | V    |
| V <sub>I</sub> Input voltage range (either input)         | - 0.3     | 36  | V    |
| V <sub>O</sub> Output voltage                             | 0         | 36  | V    |
| I <sub>O</sub> Output current                             | 0         | 20  | mA   |
| Duration of output short-circuit to ground <sup>(4)</sup> | Unlimited |     |      |
| T <sub>J</sub> Operating virtual junction temperature     | 150       |     | °C   |
| T <sub>stg</sub> Storage temperature                      | - 65      | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN - .
- (4) Short circuits from outputs to V<sub>CC</sub> can cause excessive heating and eventual destruction.

### 6.2 Absolute Maximum Ratings, TL331B-Q1 and TL391B-Q1

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|   | MIN       | MAX  | UNIT |
|---|-----------|------|------|
| V <sub>CC</sub> Supply voltage <sup>(2)</sup>             | -0.3      | 38   | V    |
| V <sub>ID</sub> Differential input voltage <sup>(3)</sup> | - 38      | 38   | V    |
| V <sub>I</sub> Input voltage range (either input)         | - 0.3     | 38   | V    |
| V <sub>O</sub> Output voltage                             | -0.3      | 38   | V    |
| I <sub>O</sub> Output current                             |           | 20   | mA   |
| Duration of output short-circuit to ground <sup>(4)</sup> | Unlimited |      |      |
| I <sub>IK</sub> Input current <sup>(5)</sup>              |           | - 50 | mA   |
| T <sub>J</sub> Operating virtual junction temperature     | - 40      | 150  | °C   |
| T <sub>stg</sub> Storage temperature                      | - 65      | 150  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN - .
- (4) Short circuits from outputs to V<sub>CC</sub> can cause excessive heating and eventual destruction.
- (5) Input current flows thorough parasitic diode to ground and will turn on parasitic transistors that will increase ICC and may cause output to be incorrect. Normal operation resumes when input current is removed.

### 6.3 ESD Ratings, All Devices

|  | VALUE   | UNIT  |
|--|---|-------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2000 |
|  | Charged-device model (CDM), per AEC Q100-0111           | ±750  |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.4 Recommended Operating Conditions, TL331-Q1

over operating free-air temperature range (unless otherwise noted)

|                 |                                    | MIN  | MAX | UNIT |
|-----------------|------------------------------------|------|-----|------|
| V <sub>CC</sub> | Supply voltage                     | 2    | 36  | V    |
| T <sub>J</sub>  | Junction temperature, TL331IDBVRQ1 | - 40 | 85  | °C   |
| T <sub>J</sub>  | Junction temperature, TL331QDBVRQ1 | - 40 | 125 | °C   |

## 6.5 Recommended Operating Conditions, TL331B-Q1 and TL391B-Q1

over operating free-air temperature range (unless otherwise noted)

|                 |                      | MIN  | MAX | UNIT |
|-----------------|----------------------|------|-----|------|
| V <sub>CC</sub> | Supply voltage       | 2    | 36  | V    |
| T <sub>J</sub>  | Junction temperature | - 40 | 125 | °C   |

## 6.6 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | TL331-Q1                                     | TL331B-Q1,<br>TL391B-Q1 | UNIT  |      |
|-------------------------------|--|-------------------------|-------|------|
|                               | DBV (SOT-23)                                 | DBV (SOT-23)            |       |      |
|                               | 5 PINS                                       | 5 PINS                  |       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 218.3                   | 211.7 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 87.3                    | 133.6 | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 44.9                    | 79.9  | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 4.3                     | 56.4  | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 44.1                    | 79.6  | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.7 Electrical Characteristics, TL331B-Q1 and TL391B-Q1

$V_S = 5\text{ V}$ ,  $V_{CM} = (V_-)$ ;  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

| PARAMETER    |   | TEST CONDITIONS   | MIN   | TYP        | MAX  | UNIT          |
|--------------|---|---|-------|------------|------|---------------|
| $V_{IO}$     | Input offset voltage                            | $V_S = 5$ to 36V  | - 2.5 | $\pm 0.37$ | 2.5  | mV            |
|              |   | $V_S = 5$ to 36V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                     | - 4   |            | 4    |               |
| $I_B$        | Input bias current                              |   |       | - 3.5      | - 25 | nA            |
|              |   | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$   |       |            | - 50 | nA            |
| $I_{OS}$     | Input offset current                            |   | - 10  | $\pm 0.5$  | 10   | nA            |
|              |   | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$   | - 25  |            | 25   | nA            |
| VCM          | Common mode range                               | $V_S = 3$ to 36V  | (V -) | (V+) - 1.5 |      | V             |
|              |   | $V_S = 3$ to 36V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                                     | (V -) | (V+) - 2.0 |      | V             |
| $A_{VD}$     | Large signal differential voltage amplification | $V_S = 15\text{V}$ , $V_O = 1.4\text{V}$ to $11.4\text{V}$ ;<br>$R_L \geq 15\text{k}$ to (V+)           | 50    | 200        |      | V/mV          |
| $V_{OL}$     | Low level output Voltage<br>{swing from (V -)}  | $I_{SINK} \leq 4\text{mA}$ , $V_{ID} = -1\text{V}$  |       | 110        | 400  | mV            |
|              |   | $I_{SINK} \leq 4\text{mA}$ , $V_{ID} = -1\text{V}$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ |       |            | 550  | mV            |
| $I_{OH-LKG}$ | High-level output leakage current               | (V+) = $V_O = 5\text{V}$ ; $V_{ID} = 1\text{V}$   |       | 0.1        | 20   | nA            |
| $I_{OH-LKG}$ | High-level output leakage current               | (V+) = $V_O = 36\text{V}$ ; $V_{ID} = 1\text{V}$ ; $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$    |       |            | 1000 | nA            |
| $I_{OL}$     | Low level output current                        | $V_{OL} = 1.5\text{V}$ ; $V_{ID} = -1\text{V}$ ; $V_S = 5\text{V}$                                      | 6     | 18         |      | mA            |
| $I_Q$        | Quiescent current                               | $V_S = 5\text{V}$ , no load   |       | 210        | 330  | $\mu\text{A}$ |
|              |   | $V_S = 36\text{V}$ , no load, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                         |       | 275        | 430  | $\mu\text{A}$ |

## 6.8 Switching Characteristics, TL331B-Q1 and TL391B-Q1

$V_S = 5\text{V}$ ,  $V_O$  PULLUP = 5V,  $V_{CM} = V_S/2$ ,  $C_L = 15\text{pF}$ ,  $R_L = 5.1\text{k}\Omega$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

| PARAMETER             |   | TEST CONDITIONS                               | MIN | TYP  | MAX | UNIT |
|-----------------------|---|---|-----|------|-----|------|
| $t_{\text{response}}$ | Propagation delay time, high-to-low; Small scale input signal (1) | Input overdrive = 5mV, Input step = 100mV     |     | 1000 |     | ns   |
| $t_{\text{response}}$ | Propagation delay time, high-to-low; TTL input signal (1)         | TTL input with $V_{\text{ref}} = 1.4\text{V}$ |     | 300  |     | ns   |

(1) High-to-low and low-to-high refers to the transition at the input.

## 6.9 Electrical Characteristics, TL331-Q1

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS <sup>(1)</sup>  | T <sub>A</sub> | MIN                        | TYP | MAX  | UNIT |
|---|---|----------------|----------------------------|-----|------|------|
| V <sub>IO</sub> Input offset voltage                            | V <sub>CC</sub> = 5 V to 30 V, V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = V <sub>IC(min)</sub>       | 25°C           |                            | 2   | 5    | mV   |
|   |   | -40°C to 125°C |                            |     | 9    |      |
| I <sub>IO</sub> Input offset current                            | V <sub>O</sub> = 1.4 V  | 25°C           |                            | 5   | 50   | nA   |
|   |   | -40°C to 125°C |                            |     | 250  |      |
| I <sub>IB</sub> Input bias current                              | V <sub>O</sub> = 1.4 V  | 25°C           |                            | -25 | -250 | nA   |
|   |   | -40°C to 125°C |                            |     | -400 |      |
| V <sub>ICR</sub> Common-mode input voltage range <sup>(2)</sup> |   | 25°C           | 0 to V <sub>CC</sub> - 1.5 |     |      | V    |
|   |   | -40°C to 125°C | 0 to V <sub>CC</sub> - 2   |     |      |      |
| A <sub>VD</sub> Large-signal differential-voltage amplification | V <sub>CC</sub> = 15 V, V <sub>O</sub> = 1.4 V to 11.4 V, R <sub>L</sub> ≥ 15 kΩ to V <sub>CC</sub> | 25°C           | 50                         | 200 |      | V/mV |
| I <sub>OH</sub> High-level output current                       | V <sub>OH</sub> = 5 V, V <sub>ID</sub> = 1 V  | 25°C           |                            | 0.1 | 50   | nA   |
|   | V <sub>OH</sub> = 30 V, V <sub>ID</sub> = 1 V   | -40°C to 125°C |                            |     | 1    | μA   |
| V <sub>OL</sub> Low-level output voltage                        | I <sub>OL</sub> = 4 mA, V <sub>ID</sub> = -1 V  | 25°C           |                            | 150 | 400  | mV   |
|   |   | -40°C to 125°C |                            |     | 700  |      |
| I <sub>OL</sub> Low-level output current                        | V <sub>OL</sub> = 1.5 V, V <sub>ID</sub> = -1 V   | 25°C           | 6                          |     |      | mA   |
| I <sub>CC</sub> Supply current                                  | R <sub>L</sub> = ∞, V <sub>CC</sub> = 5 V   | 25°C           |                            | 0.4 | 0.7  | mA   |

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

(2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V<sub>CC+</sub> - 1.5 V at 25°C, but either or both inputs can go to 30 V without damage.

## 6.10 Switching Characteristics, TL331-Q1

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER     | TEST CONDITIONS   | TYP                                   | UNIT |    |
|---------------|---|---------------------------------------|------|----|
| Response time | R <sub>L</sub> connected to 5 V through 5.1 kΩ, C <sub>L</sub> = 15 pF <sup>(1) (2)</sup> | 100-mV input step with 5-mV overdrive | 1.3  | μs |
|               |   | TTL-level input step                  | 0.3  |    |

(1) C<sub>L</sub> includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.



### 6.11 Typical Characteristics, TL331-Q1

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_{\text{PULLUP}} = 5.1\text{k}$ ,  $C_L = 15\text{pF}$ ,  $V_{\text{CM}} = 0\text{V}$  unless otherwise noted.

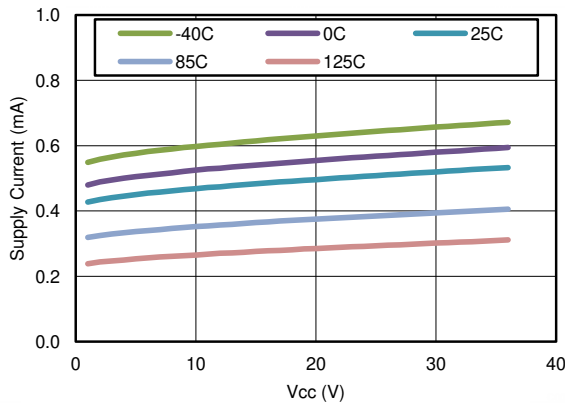


图 6-1. Supply Current vs Supply Voltage

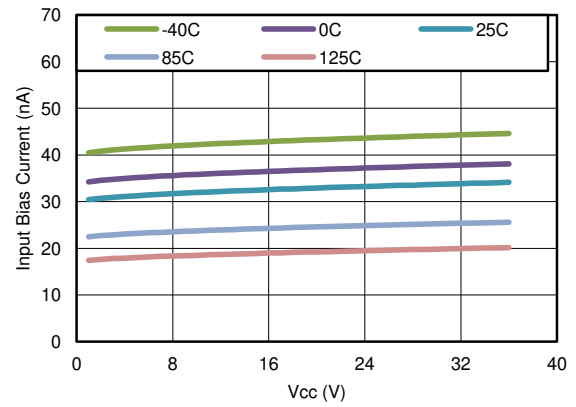


图 6-2. Input Bias Current vs Supply Voltage

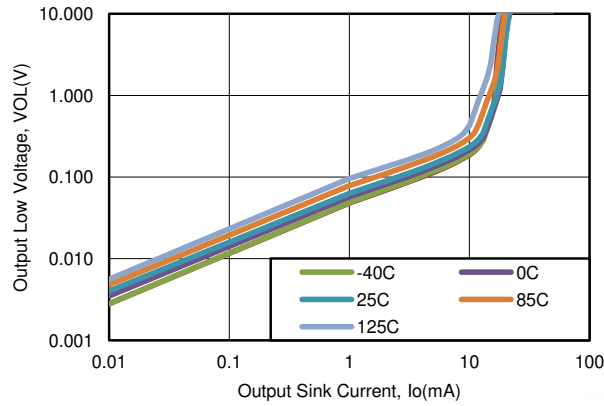


图 6-3. Output Low Voltage vs Output Current ( $I_{OL}$ )

## 6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 5.1\text{ k}$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

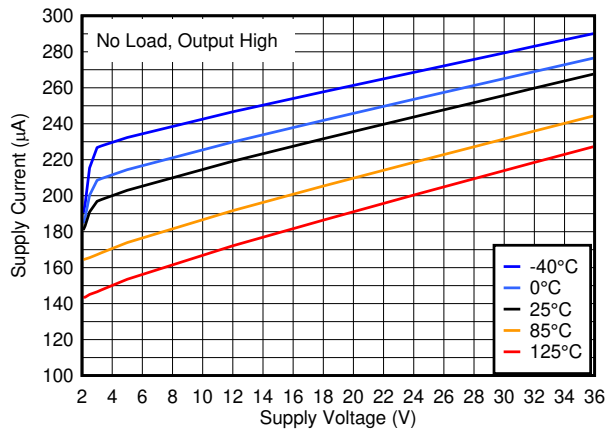


图 6-4. Supply Current vs. Supply Voltage

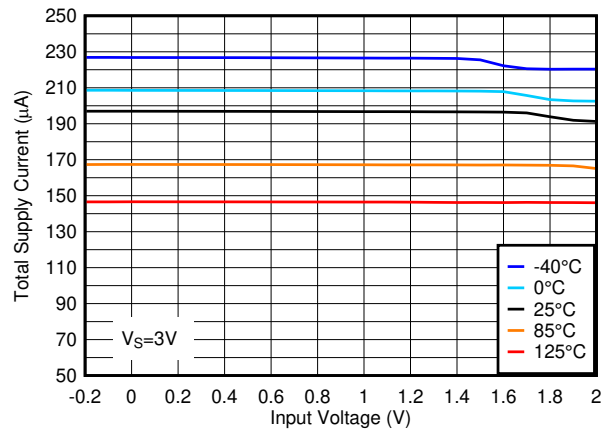


图 6-5. Total Supply Current vs. Input Voltage at 3V

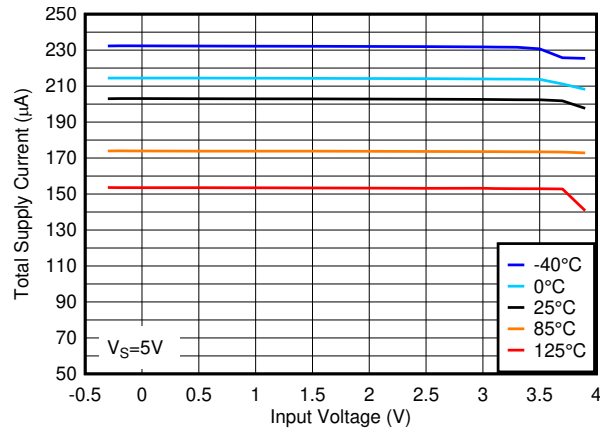


图 6-6. Total Supply Current vs. Input Voltage at 3.3V

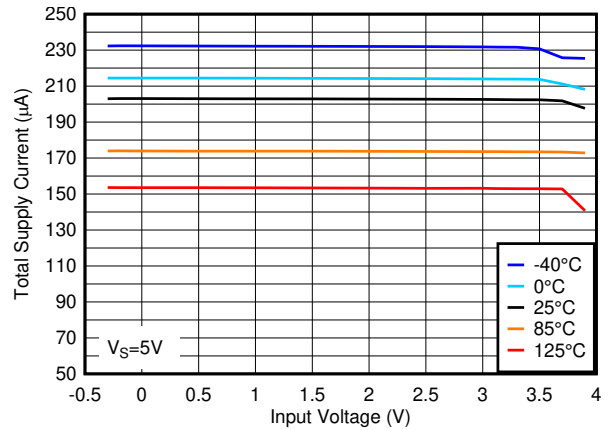


图 6-7. Total Supply Current vs. Input Voltage at 5V

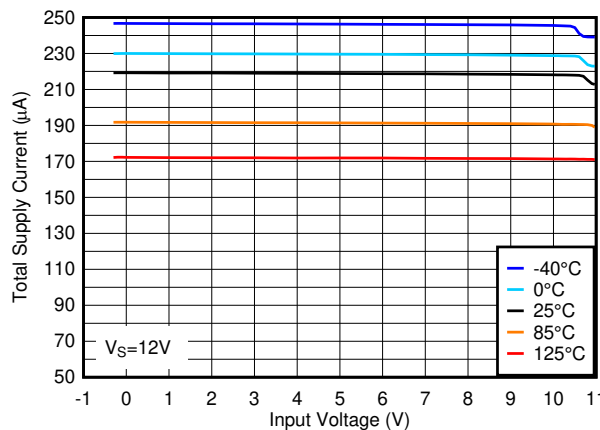


图 6-8. Total Supply Current vs. Input Voltage at 12V

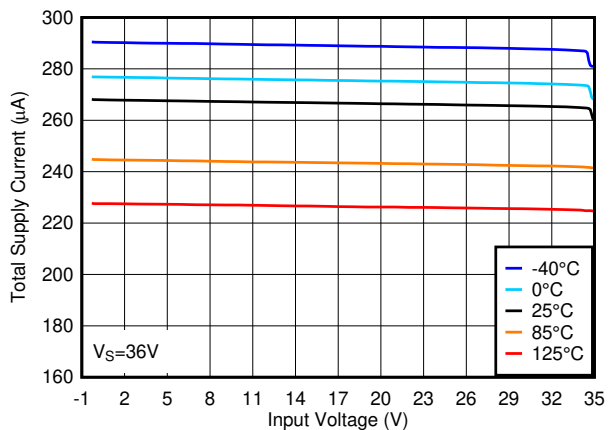


图 6-9. Total Supply Current vs. Input Voltage at 36V

### 6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 5.1\text{ k}$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

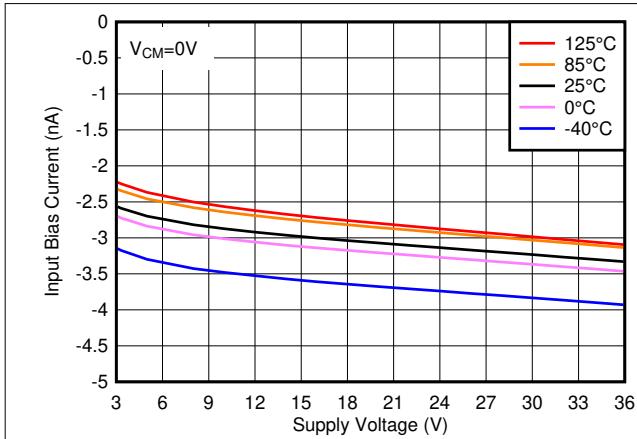


图 6-10. Input Bias Current vs. Supply Voltage

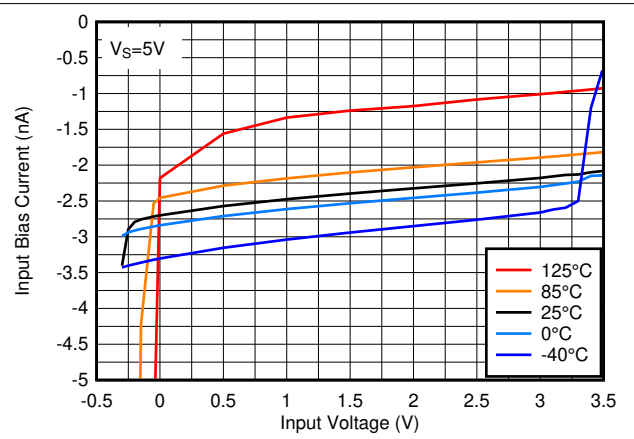


图 6-11. Input Bias Current vs. Input Voltage at 5V

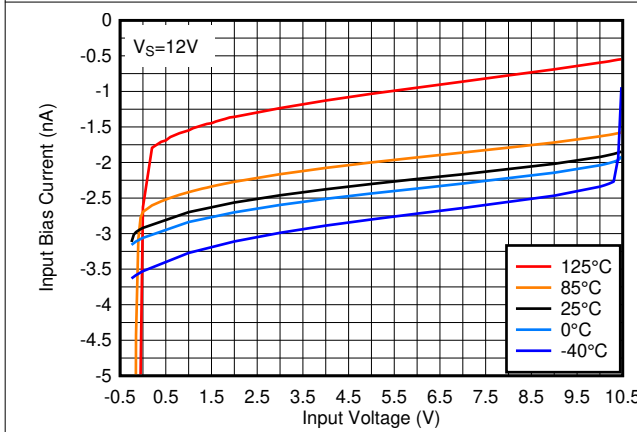


图 6-12. Input Bias Current vs. Input Voltage at 12V

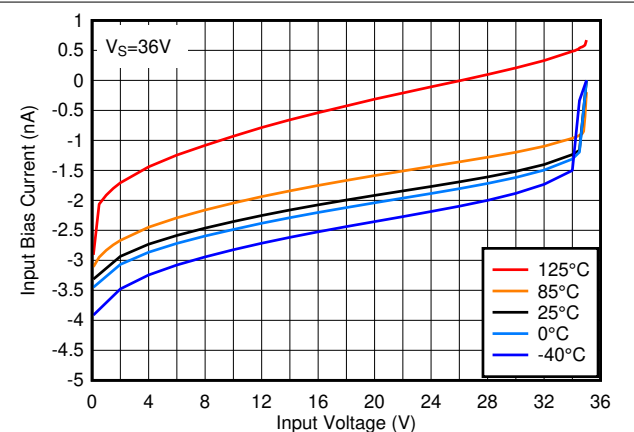


图 6-13. Input Bias Current vs. Input Voltage at 36V

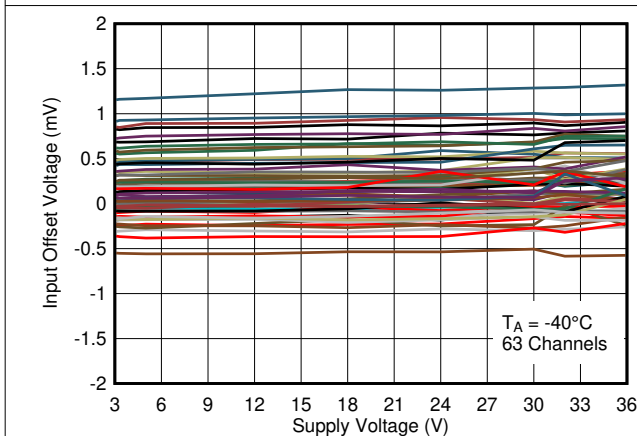


图 6-14. Input Offset Voltage vs. Supply Voltage at  $-40^\circ\text{C}$

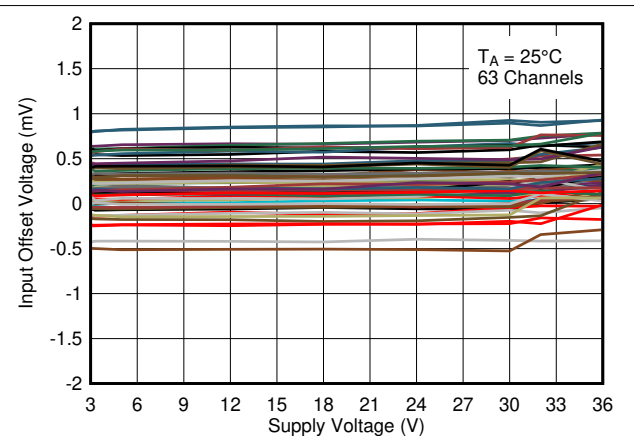


图 6-15. Input Offset Voltage vs. Supply Voltage at  $25^\circ\text{C}$

## 6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 5.1\text{ k}$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

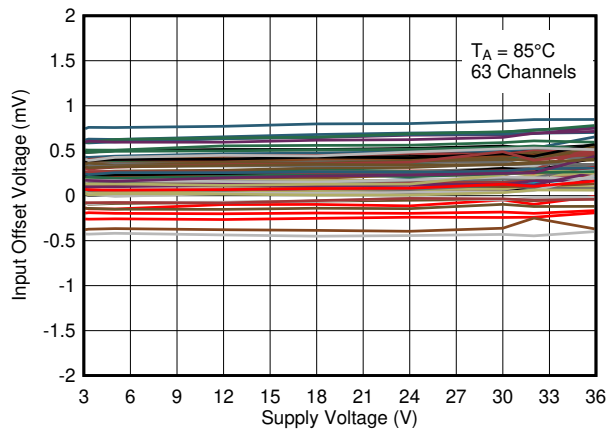


图 6-16. Input Offset Voltage vs. Supply Voltage at 85°C

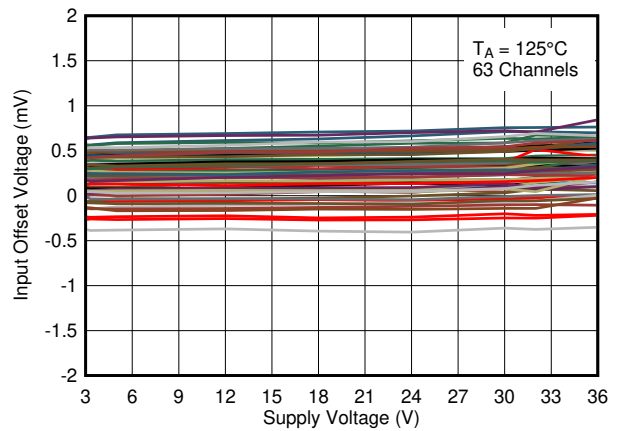


图 6-17. Input Offset Voltage vs. Supply Voltage at 125°C

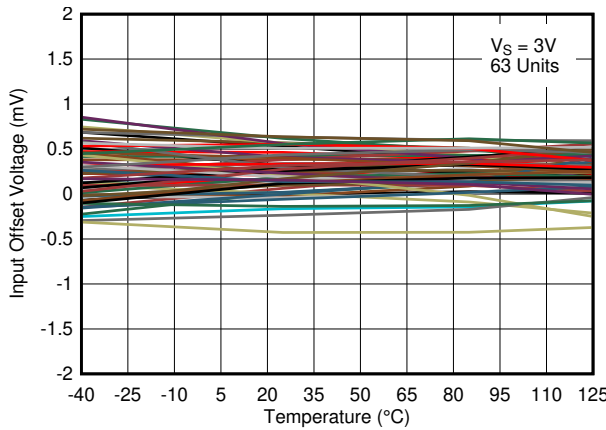


图 6-18. Input Offset Voltage vs. Temperature at 3V

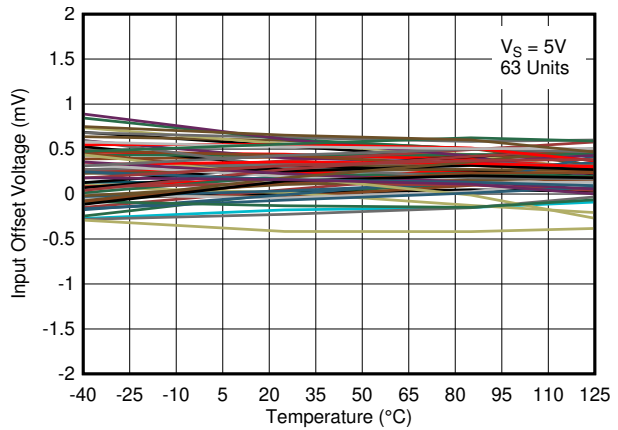


图 6-19. Input Offset Voltage vs. Temperature at 5V

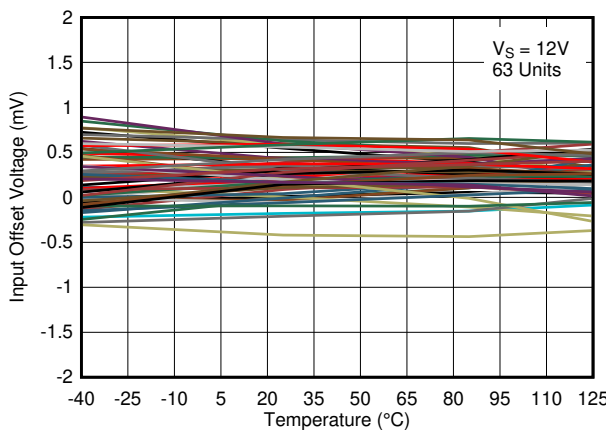


图 6-20. Input Offset Voltage vs. Temperature at 12V

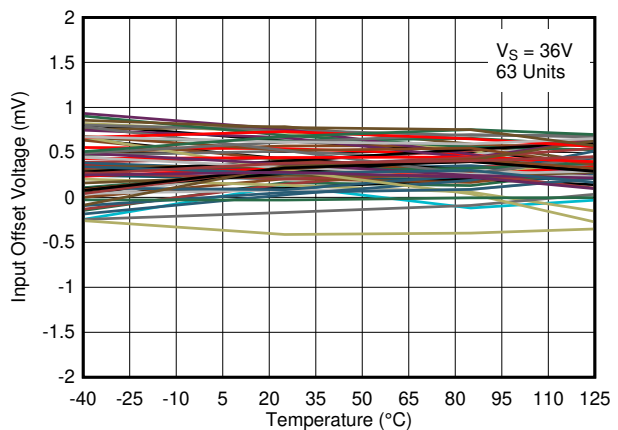


图 6-21. Input Offset Voltage vs. Temperature at 36V

### 6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 5.1\text{ k}$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

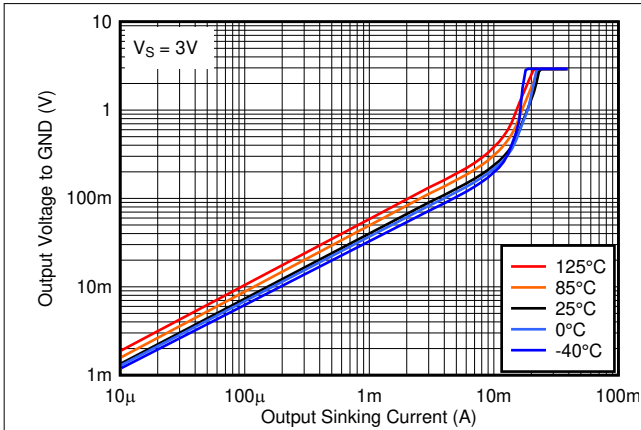


图 6-22. Output Low Voltage vs. Output Sinking Current at 3V

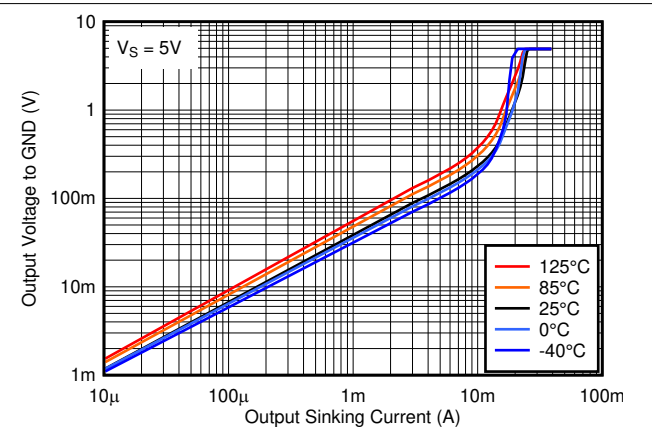


图 6-23. Output Low Voltage vs. Output Sinking Current at 5V

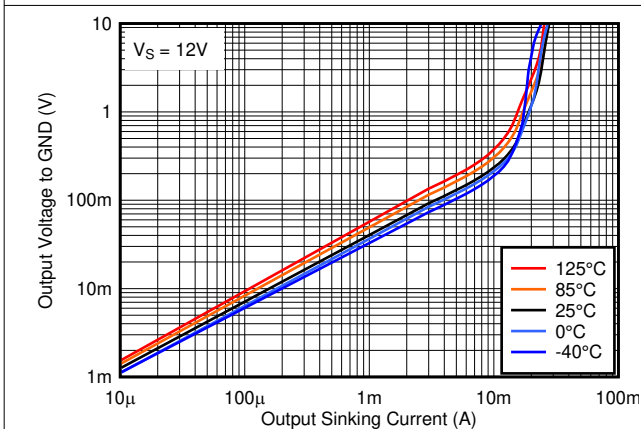


图 6-24. Output Low Voltage vs. Output Sinking Current at 12V

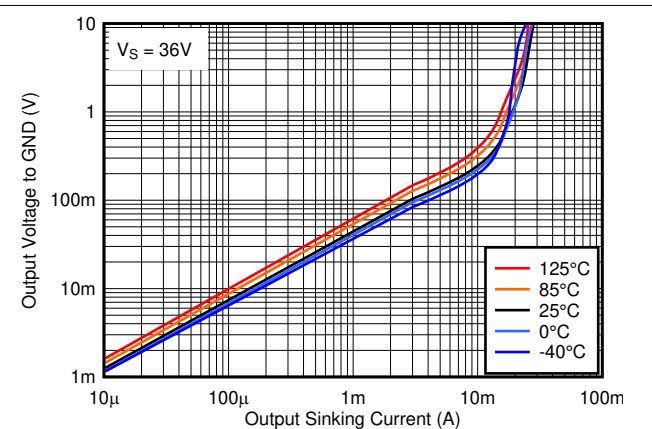


图 6-25. Output Low Voltage vs. Output Sinking Current at 36V

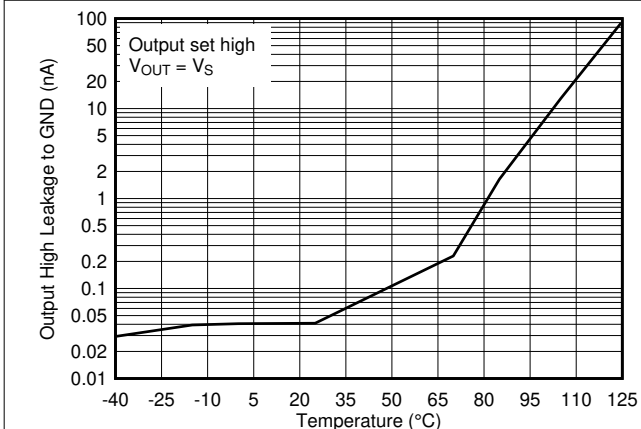


图 6-26. Output High Leakage Current vs. Temperature at 5V

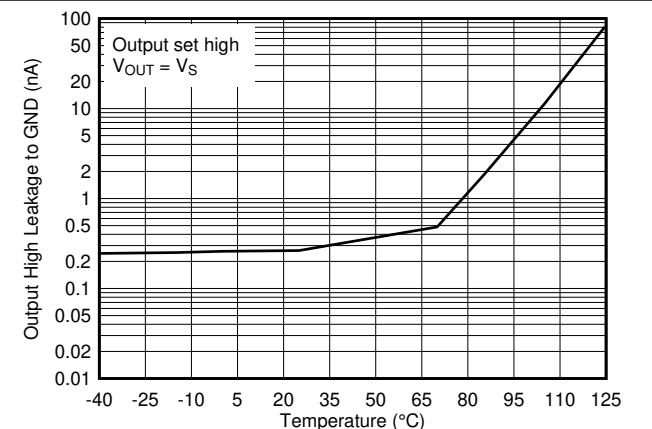
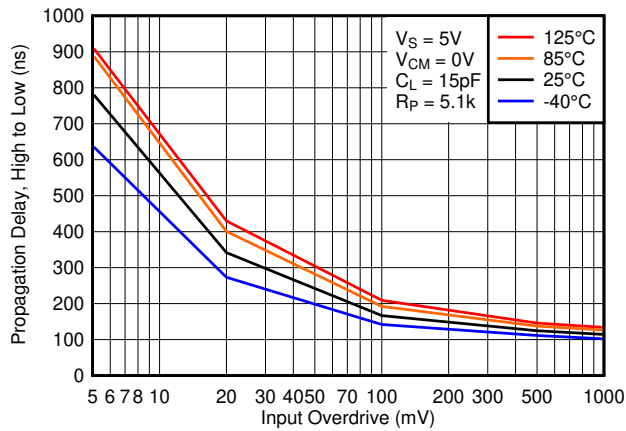


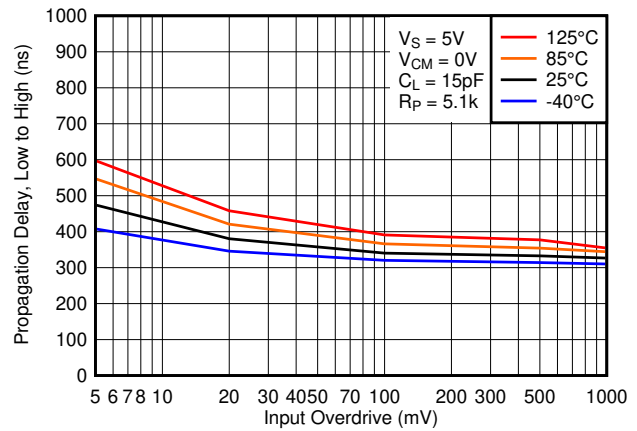
图 6-27. Output High Leakage Current vs. Temperature at 36V

### 6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

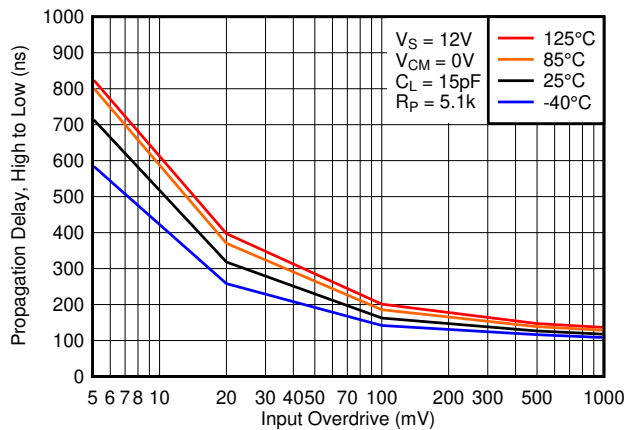
$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 5.1\text{ k}$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.



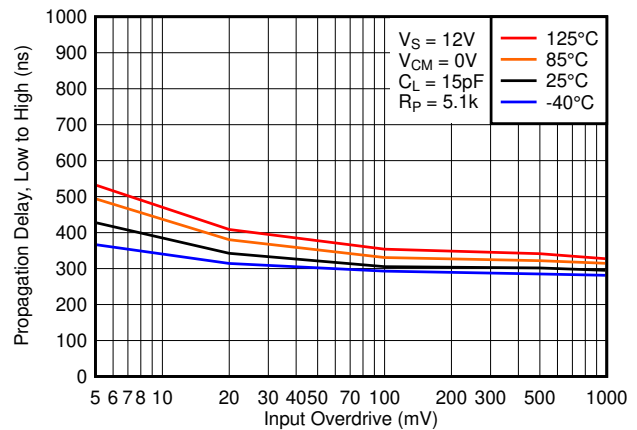
**图 6-28. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V**



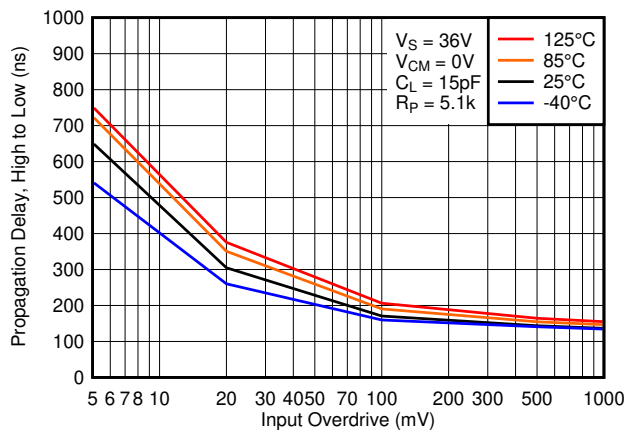
**图 6-29. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V**



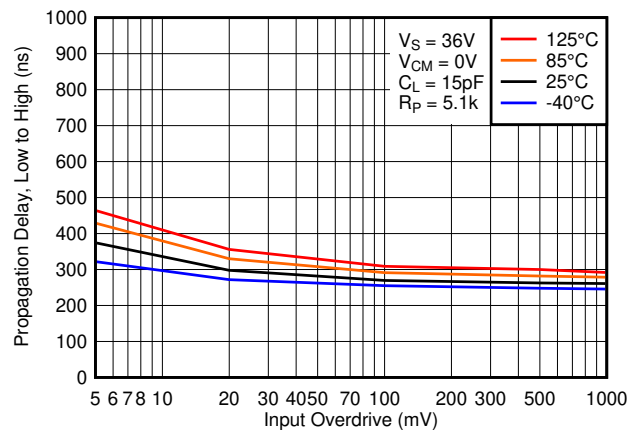
**图 6-30. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V**



**图 6-31. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V**



**图 6-32. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V**



**图 6-33. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V**

### 6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_{\text{PULLUP}} = 5.1\text{ k}$ ,  $C_L = 15\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

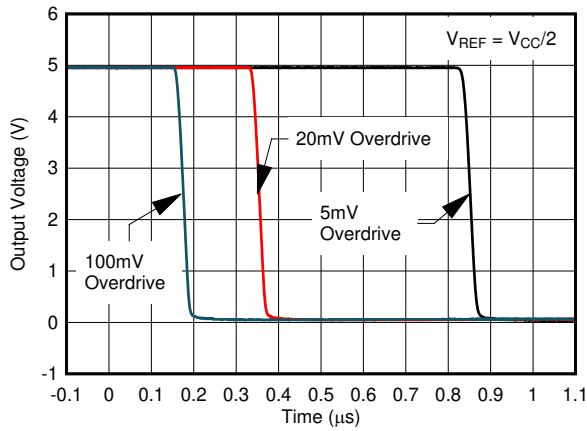


图 6-34. Response Time for Various Overdrives, High-to-Low Transition

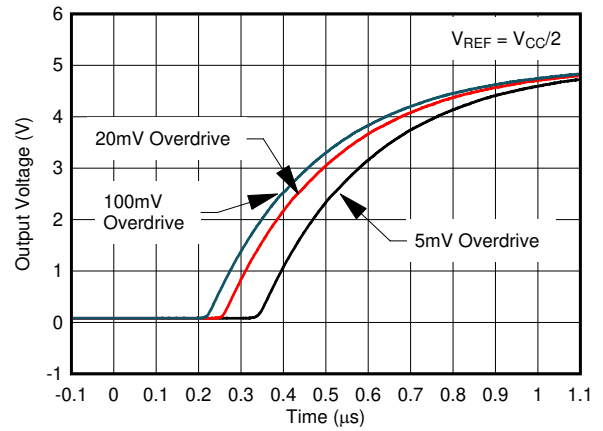


图 6-35. Response Time for Various Overdrives, Low-to-High Transition

## 7 Detailed Description

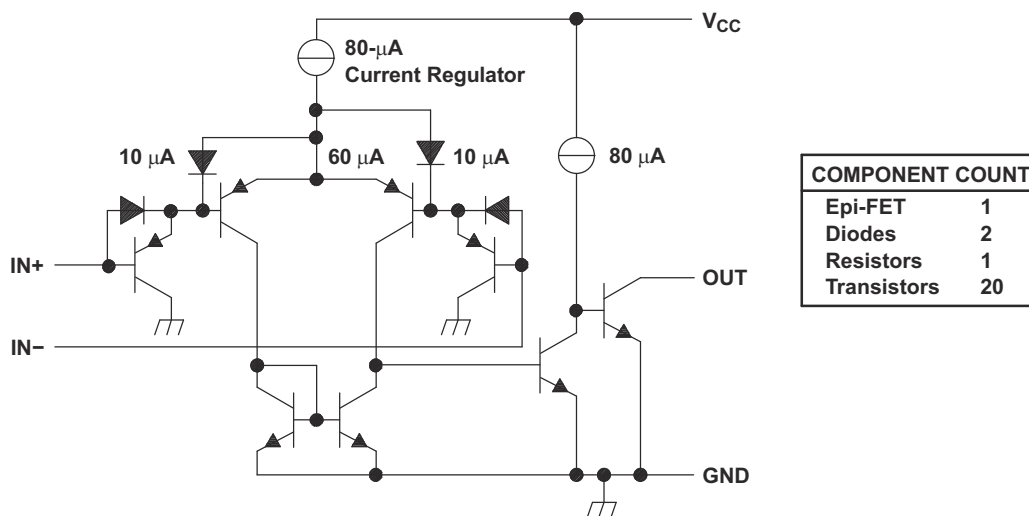
### 7.1 Overview

The TL331-Q1 is a single comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its very wide supply voltages range (2 V to 36 V), low  $I_q$ , and fast response.

The open-collector output allows the user to configure the output's logic low voltage ( $V_{OL}$ ) and can be utilized to enable the comparator to be used in AND functionality.

The TL331B-Q1 and TL391B-Q1 are performance upgrades to industry standard TL331-Q1 using the latest semiconductor process technologies that allows for lower offset voltages, lower input bias and supply currents and faster response times. The TL331B can drop-in replace the "I" or "Q" versions of TL331-Q1. The TL391B-Q1 is an alternate pinout of the TL331B-Q1 for replacing competitive devices.

### 7.2 Functional Block Diagram



Current values shown are nominal.

### 7.3 Feature Description

The TL331-Q1 consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing TL331-Q1 to accurately function from ground to  $V_{CC} - 1.5$  V differential input.

The output consists of an open collector NPN (pull-down or low side) transistor. The output NPN will sink current when the negative input voltage is higher than the positive input voltage and the offset voltage. The  $V_{OL}$  is resistive and will scale with the output current. Please see [Figure 6-3](#) for  $V_{OL}$  values with respect to the output current.

### 7.4 Device Functional Modes

#### 7.4.1 Voltage Comparison

The TL331-Q1 operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.



## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

TL331-Q1 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes TL331-Q1 optimal for level shifting to a higher or lower voltage.

### 8.2 Typical Application

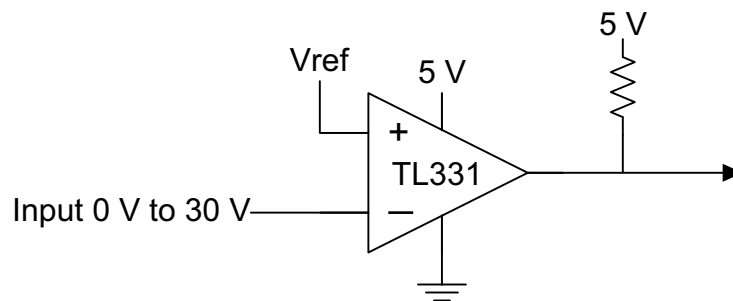


图 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

| DESIGN PARAMETER                             | EXAMPLE VALUE           |
|--|-------------------------|
| Input Voltage Range                          | 0 V to $V_{CC} - 1.5$ V |
| Supply Voltage                               | 2 V to 36 V             |
| Logic Supply Voltage ( $R_{PULLUP}$ Voltage) | 2 V to 36 V             |
| Output Current ( $V_{LOGIC}/R_{PULLUP}$ )    | 1 $\mu$ A to 4 mA       |
| Input Overdrive Voltage                      | 100 mV                  |
| Reference Voltage                            | 2.5 V                   |
| Load Capacitance ( $C_L$ )                   | 15 pF                   |

#### 8.2.2 Detailed Design Procedure

When using TL331-Q1 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

##### 8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range ( $V_{ICR}$ ) must be taken in to account. If temperature operation is above or below 25°C the  $V_{ICR}$  can range from 0 V to  $V_{CC} - 1.5$  V. This limits the input voltage range to as high as  $V_{CC} - 1.5$  V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
  - a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
  - b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

#### 8.2.2.2 TL331B-Q1 and TL391B-Q1 ESD Protection

The "B" versions add dedicated ESD protections on all the pins for improved ESD performance as well as improved negative input voltage handling. Please see Application Note [SNOAA35](#) for more information.

#### 8.2.2.3 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage ( $V_{IO}$ ). In order to make an accurate comparison the Overdrive Voltage ( $V_{OD}$ ) should be higher than the input offset voltage ( $V_{IO}$ ). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. [图 8-2](#) and [图 8-3](#) show positive and negative response times with respect to overdrive voltage.

#### 8.2.2.4 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current will produce a output low voltage ( $V_{OL}$ ) from the comparator. In which  $V_{OL}$  is proportional to the output current. Use [图 6-3](#) to determine  $V_{OL}$  based on the output current.

The output current can also effect the transient response. More is explained in the next section.

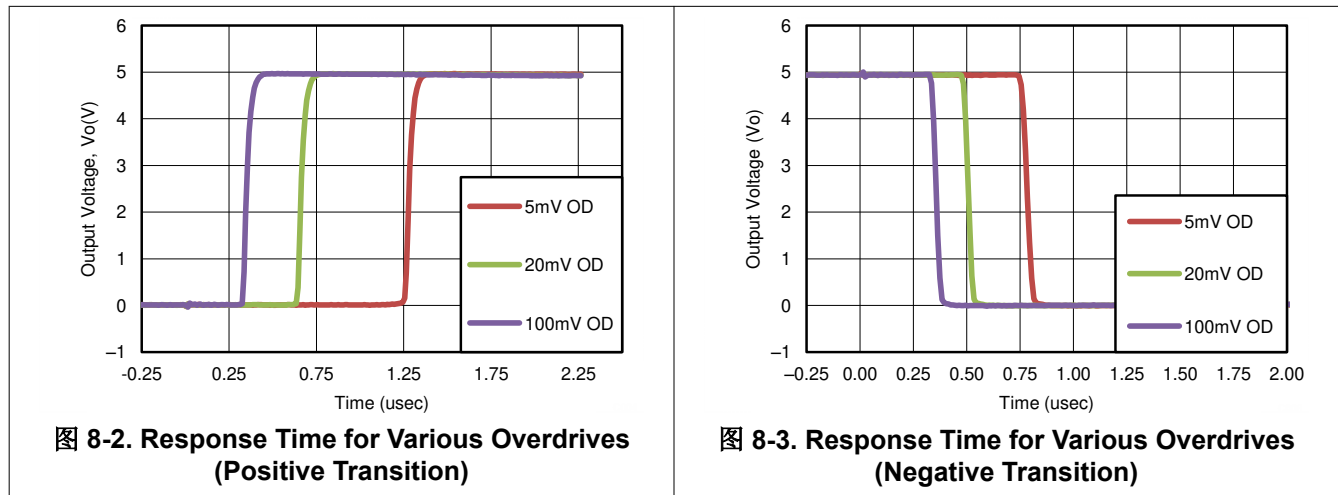
#### 8.2.2.5 Response Time

Response time is a function of input over drive. See [图 8.2.3](#) for typical response times. The rise and fall times can be determined by the load capacitance ( $C_L$ ), load/pullup resistance ( $R_{PULLUP}$ ), and equivalent collector-emitter resistance ( $R_{CE}$ ).

- The rise time ( $\tau_R$ ) is approximately  $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time ( $\tau_F$ ) is approximately  $\tau_F \sim R_{CE} \times C_L$ 
  - $R_{CE}$  can be determined by taking the slope of [图 6-3](#) in its linear region at the desired temperature, or by dividing the  $V_{OL}$  by  $I_{out}$

### 8.2.3 Application Curves

The following curves were generated with 5 V on  $V_{CC}$  and  $V_{Logic}$ ,  $R_{PULLUP} = 5.1\text{ k}\Omega$ , and 50 pF scope probe.



## 9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

## 10 Layout

### 10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

### 10.2 Layout Example

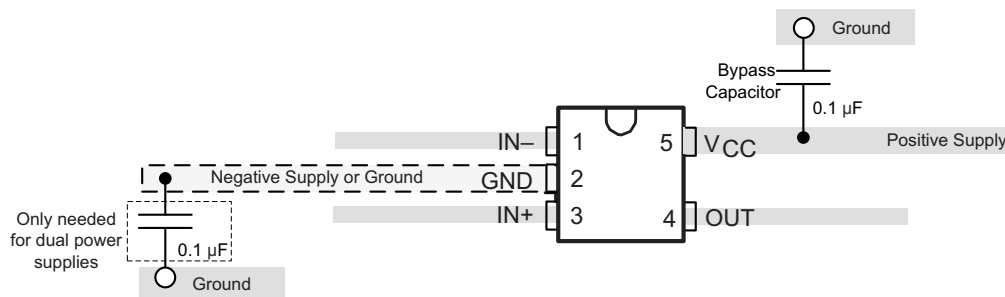


图 10-1. TL331-Q1 Layout Example

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

[Application Design Guidelines for LM339, LM393, TL331 Family Comparators](#) - SNOAA35

[Analog Engineers Circuit Cookbook: Amplifiers \(See Comparators section\)](#) - SLYY137

[Precision Design, Comparator with Hysteresis Reference Design](#)- TIDU020

[Window comparator circuit](#) - SBOA221

[Reference Design, Window Comparator Reference Design](#)- TIPD178

[Comparator with and without hysteresis circuit](#) - SBOA219

[Inverting comparator with hysteresis circuit](#) - SNOA997

[Non-Inverting Comparator With Hysteresis Circuit](#) - SBOA313

[Zero crossing detection using comparator circuit](#) - SNOA999

[A Quad of Independently Functioning Comparators](#) - SNOA654

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 11.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL331BQDBVRQ1    | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 31BQ                    | <a href="#">Samples</a> |
| TL331IDBVRQ1     | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | TQ1U                    | <a href="#">Samples</a> |
| TL331QDBVRQ1     | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | T1RU                    | <a href="#">Samples</a> |
| TL391BQDBVRQ1    | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 91BQ                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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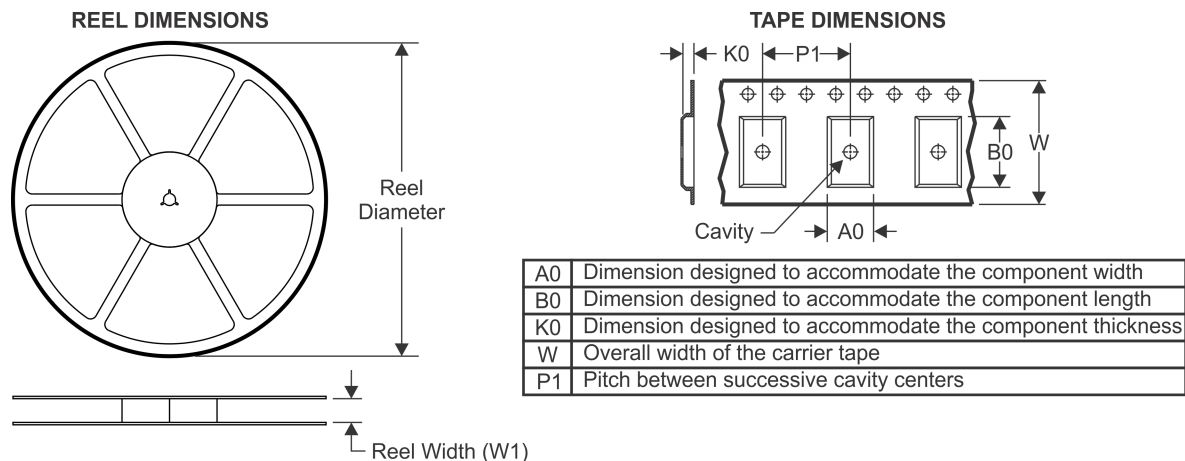
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL331-Q1, TL331B-Q1, TL391B-Q1 :**

- Catalog : [TL331](#), [TL331B](#), [TL391B](#)
- Enhanced Product : [TL331-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL331BQDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TL331IDBVRQ1  | SOT-23       | DBV             | 5    | 3000 | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TL331QDBVRQ1  | SOT-23       | DBV             | 5    | 3000 | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TL391BQDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL331BQDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| TL331IDBVRQ1  | SOT-23       | DBV             | 5    | 3000 | 200.0       | 183.0      | 25.0        |
| TL331QDBVRQ1  | SOT-23       | DBV             | 5    | 3000 | 200.0       | 183.0      | 25.0        |
| TL391BQDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |



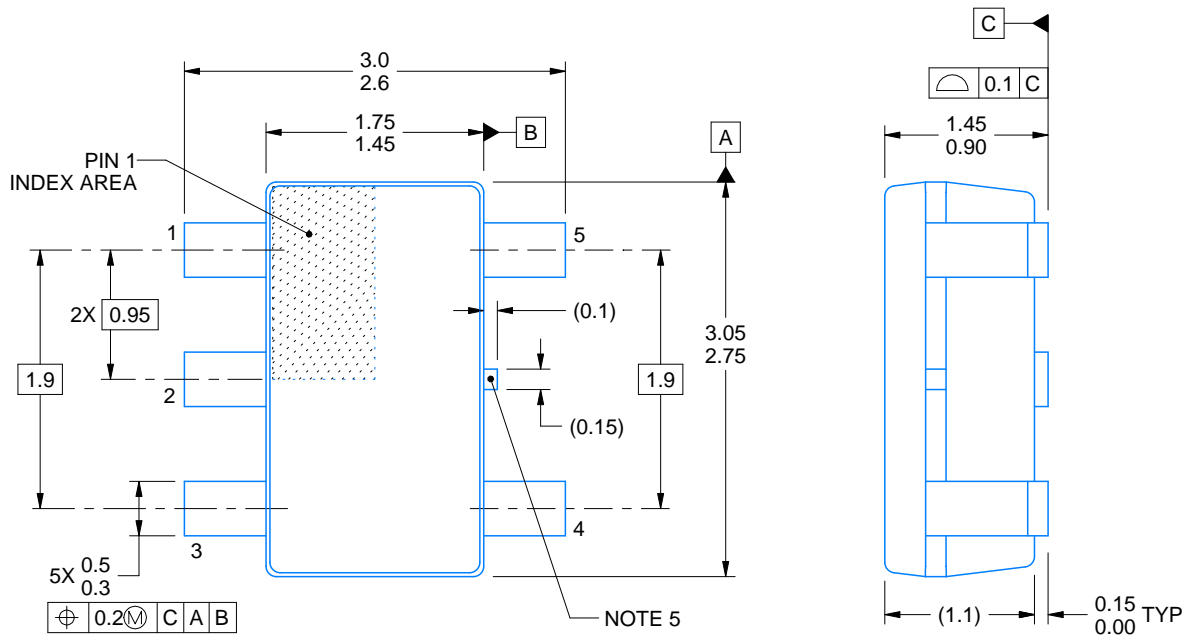
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



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