

## 带有升压直流/直流转换器、 电平转换器和 ESD 钳位的 TPD5S115 HDMI 配套芯片

### 1 特性

- 符合 HDMI 合规性测试，无需任何外部组件
- 支持 HDMI 2.0、HDMI 1.4 和 HDMI 1.3 标准
- 与 HDMI 连接器引脚映射相匹配
- 内部 DC-DC 转换器以从一个低至 2.3V 的电池电压生成 5V 电压
- CEC、SDA 和 SCL 路径内的自动方向感应、电平转换和缓冲
- IEC 61000-4-2 (4 级) 系统级 ESD 兼容
- 反向电流阻断和短路保护以防止出现故障状况
- 工业温度范围: -40°C 至 85°C

### 2 应用

- 机顶盒
- 电视
- 智能手机
- 数码摄像机
- 便携式游戏机
- 数码相机

### 3 说明

TPD5S115 器件是一款集成式 HDMI 配套芯片解决方案。该器件提供稳定的 5V 输出电压 (5VOUT)，用于为 HDMI 电源线路供电。稳定的 5V 输出电压可为 HDMI 接收器提供高达 55mA 的电流，同时具备电流限制功能。TPD5S115 采用两个控制信号：EN 和 LS\_OE。5VOUT 和热插拔检测 (HPD) 电路的控制独立于 LS\_OE 控制信号，并由 EN 引脚控制。EN 引脚可在打开整个 HDMI 链路之前激活检测系统 (5VOUT+HPD)。只有当 EN 也被激活时，LS\_OE 才激活内部 LDO，CEC，SCL 和 SDA 缓冲器。这个双极启用方案能够确保针对便携式应用的省电优化。

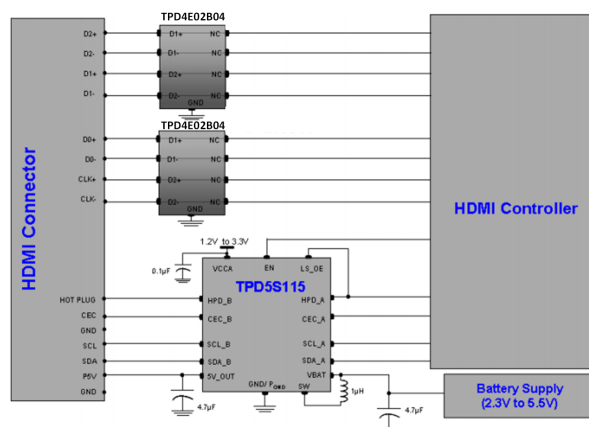
有 3 个适用于 SDA、SCL 和 CEC 线路的同相双向电压级转换电路。每个电路在 A 侧具有一个介于 1.1V 至 3.6V 之间的共同电源轨 (VCCA)。在 B 侧，SCL\_B 和 SDA\_B 各有一个被连接至经稳压 5V 电源轨 (5VOUT) 的内部 1.75kΩ 上拉电阻器。DDC (SCL\_B 和 SDA\_B) 引脚符合 I<sup>2</sup>C 技术规格，使用缓冲器可驱动高达 750pF 的负载。CEC\_B 引脚具有一个与内部 3.3V 电源相连的 27kΩ 上拉电阻器。TPD5S115 超过了 IEC61000-4-2 (4 级) ESD 保护级别。该器件采用节省空间的间距 0.4mm 的 1.72mm × 1.72mm YFF 封装。

#### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPD5S115	DSBGA (16)	1.72mm × 1.72mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

#### 典型系统图



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## 4 修订历史记录

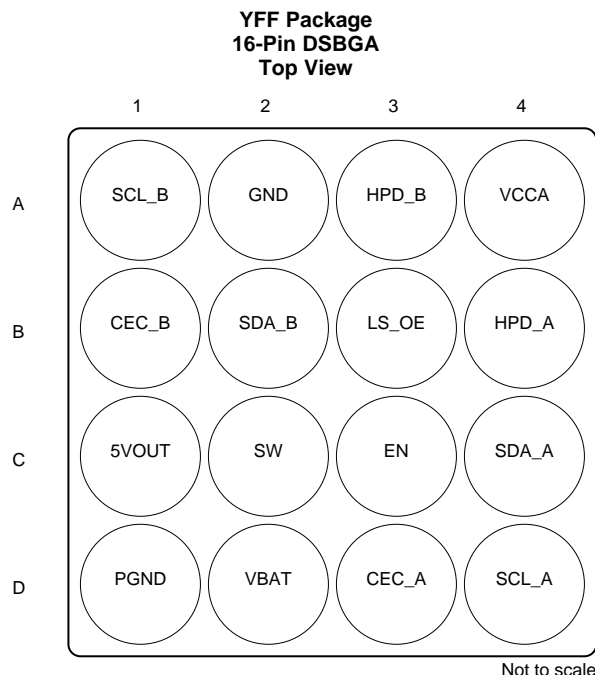
注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Revision C (December 2016) to Revision D</b>	<b>Page</b>
• Updated Pinout image .....	<b>3</b>

<b>Changes from Revision B (March 2013) to Revision C</b>	<b>Page</b>
• 已添加 器件信息表、引脚配置和功能部分、规格部分、ESD 额定值表、详细 说明部分、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 .....	<b>1</b>
• 已删除 订购信息表；请参见数据表末尾的 POA .....	<b>1</b>
• Added <i>Thermal Information</i> table .....	<b>5</b>
• Moved the passive components parameters from <i>Recommended Operating Conditions</i> table to the <i>Output Capacitor</i> section .....	<b>18</b>

<b>Changes from Revision A (February 2013) to Revision B</b>	<b>Page</b>
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## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
5VOUT	C1	O	DC-DC output. The 5-V power pin can supply a 55-mA regulated current to the HDMI receiver. A separate DC-DC converter control pin (EN) disables the DC-DC converter when operating at low-power mode
CEC_A	D3	I/O	LS system side CEC bus I/O. This pin is bidirectional and referenced to VCCA
CEC_B	B1	I/O	LS HDMI connector side CEC bus I/O. This pin is bidirectional and referenced to the 3.3-V internal supply
EN	C3	C	DC-DC enable. Enables the DC-DC converter and HPD circuitry when EN is HIGH. The EN is referenced based off VCCA
GND	A2	G	Device ground
HPD_A	B4	O	System side output for the hot plug detect. This pin is unidirectional and is referenced to VCCA
HPD_B	A3	I	HDMI side input for the hot plug detect. This pin is unidirectional and is referenced to 5VOUT
LS_OE	B3	C	Level shifter enable. This pin is referenced to VCCA. Enables level shifters and LDO when EN is HIGH and LS_OE is HIGH
PGND	D1	G	DC-DC converter ground. These pins are isolated from the GND pins. This pin should be tied to system GND
SCL_A, SDA_A	D4, C4	I/O	LS system side input and output for I <sup>2</sup> C Bus. These pins are bidirectional and referenced to VCCA
SCL_B, SDA_B	A1, B2	I/O	LS HDMI side connector side input and output for I <sup>2</sup> C Bus. These pins are bidirectional and referenced to 5VOUT
SW	C2	I	Switch input. This pin is the inductor input for the DC-DC converter
VBAT	D2	P	Battery supply. This voltage is typically 2.3 V to 5.5 V
VCCA	A4	P	System side supply. This voltage is typically 1.2 V to 3.3 V from the core microcontroller

(1) C = Control, G = Ground, I = Input, O = Output, P = Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	VCCA		4	V
	VBAT	-0.3	6	V
Input voltage, $V_I$ <sup>(2)</sup>	SCL_A, SDA_A, CEC_A	-0.3	4	V
	SCL_B, SDA_B, CEC_B, HPD_B	-0.3	6	
	EN, LS_OE	-0.3	4	
Voltage applied to any output in the high-impedance or power-off state, $V_O$ <sup>(2)</sup>	SCL_A, SDA_A, CEC_A	-0.3	4	V
	SCL_B, SDA_B, CEC_B	-0.3	6	
Voltage applied to any output in the high or low state, $V_O$ <sup>(2)</sup>	SCL_A, SDA_A, CEC_A	-0.3	VCCA + 0.3	V
	SCL_B, SDA_B, CEC_B	-0.3	5VOUT + 0.3	
Input clamp current ( $I_V < 0$ )			-50	mA
Output clamp current ( $V_O < 0$ )			-50	mA
Continuous current through 5VOUT, or GND			±100	mA
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	All pins except pins 4A, B3, C3, C4, D3, and D4	500	V
		Pins 4A, B3, C3, C4, D3, and D4	2000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		1000	
	IEC 61000-4-2 Contact Discharge	Pins A1, A3, B1, B2, and C1	±14000	
	IEC 61000-4-2 Air-gap Discharge	Pins A1, A3, B1, B2, and C1	±16000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CCA}$	Supply voltage, VCCA	1.2		3.6	V
$V_{BAT}$	Supply voltage, VBAT	2.3		5.5	V
$V_{IH}$	High-level input voltage	VCCA = 1.2 V to 3.6 V	SCL_A, SDA_A	$0.7 \times V_{CCA}$	$V_{CCA}$
			CEC_A	$0.7 \times V_{CCA}$	$V_{CCA}$
			EN, LS_OE	1	$V_{CCA}$
	5VOUT = 5 V		SCL_B, SDA_B	$0.7 \times 5VOUT$	5VOUT
			CEC_B	$0.7 \times 3.3 V$ (internal) <sup>(1)</sup>	3.3 V (internal) <sup>(1)</sup>
			HPD_B	2	

- (1) 3.3 V (internal) is an internally generated voltage node for the CEC\_B output buffer supply reference. An LDO generates this 3.3 V from 5VOUT when LS\_OE and EN are HIGH.

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>IL</sub>	Low-Level input voltage	V <sub>CCA</sub> = 1.2 V to 3.6 V	SCL_A, SDA_A	–0.5	0.082 × V <sub>CCA</sub>	V
			CEC_A	–0.5	0.082 × V <sub>CCA</sub>	
			EN, LS_OE	–0.5	0.4	
	5VOUT = 5 V	SCL_B, SDA_B	–0.5	0.3 × 5VOUT		
		CEC_B	–0.5	0.3 × 3.3 (internal) <sup>(1)</sup>		
		HPD_B	0	0.8		
V <sub>ILC</sub>	Low-level input voltage		–0.5	0.065 × V <sub>CCA</sub>	V	
V <sub>OL</sub> – V <sub>ILC</sub>	Delta between V <sub>OL</sub> and V <sub>ILC</sub> (V <sub>IO</sub> = 2.5 V)		0.1 × V <sub>CCA</sub>		V	
T <sub>A</sub>	Operating free-air temperature		–40		85	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD5S115	UNIT
		YFF (DSBGA)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	78.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	13.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

T<sub>A</sub> = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V <sub>OHA</sub>		I <sub>OH</sub> = –10 μA, V <sub>I</sub> = V <sub>IH</sub> , V <sub>CCA</sub> = 1.2 V to 3.6 V		V <sub>CCA</sub> × 0.8			V	
V <sub>OLA</sub>		I <sub>OL</sub> = 10 μA, V <sub>I</sub> = V <sub>IL</sub> , V <sub>CCA</sub> = 1.2 V to 3.6 V		V <sub>CCA</sub> × 0.16			V	
V <sub>OHB</sub>		I <sub>OH</sub> = –10 μA, V <sub>I</sub> = V <sub>IH</sub>					V	
V <sub>OLB</sub>		I <sub>OL</sub> = 3 mA, V <sub>I</sub> = V <sub>IL</sub>				0.4	V	
R <sub>PU</sub>	Internal pullup	SCL_A, SDA_A	Pullup connected to V <sub>CCA</sub> rail	10			kΩ	
		SCL_B, SDA_B	Pullup connected to 5-V rail	1.75				
I <sub>PULLUPAC</sub>	Transient boosted pullup current (rise-time accelerator)	SCL_B, SDA_B	Pullup connected to 5-V rail	15			mA	
I <sub>OFF</sub>	Leakage current	A port	V <sub>CCA</sub> = 0 V, V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V, V <sub>CCA</sub> = 0 V			±5	μA	
		B port	5VOUT = 0 V, V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V, V <sub>CCA</sub> = 0 V to 3.6 V			±5		
I <sub>OZ</sub>		A port	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>CCA</sub> = 1.2 V to 3.6 V			±5		
		B port	V <sub>I</sub> = V <sub>CCI</sub> or GND, V <sub>CCA</sub> = 1.2 V to 3.6 V			±5		
C <sub>L</sub>	Bus load capacitance	A port				15	pF	
		B port				750		
<b>SUPPLY CURRENT</b>								
I <sub>CCA</sub>	V <sub>CCA</sub> supply current	Standby	I/Os = HIGH			2	μA	
		Active	I/Os = HIGH			15	μA	
I <sub>CCB</sub>	V <sub>BAT</sub> supply current	Standby	EN = LOW, LS_OE = LOW			0.5	μA	
		DC-DC and HPD active	EN = HIGH, LS_OE = LOW			30	50	μA
		DC-DC, HPD, DDC, CEC Active	EN = HIGH, LS_OE = LOW, I/Os = HIGH			225	300	μA

**Electrical Characteristics (continued)**
 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC-DC CONVERTER</b>						
$V_{BAT}$	Input voltage		2.3		5.5	V
$V_{OUT}$	Total DC output voltage <sup>(1)</sup>		4.9	5	5.13	V
$T_{OVA}$	Total output voltage accuracy <sup>(2)</sup>		4.8	5	5.3	V
$V_{IO\_Ripple}$	Output voltage ripple, loaded	$I_O = 65\text{ mA}$		50.6		mV <sub>pp</sub>
		$I_O = 150\text{ mA}$		16		
$f_{CLK}$	Internal operating frequency	$V_{BAT} = 2.3\text{ V to }5.5\text{ V}$		3.5		MHz
$t_{START}$	Start-up time	From EN input to 5-V power output 90% point		187		μs
$I_O$	Output current	$V_{BAT} = 2.3\text{ V to }5.5\text{ V}$	55			mA
	Reverse leakage current, $V_O$	EN = LOW, $V_O = 5.5\text{ V}$			2.5	μA
	Leakage current from battery to $V_O$	EN = LOW			5	μA
$V_{BATUV}$	Undervoltage lockout threshold	Falling		2		V
		Rising		2.1		V
	Line transient response	$V_{BAT} = 3.4\text{ V}$ , $I_O = 20\text{ mA to }65\text{ mA}$ , A 217 Hz, 600 mV <sub>pp</sub> square wave pulse		17.1		mV <sub>pk</sub>
	Load transient response	$V_{BAT} = 3.4\text{ V}$ , $I_O = 5\text{ mA to }65\text{ mA}$ , 10-μs pulse, $t_{RISE} = t_{FALL} = 0.1\text{ μs}$		63.5		mV <sub>pk</sub>
$I_{INRUSH}$	Inrush current, average over $t_{START}$	$V_{BAT} = 2.3\text{ V to }5.5\text{ V}$ , $I_{OUT} = 65\text{ mA}$		168		mA
$I_{SC}$	Short-circuit current limit from output			90		mA
<b>VOLTAGE LEVEL SHIFTER CEC LINE (x_A &amp; x_B PORTS)</b>						
$V_{OHA}$		$I_{OH} = -10\text{ μA}$ , $V_I = V_{IH}$ , $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$	$V_{CCA} \times 0.8$			V
$V_{OLA}$		$I_{OL} = 10\text{ μA}$ , $V_I = V_{IL}$ , $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$		$V_{CCA} \times 0.16$		V
$V_{OHB}$		$I_{OH} = -20\text{ μA}$ , $V_I = V_{IH}$	$V_{CCA} \times 0.8$			V
$V_{OLB}$		$I_{OL} = 3\text{ mA}$ , $V_I = V_{IL}$			0.4	V
$R_{PU}$	Internal pullup	CEC_A	Pullup connected to $V_{CCA}$ rail	10		kΩ
		CEC_B	Pullup connected to 3.3 V rail	22	26	
$R_{PD}$	Internal pulldown	CEC_B	Pullup connected to GND	14		MΩ
$I_{OFF}$	A port	$V_{CCA} = 0\text{ V}$ , $V_I$ or $V_O = 0$ to 3.6 V, $V_{CCA} = 0\text{ V}$			±5	μA
	B port	$5V_{OUT} = 0\text{ V}$ , $V_I$ or $V_O = 0$ to 5.5 V, $V_{CCA} = 0\text{ V to }3.6\text{ V}$			±1.8	
$I_{OZ}$	A port	$V_O = V_{CCO}$ or GND, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$			±5	μA
	B port	$V_I = V_{CCI}$ or GND, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$			±5	
<b>VOLTAGE LEVEL SHIFTER - HPD LINE (X_A &amp; x_B)</b>						
$V_{OHA}$		$I_{OH} = -3\text{ mA}$ , $V_I = V_{IH}$ , $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$	$V_{CCA} \times 0.7$			V
$V_{OLA}$		$I_{OL} = 3\text{ mA}$ , $V_I = V_{IL}$ , $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$			0.4	V
$R_{PD}$	Internal pulldown	HPD_B	Pullup connected to GND	100		kΩ
$I_{OZ}$		A port	$V_I = V_{CCI}$ or GND, $V_{CCA} = 3.6\text{ V}$			±5
<b>LS_OE, EN</b>						
$I_i$		$V_I = V_{CCA}$ or GND, $V_{CCA} = 1.2\text{ V to }3.6\text{ V}$				±12

(1) Includes voltage references, DC load and line regulations, process and temperature.

(2) Includes voltage references, DC load and line regulations, transient load and line regulations, ripple, process, and temperature.

## 6.6 Electrical Characteristics – I/O Capacitances

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Capacitance	EN, LS_OE	$V_{BIAS} = 1.8\text{ V}$ , $f = 1\text{ MHz}$ , 30-mV <sub>pp</sub> AC signal	$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$		7.1	9.5	pF
	SCL_A, SDA_A, CEC_A		$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$ , EN = LOW		7		pF
	HPD_A, HPD_B		$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$ , EN = LOW		4		pF
	SCL_B, SDA_B	$V_{BIAS} = 2.5\text{ V}$ , $f = 100\text{ kHz}$ , 3.5-V <sub>pp</sub> AC signal	$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$ , EN = LOW, LS_OE = HIGH		10		pF
	CEC_B	$V_{BIAS} = 1.65\text{ V}$ , $f = 100\text{ kHz}$ , 2.5-V <sub>pp</sub> AC signal	$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$ , EN = LOW, LS_OE = HIGH		7		pF
	CEC_B		$V_{CCA} = 0\text{ V}$ , $5V_{IN} = 0\text{ V}$		7		pF

## 6.7 Switching Characteristics – $V_{CCA} = 1.2\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SCL and SDA LINES (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	DDC channels enabled		394		ns
		B to A	DDC channels enabled		347		
$t_{PLH}$	Low-to-high propagation delay	A to B	DDC channels enabled		504		ns
		B to A	DDC channels enabled		171		
$t_{FALL}$	Fall time	A port	DDC channels enabled		146		ns
		B port	DCC channels enabled		135		
$t_{RISE}$	Rise time	A port	DCC channels enabled		190		ns
		B port	DCC channels enabled		93		
$f_{MAX}$	Maximum switching frequency		DCC channels enabled		400		kHz
<b>CEC LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	CEC channels enabled		550		ns
		B to A	CEC channels enabled		350		
$t_{PLH}$	Low-to-high propagation delay	A to B	CEC channels enabled		13		μs
		B to A	CEC channels enabled		290		
$t_{FALL}$	Fall time	A port	CEC channels enabled		146		ns
		B port	CEC channels enabled		200		
$t_{RISE}$	Rise time	A port	CEC channels enabled		190		ns
		B port	CEC channels enabled		16.4		
<b>HPD LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	Propagation delay	B to A	CEC channels enabled		10.4		ns
$t_{PLH}$	Low-to-high propagation delay	B to A	CEC channels enabled		9.9		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		0.7		ns
$t_{RISE}$	Rise time	A port	CEC channels enabled		0.8		ns

## 6.8 Switching Characteristics – $V_{CCA} = 1.5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SCL, SDA LINES (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	DDC channels enabled		375		ns
		B to A	DDC channels enabled		272		
$t_{PLH}$	Low-to-high propagation delay	A to B	DDC channels enabled		488		ns
		B to A	DDC channels enabled		166		
$t_{FALL}$	Fall time	A port	DDC channels enabled		114		ns
		B port	DCC channels enabled		135		
$t_{RISE}$	Rise time	A port	DCC channels enabled		186		ns
		B port	DCC channels enabled		93		
$f_{MAX}$	Maximum switching frequency		DCC channels enabled		400		kHz
<b>CEC Line (x_A &amp; x_B Ports)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	CEC channels enabled		536		ns
		B to A	CEC channels enabled		272		
$t_{PLH}$	Low-to-high propagation delay	A to B	CEC channels enabled		13		$\mu\text{s}$
		B to A	CEC channels enabled		285		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		113		ns
		B port	CEC channels enabled		201		
$t_{RISE}$	Rise time	A port	CEC channels enabled		187		ns
		B port	CEC channels enabled		16		$\mu\text{s}$
<b>HPD LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	B to A	CEC channels enabled		10		ns
$t_{PLH}$	Low-to-high propagation delay	B to A	CEC channels enabled		10		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		0.46		ns
$t_{RISE}$	Rise time	A port	CEC channels enabled		0.5		ns

## 6.9 Switching Characteristics – $V_{CCA} = 1.8\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SCL, SDA LINES (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	DDC channels enabled		370		ns
		B to A	DDC channels enabled		230		
$t_{PLH}$	Low-to-high propagation delay	A to B	DDC channels enabled		480		ns
		B to A	DDC channels enabled		163		
$t_{FALL}$	Fall time	A port	DDC channels enabled		100		ns
		B port	DCC channels enabled		135		
$t_{RISE}$	Rise time	A port	DCC channels enabled		180		ns
		B port	DCC channels enabled		93		
$f_{MAX}$	Maximum switching frequency		DCC channels enabled		400		kHz
<b>CEC LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	CEC channels enabled		530		ns
		B to A	CEC channels enabled		230		
$t_{PLH}$	Low-to-high propagation delay	A to B	CEC channels enabled		13		$\mu\text{s}$
		B to A	CEC channels enabled		280		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		98		ns
		B port	CEC channels enabled		200		



**Switching Characteristics –  $V_{CCA} = 1.8\text{ V}$  (continued)**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{RISE}$	Rise time	A port	CEC channels enabled		180		ns
		B port	CEC channels enabled		16		$\mu\text{s}$
<b>HPD LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	B to A	CEC channels enabled		10		ns
$t_{PLH}$	Low-to-high propagation delay	B to A	CEC channels enabled		10		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		0.41		ns
$t_{RISE}$	Rise time	A port	CEC channels enabled		0.41		ns

**6.10 Switching Characteristics –  $V_{CCA} = 2.5\text{ V}$** 

over operating free-air temperature range (unless otherwise noted)

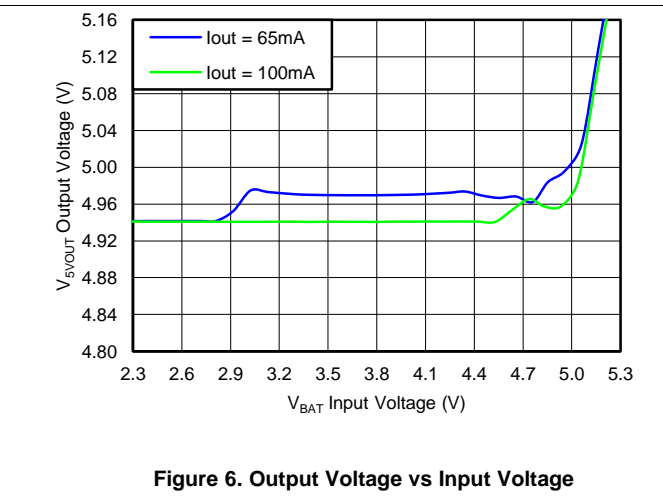
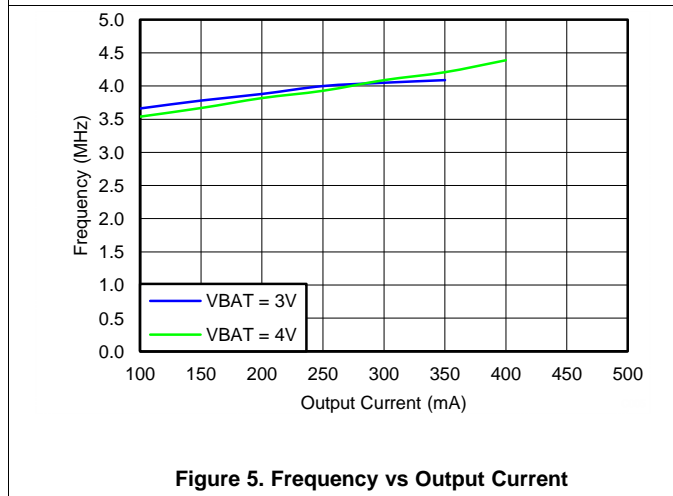
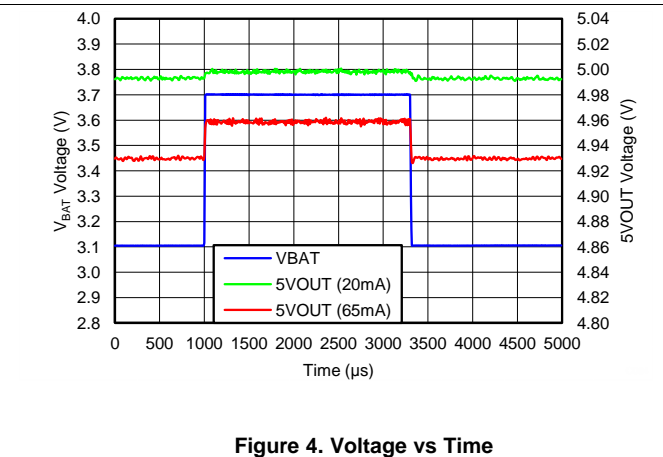
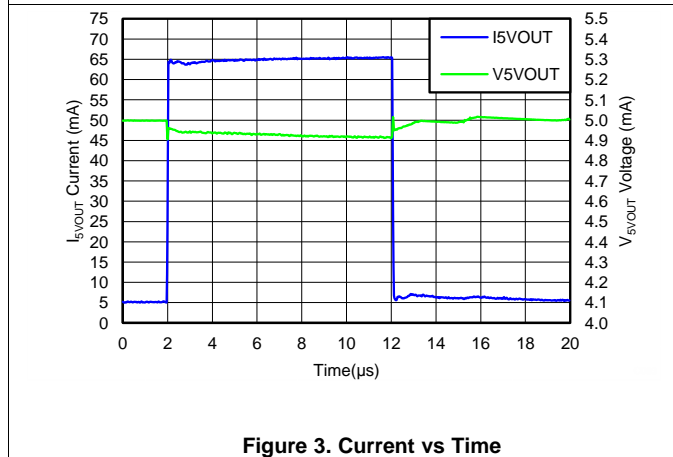
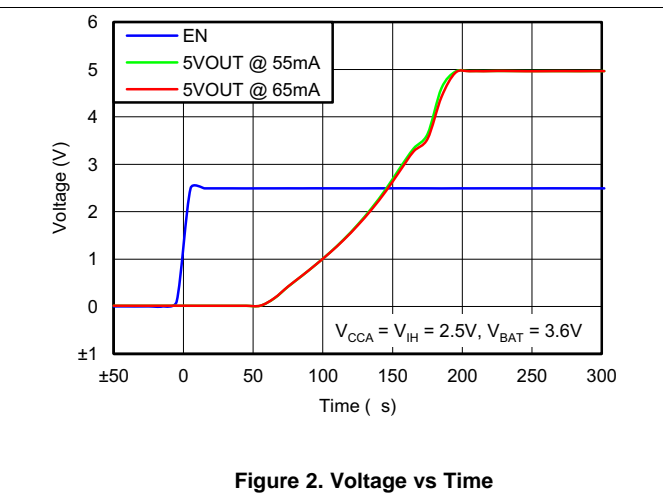
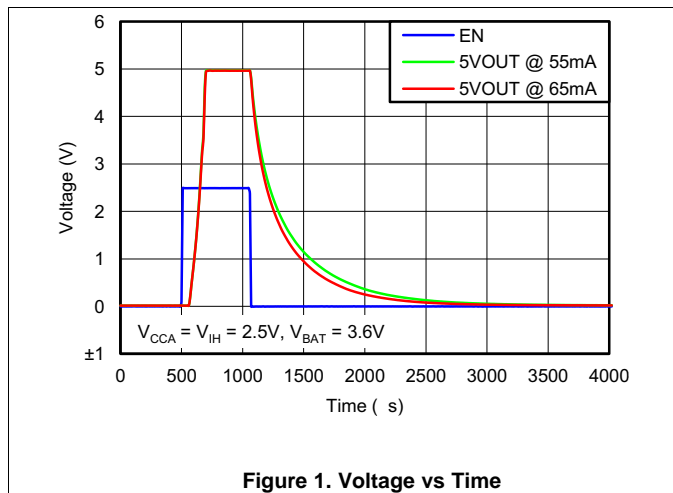
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SCL, SDA LINES (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	DDC channels enabled		370		ns
		B to A	DDC channels enabled		185		
$t_{PLH}$	Low-to-high propagation delay	A to B	DDC channels enabled		467		ns
		B to A	DDC channels enabled		160		
$t_{FALL}$	Fall time	A port	DDC channels enabled		80		ns
		B port	DCC channels enabled		135		
$t_{RISE}$	Rise time	A port	DCC channels enabled		179		ns
		B port	DCC channels enabled		93		
$f_{MAX}$	Maximum switching frequency		DCC channels enabled	400			kHz
<b>CEC LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	CEC channels enabled		530		ns
		B to A	CEC channels enabled		185		
$t_{PLH}$	Low-to-high propagation delay	A to B	CEC channels enabled		13		$\mu\text{s}$
		B to A	CEC channels enabled		275		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		80		ns
		B port	CEC channels enabled		200		
$t_{RISE}$	Rise time	A port	CEC channels enabled		180		ns
		B port	CEC channels enabled		16		$\mu\text{s}$
<b>HPD LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	B to A	CEC channels enabled		10		ns
$t_{PLH}$	Low-to-high propagation delay	B to A	CEC channels enabled		10		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		0.35		ns
$t_{RISE}$	Rise time	A port	CEC channels enabled		0.35		ns

## 6.11 Switching Characteristics – $V_{CCA} = 3.3\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SCL, SDA LINES (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	DDC channels enabled		370		ns
		B to A	DDC channels enabled		160		
$t_{PLH}$	Low-to-high propagation delay	A to B	DDC channels enabled		460		ns
		B to A	DDC channels enabled		155		
$t_{FALL}$	Fall time	A port	DDC channels enabled		75		ns
		B port	DCC channels enabled		135		
$t_{RISE}$	Rise time	A port	DCC channels enabled		180		ns
		B port	DCC channels enabled		93		
$f_{MAX}$	Maximum switching frequency		DCC channels enabled		400		kHz
<b>CEC LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	A to B	CEC channels enabled		530		ns
		B to A	CEC channels enabled		160		
$t_{PLH}$	Low-to-high propagation delay	A to B	CEC channels enabled		13		$\mu\text{s}$
		B to A	CEC channels enabled		275		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		73		ns
		B port	CEC channels enabled		200		
$t_{RISE}$	Rise time	A port	CEC channels enabled		180		ns
		B port	CEC channels enabled		16		$\mu\text{s}$
<b>HPD LINE (x_A &amp; x_B PORTS)</b>							
$t_{PHL}$	High-to-low propagation delay	B to A	CEC channels enabled		10		ns
$t_{PLH}$	Low-to-high propagation delay	B to A	CEC channels enabled		10		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled		0.34		ns
$t_{RISE}$	Rise time	A port	CEC channels enabled		0.36		ns

### 6.12 Typical Characteristics



Typical Characteristics (continued)

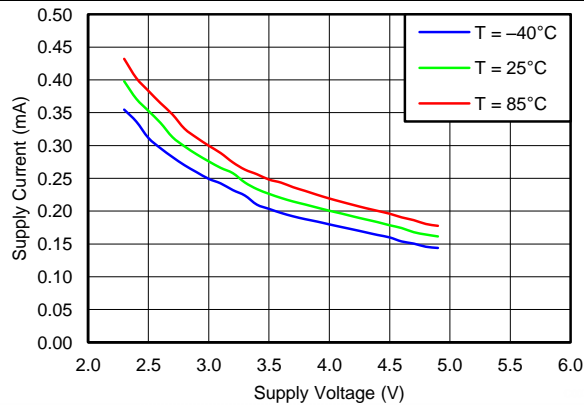


Figure 7. Supply Current vs Supply Voltage

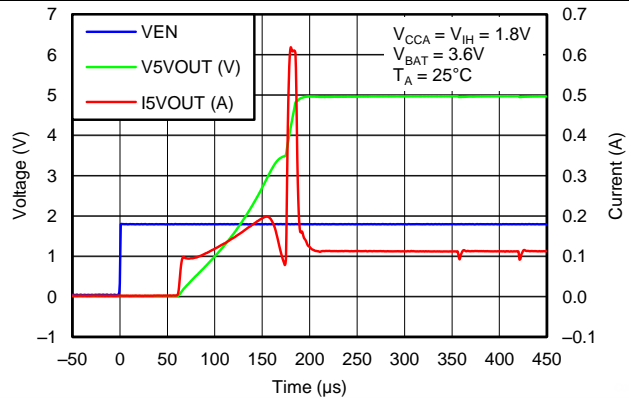


Figure 8. Voltage and Current vs Time

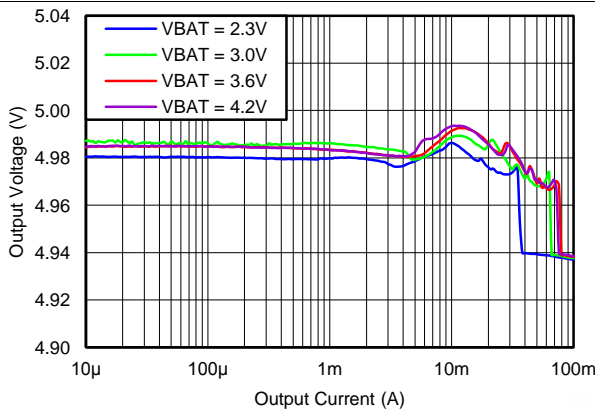


Figure 9. Output Voltage vs Output Current

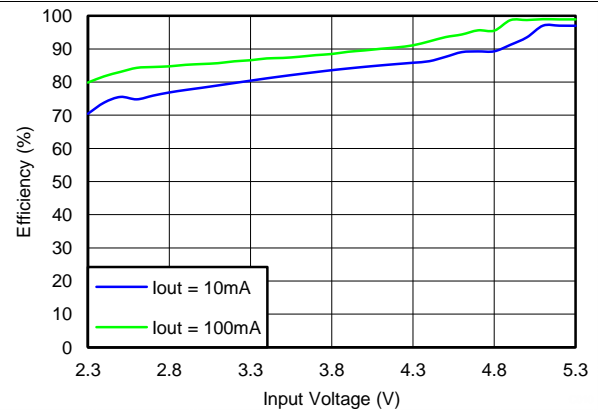


Figure 10. Efficiency vs Input Voltage

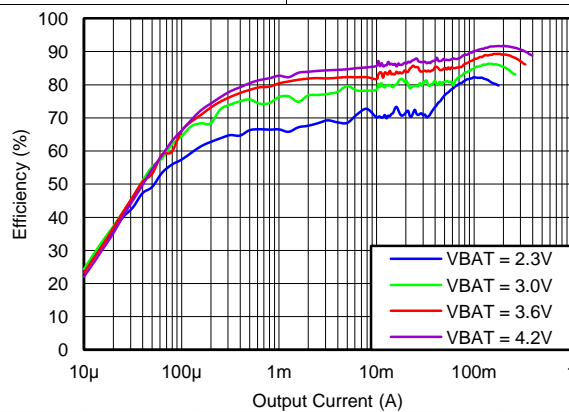


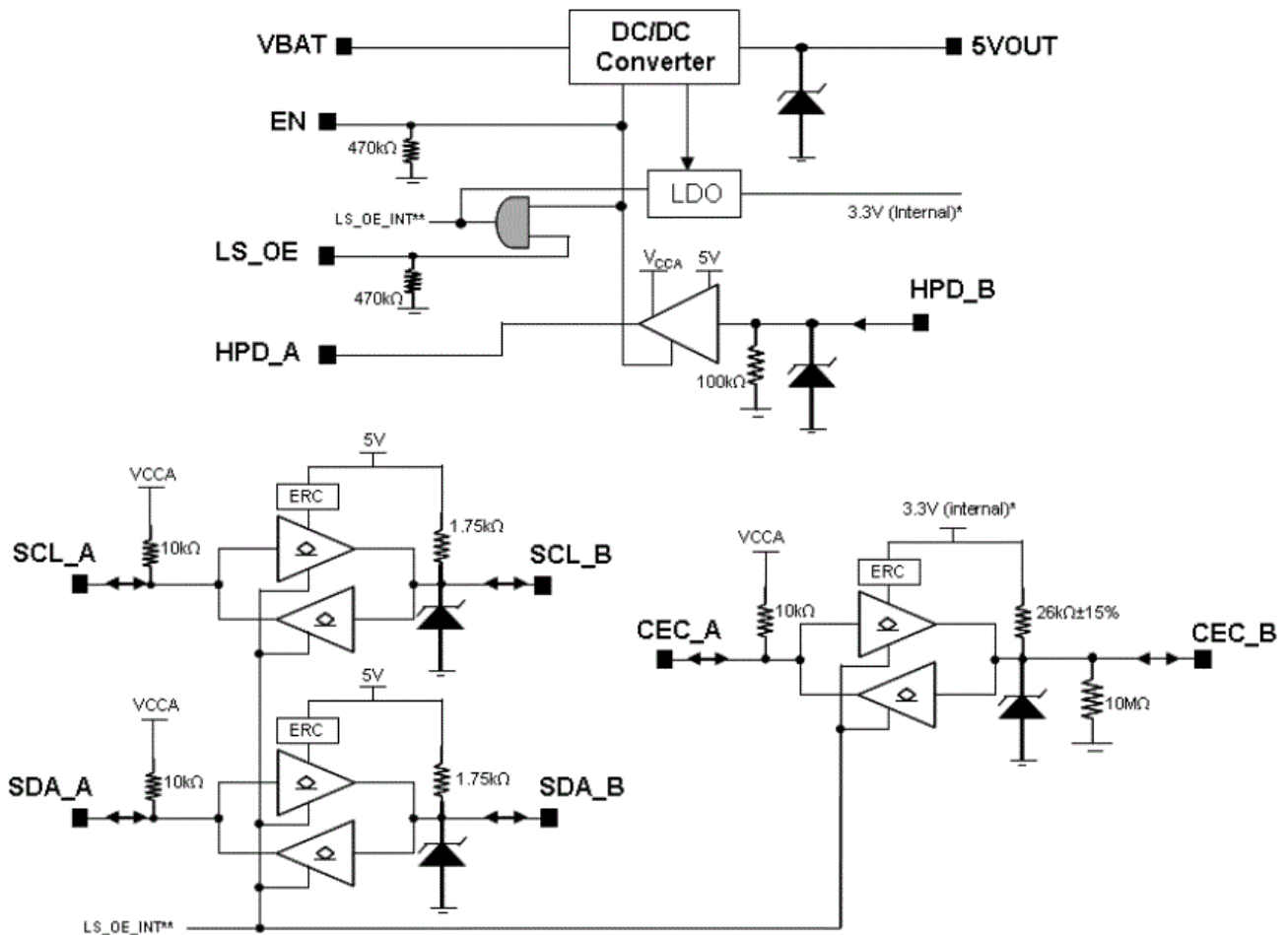
Figure 11. Efficiency vs Output Current

## 7 Detailed Description

### 7.1 Overview

The TPD5S115 is an integrated interface solution that covers HDMI versions' 2.0, 1.4, and 1.3 need for power supply voltage management and control line level translation. On the power supply line, it has a DC-DC converter that takes the internal power supply from 2.3 V to 5.5 V, and outputs a regulated and current-limited, 5-V voltage to the connector. The drivers support level translation on HPD, ECE, SCL, and SDA lines in both transmission directions. Moreover, the rise-time acceleration feature helps drive the high capacitive load on the cable side. Every channel comes with robust ESD protection with  $\pm 14$ -kV contact and  $\pm 16$ -kV air-gap IEC61000-4-2 capability.

### 7.2 Functional Block Diagram



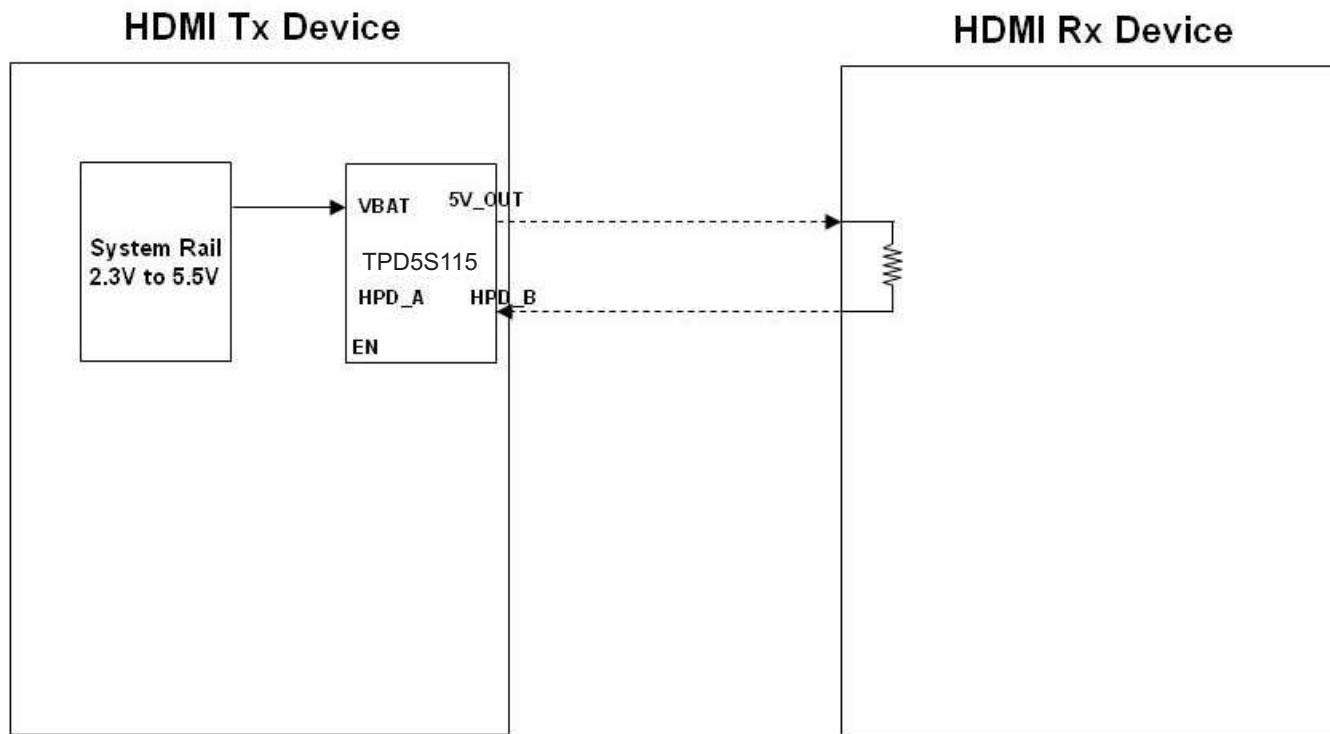
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- (1) 3.3 V (internal) is an internal 3.3-V supply rail which is generated from 5VOUT when EN and LS\_OE are HIGH.
- (2) LS\_OE\_INT is an internal control signal generated from EN and LS\_OE signals. LS\_OE\_INT is active when both EN and LS\_OE are HIGH.

### 7.3 Feature Description

#### 7.3.1 Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high capacitive load on the HDMI cable side. The rise-time accelerator boosts the cable-side DDC signal, independent of which side of the bus is releasing the signal.

**Feature Description (continued)**


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**Figure 12. Receiving and Transmitting Interaction**
**7.3.2 Hot Plug Detect**

After the TPD5S115's DC-DC converter and HPD block are enabled through the EN pin, the TPD5S115 is ready for continual HDMI receiver detection. After a HDMI cable connects a receiving and transmitting device together, the 5-V signal from the DC-DC output flows through the receiving device's internal resistor and into HPD's input. The HPD buffer's output then goes high, indicating to the transmitter that a receiving device is connected. To save power, periodic detection can be done by turning on and off the DC-DC converter before a receiving device is connected.

**NOTE**

Ground offset between the TPD5S115 ground and the ground of devices on port A of the TPD5S115 must be avoided. A CMOS or NMOS open-drain capable of sinking 3 mA of current at 0.4 V has an output resistance of 133  $\Omega$  or less ( $R = E / I$ ). Such a driver shares enough current with the port A output pulldown of the TPD5S115 to be detected as a LOW while the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Because  $V_{ILC}$  can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD5S115 as their output LOW levels are not recognized by the TPD5S115 as a LOW. If the TPD5S115 is placed in an application where the  $V_{IL}$  of port A of the TPD5S115 does not go below its  $V_{ILC}$  it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it does not reproduce the port A input on port B. Such applications must be avoided. Port B is interoperable with all I<sup>2</sup>C-bus slaves, masters, and repeaters.

## Feature Description (continued)

### 7.3.3 CEC Level Shift Operation

The CEC level shift function operates in the same manner as the DDC lines except that the CEC line does not need the rise time accelerator function.

### 7.3.4 Pullup Resistor

The system is designed to work properly with no external pullup resistors on the DDC, CEC, and HPD lines.

### 7.3.5 Undervoltage Lockout

The undervoltage-lockout circuit prevents the DC-DC converter from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling  $V_{IN}$  trips the undervoltage-lockout threshold ( $V_{BATUV}$ ). The undervoltage-lockout threshold for falling  $V_{IN}$  is typically 2 V. The device starts operation once the rising  $V_{IN}$  trips the under-voltage-lockout threshold again at 2.1 V (typical).

### 7.3.6 Soft Start

The DC-DC converter has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage reaches its nominal value within 250  $\mu$ s (typical) after EN has been pulled high. The output voltage ramps up from 5% to its nominal value within 300  $\mu$ s (typical). This limits the in-rush current in the converter during start-up and prevents possible input voltage drops when a battery or high impedance power source is used. During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches  $V_{IN}$ . Once the output voltage trips this threshold, the device operates with its nominal current limit.

## 7.4 Device Functional Modes

### 7.4.1 Power-Save Mode

The TPD5S115 integrates a power-save mode to improve efficiency at light loads. In power-save mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power-save mode once the output voltage exceeds the set threshold voltage. The PFM mode is ended and PWM mode begins in case the output current can no longer be supported in PFM mode.

### 7.4.2 Enable

The DC-DC converter is enabled when the EN is set to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches its nominal value in 250  $\mu$ s (typical) after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can be connected to the output of another converter to drive the EN pin high and create a sequencing of supply rails. When EN = GND, the converter enters shutdown mode.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

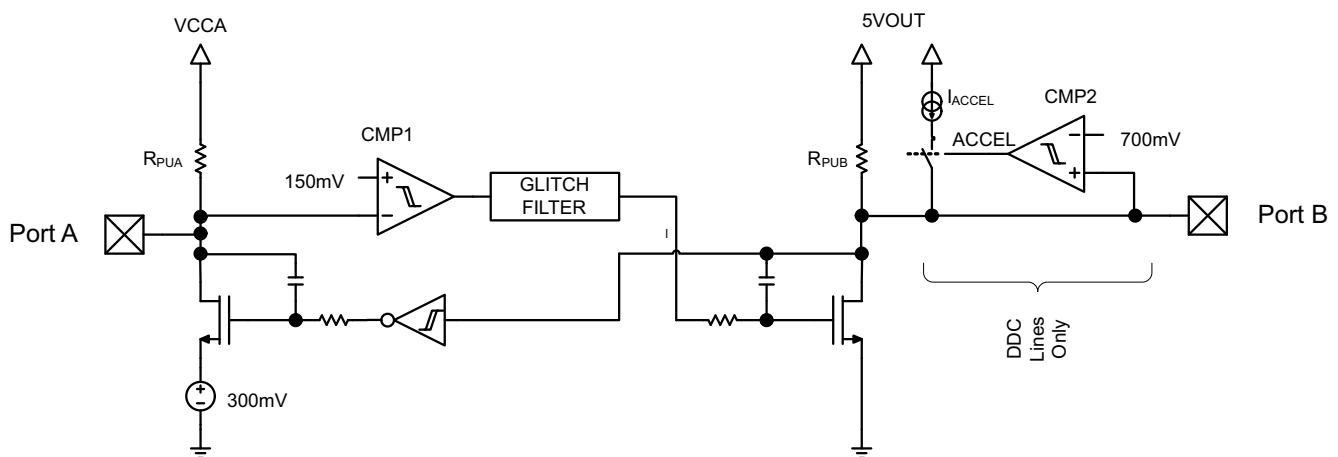
### 8.1 Application Information

The TPD5S115 is an integrated solution for HDMI 2.0, 1.3, and 1.4 interfaces. The device has a boost converter on the power supply, signal conditioning circuits on CEC, SCL, SDA, and HPD lines, and ESD protection on all the connector-facing lines.

### 8.2 Typical Applications

#### 8.2.1 DDC or CEC Level Shifter

The TPD5S115 enables DDC translation from  $V_{CCA}$  (system side) voltage levels to 5-V (HDMI cable side) voltage levels without degradation of system performance. The TPD5S115 contains 2 bidirectional, open-drain buffers specifically designed to support up and down-translation between the low voltage,  $V_{CCA}$  side DDC-bus and the 5-V DDC-bus. The port B I/Os are overvoltage tolerant to 5.5 V, even when the device is shutdown. After power up and with the LS\_OE and EN pins HIGH, a LOW level on port A (below  $V_{ILC} = 0.08 \times V_{CCA}$ ) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to  $V_{OLB}$ . When port A rises above approximately  $0.10 \times V_{CCA}$ , the port B pulldown driver is turned off and the internal pullup resistor pulls the pin HIGH. When port B falls first and goes below  $0.3 \times V_{OUT}$ , a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately  $V_{OLA} = 0.16 \times V_{CCA}$ . The port B pulldown is not enabled unless the port A voltage goes below  $V_{ILC}$ . If the port A low voltage goes below  $V_{ILC}$ , the port B pulldown driver is enabled until port A rises above  $(V_{ILC} + \Delta V_{T-HYSTA})$ , then port B, if not externally driven LOW, continues to rise being pulled up by the internal pullup resistor.



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**Figure 13. DDC or CEC Level Shifter Block Diagram**



## Typical Applications (continued)

### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

**Table 1. Design Parameters**

PARAMETER	VALUE
5VOUT DC current	55 mA
CEC_A, HPD_A, SCL_A, SDA_A voltage level	V <sub>CCA</sub>
HDMI 2.0 data rate per TMDS signal pair	6 Gbps
Required IEC 61000-4-2 ESD Protection	±8-kV contact

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 DDC or CEC Level Shifter Operational Notes for V<sub>CCA</sub> = 1.8 V

- The threshold of CMP1 is approximately 150 mV ± the 40 mV of total hysteresis
- The comparator trips for a falling waveform at approximately 130 mV
- The comparator trips for a rising waveform at approximately 170 mV
- To be recognized as a zero, the level at port A must first go below 130 mV (V<sub>ILC</sub> in spec) and then stay below 170 mV (V<sub>ILA</sub> in spec)
- To be recognized as a one, the level at A must first go above 170 mV and then stay above 130 mV
- V<sub>ILC</sub> is specified as 110 mV in [Electrical Characteristics](#) to give some margin to the 130 mV
- V<sub>ILA</sub> is specified as 140 mV in [Electrical Characteristics](#) to give some margin to the 170 mV
- V<sub>IHA</sub> is specified as 70% of V<sub>CCA</sub> to be consistent with standard CMOS levels

#### 8.2.1.2.2 Input Capacitor

Due to the nature of the boost converter having a pulsating input current, a low-ESR input capacitor is required to prevent large voltage transients that can cause poor performance of the device or interference with other circuits in the system. TI recommends a 1.2-μF (minimum) input capacitor to improve transient behavior of the regulator and EMI behavior of the total power-supply circuit. TI recommends placing a ceramic capacitor (4.7 μF) as close as possible to the V<sub>IN</sub> and GND pins to improve the input noise filtering.

#### 8.2.1.2.3 Output Capacitor

TI recommends using a small ceramic capacitors placed as close as possible to the V<sub>OUT</sub> and GND pins of the IC. If the application requires the use of large capacitors which can not be placed close to the IC, TI recommends using a smaller ceramic capacitor in parallel to the large capacitor. This small capacitor must be placed as close as possible to the V<sub>OUT</sub> and GND pins of the IC. Use [Equation 1](#) to estimate the recommended minimum output capacitance.

$$C_{\min} = \frac{I_{\text{OUT}} \times (V_{\text{OUT}} - V_{\text{IN}})}{f \times \Delta V \times V_{\text{OUT}}}$$

where

- f is the switching frequency
  - ΔV is the maximum allowed ripple
- (1)

If a ripple voltage of 10 mV is chosen, a minimum effective capacitance of 2.7 μF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using [Equation 2](#).

$$\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}}$$
(2)

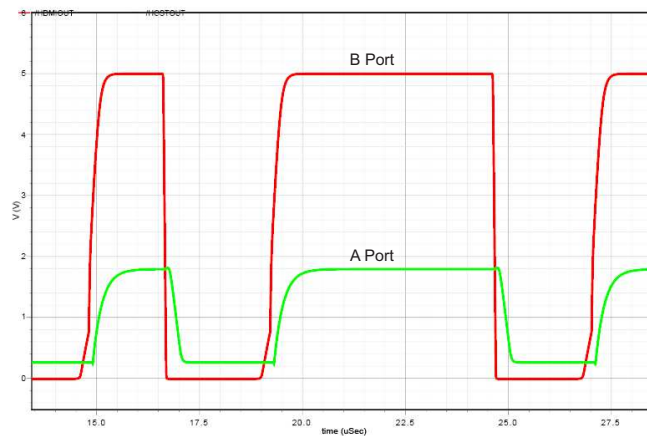
To maintain control loop stability, a capacitor with a value in the range of the calculated minimum must be used. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Ceramic capacitors have a DC-bias effect, which has a strong influence on the final effective capacitance needed. Therefore the appropriate capacitor value must be chosen very carefully. Package size, voltage rating, and material are responsible for differences between the rated capacitor value and the effective capacitance. The minimum effective capacitance value is 1.2  $\mu\text{F}$ , but the recommended value is 4.7  $\mu\text{F}$ .

**Table 2. Passive Components: Recommended Effective Values**

COMPONENT	MIN	TYP	MAX	UNIT
C <sub>IN</sub>	1.2	4.7	6.5	$\mu\text{F}$
C <sub>OUT</sub>	1.2	4.7	10	$\mu\text{F}$
L <sub>IN</sub>	0.7	1	1.3	$\mu\text{H}$
C <sub>VCCA</sub>		0.1		$\mu\text{F}$

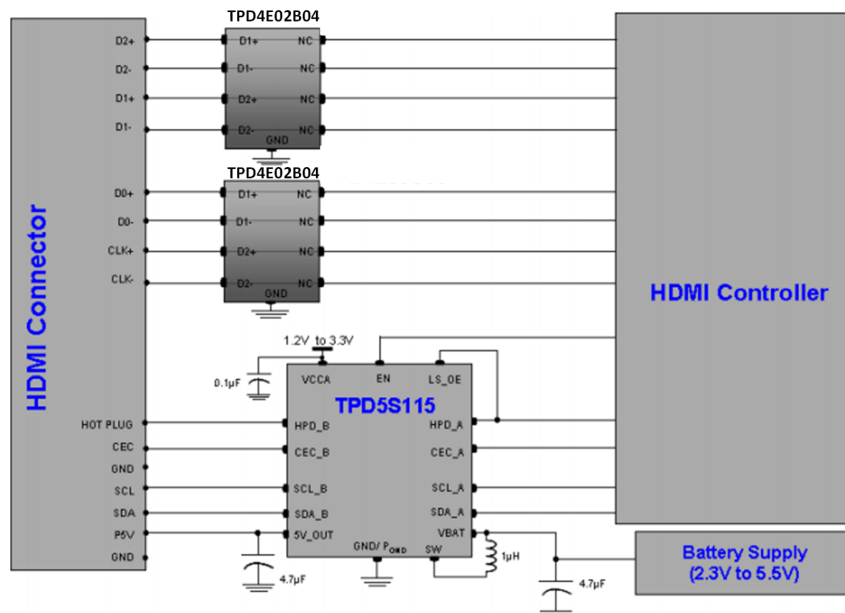
**8.2.1.3 Application Curve**



**Figure 14. DDC Level Shifter Operation (B to A Direction)**

8.2.2 Other Application Circuits

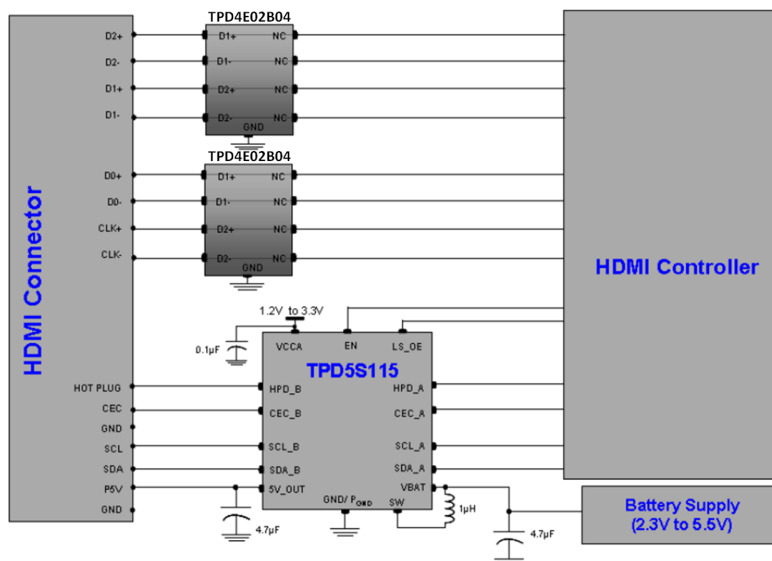
Figure 15 and Figure 16 show application examples using the TPD5S115 devices. Customers must fully validate and test any circuit before implementing a design based on an example in this section. Unless otherwise noted, the design procedures in *DDC or CEC Level Shifter* are applicable.



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Figure 15. Application Schematic for HDMI Controllers With One GPIO for HDMI Interface Control

Some HDMI controllers may have only one GPIO to control the HDMI interface, thus, the HDMI driver chip controls the TPD5S115 through only one control line (EN). In this mode the HPD\_A to LS\_OE pins are connected to each other (see Figure 15).



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Figure 16. Application Schematic for HDMI Controllers With Two GPIOs for HDMI Interface Control

Some HDMI driver chips may have two GPIOs to control the HDMI interface chip. In this case a flexible power saving mode can be implemented. The LS\_OE and EN are active-high enable pins. They control the TPD5S115 power-saving options according to [Table 3](#) and [Table 4](#).

**Table 3. Device Status – Part 1**

LS_OE	EN	V <sub>CCA</sub>	V <sub>BAT</sub>	5VOUT	A-SIDE PULLUPS	DCC, B-SIDE PULLUPS	CEC, B-SIDE PULLUPS
L	L	1.8 V	5 V	Off	Off	Off	Off
L	H	1.8 V	5 V	On	On	On	Off
H	L	1.8 V	5 V	Off	Off	Off	Off
H	H	1.8 V	5 V	On	On	On	On
X	X	0 V	0 V	High-Z	High-Z	High-Z	High-Z
X	X	1.8 V	0 V	Low	Low	High-Z	High-Z
X	X	0 V	5 V	High-Z	High-Z	High-Z	High-Z

**Table 4. Device Status – Part 2**

LS_OE	EN	CEC LDO	DC-DC AND HPD	DDC OR CEC VLTS	I <sub>CCA</sub> TYP	I <sub>CC</sub> V <sub>BAT</sub> TYP	COMMENT
L	L	Off	Off	OFF and High-Z	1 μA	1 μA	Fully disabled
L	H	Off	On	OFF and High-Z	1 μA	30 μA	DC-DC (30 μA) ON
H	L	Off	Off	OFF and High-Z	1 μA	1 μA	Not valid state
H	H	On	On	ON	13 μA	225 μA	Fully ON
X	X	Off	Off	High-Z	0 μA	0 μA	Power down
X	X	Off	Off	High-Z	0 μA	0 μA	Power down
X	X	Off	Off	High-Z	0 μA	0 μA	Power down

## 9 Power Supply Recommendations

To keep the normal function of TPD5S115, the designer needs to make sure that both V<sub>BAT</sub> and V<sub>CCA</sub> are within the recommended operating range. See [Detailed Design Procedure](#) for power supply recommendations.

## 10 Layout

### 10.1 Layout Guidelines

For proper operation, follow these layout and design guidelines:

- Place the TPD5S115 as close to the connector as possible. This allows it to remove the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- Place power line capacitors and inductors close to the pins with wide traces to allow enough current to flow through with less trace parasitics. Ensure that there is enough metallization for the GND pad. A sufficient current path enables safe discharge of all the energy associated with the ESD strike.

### 10.2 Layout Example

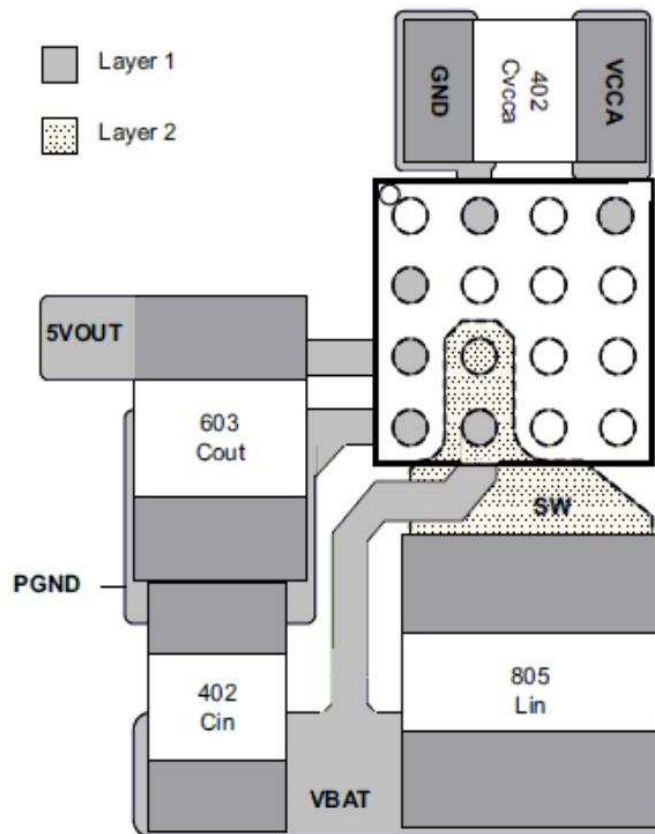


Figure 17. Board Layout With DC-DC Components (Top View)

## 11 器件和文档支持

### 11.1 文档支持

#### 11.1.1 相关文档

请参阅如下相关文档：

- [阅读并了解 ESD 保护数据表](#)
- [《ESD 布局指南》](#)

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。请单击右上角的 [通知我](#) 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

### 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.4 商标

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD5S115YFFR	ACTIVE	DSBGA	YFF	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RE115	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD5S115YFFR	DSBGA	YFF	16	3000	180.0	8.4	1.84	1.84	0.69	4.0	8.0	Q1



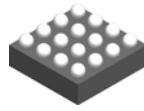
**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD5S115YFFR	DSBGA	YFF	16	3000	182.0	182.0	20.0

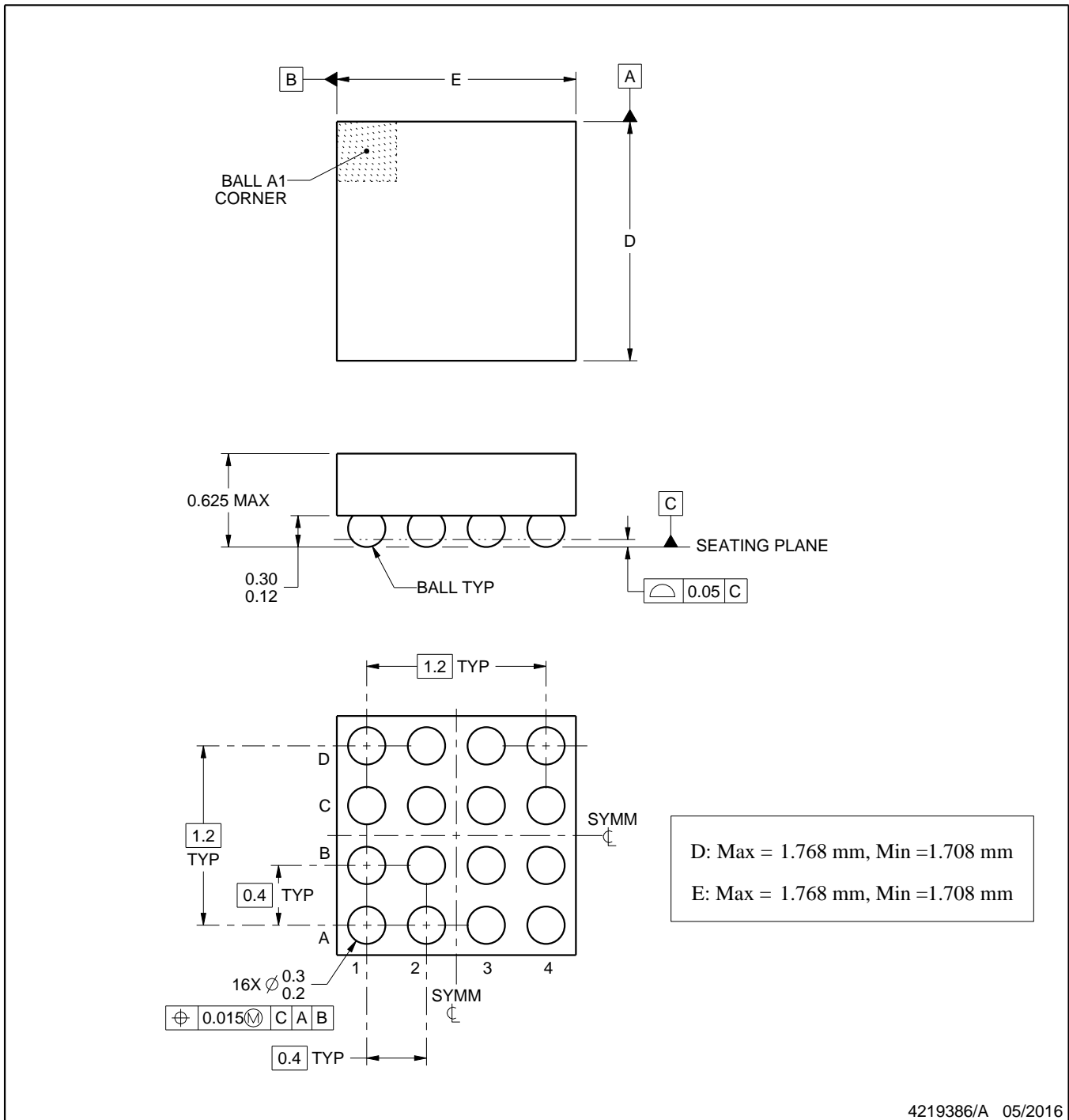
YFF0016



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

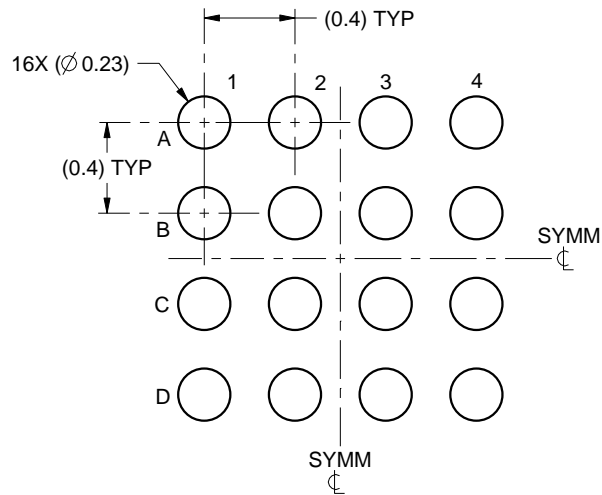
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

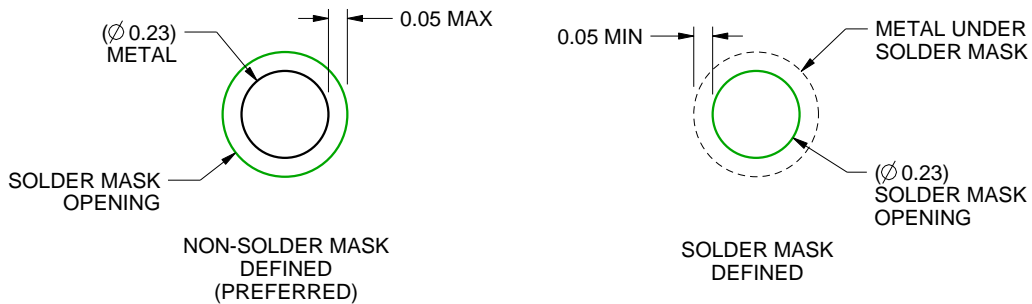
YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

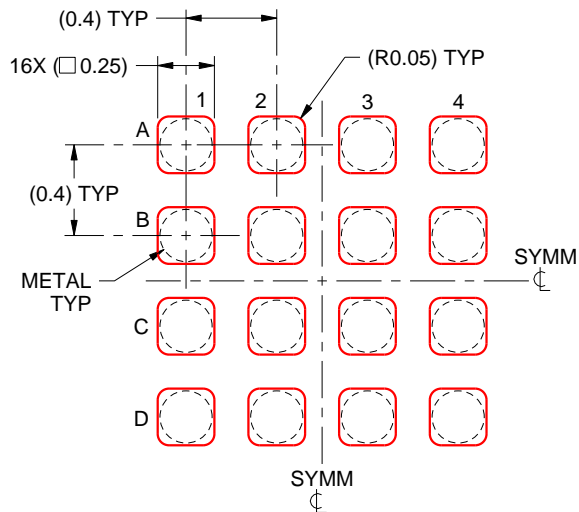
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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