TPIC2050 具有 3 波束激光二极管驱动器、由串行接口控制的 9 通道电机驱动器

1 特性

- 串行端口数字接口
  - 串行外设接口 (SPI)
  - 4 线接口：SSZ、SCLK、SIMO、SOMI
  - 最大读写频率 35MHz
  - 3.3V 数字输入输出 (I/O)
- 执行器和电机驱动器
  - 具有 H 桥输出的脉冲宽度调制 (PWM) 控制
  - 具有 12 位数模转换器 (DAC) 控制的聚焦/跟踪/倾斜执行器驱动器
  - 具有电流模式、10 位 DAC 控制的滑动电机驱动器
  - 具有 12 位 DAC 控制的负载驱动器可选 5V 或 12V
  - 具有 8 位 PWM 控制的步进电机驱动器
- 主轴电机驱动器
  - 0.3Ω 低导通电阻、典型金属氧化物半导体场效应晶体管 (MOSFET) 输出
  - 无传感器：通过电机反电动势 (BEMF) 感测转子位置
  - 适用于 10500rpm 转速（假设使用 12 极点电机）
  - 通过串行端口编程设定的 12 位主轴 DAC
  - 独立的感应位置感测和启动
  - 自动制动功能，在每种转速下均可选择最佳制动模式
  - 最大持续电流为 1.5A，不存在散热问题
- 实用功能
  - 状态锁存器：执行器定时器、SIF 错误、电源监视器、热保护和过流保护 (OCP) 故障
  - 片上温度计（15°C 至 165°C）
- 3 波束激光二极管驱动器
  - 120mA 电流输出，通过 11 位 DAC 寄存器或模拟输入 (VLDDIN)
  - 通过斜率控制电流快速变化
  - 通过串行位选择光盘 (CD)、数字化视频光盘 (DVD)、蓝光光盘 (BD) 的输出端口
- 保护
  - 同步永磁电机 (SPM) 和执行器驱动器上均配有独立热保护电路
  - 两个警报级别：热保护中的预检测和检测
  - ACTTEMP：监视由过去累积的 DAC 值计算得出的执行器温度
  - SPM、滑动电机、负载、执行器和步进驱动器通道中具有短路保护
  - 硬件器件禁用引脚，XRSTIN
  - 具有欠压锁定 (UVLO) 和过压保护 (OVP) 的电源监视器
  - 托盘锁定检测
  - PREOVP-12V：在 SPM 制动时防止通过电机 BEMF 进行 12V OVP 检测

2 应用

光盘驱动器（蓝光碟、DVD、CD）

3 说明

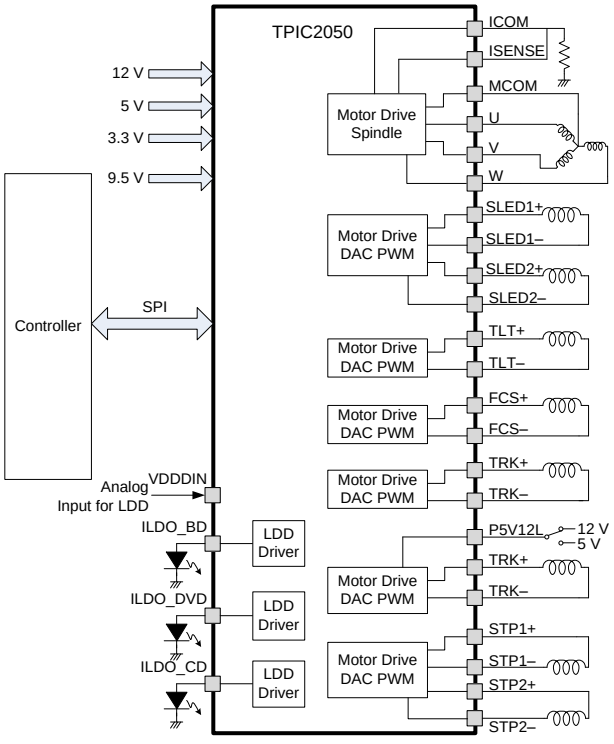
TPIC2050 是一款适用于 12V ODD 的超低噪声电机驱动器集成电路 (IC)。该驱动器 IC 有 9 条通道且由串行接口控制，非常适用于驱动主轴电机、滑动电机（适用的步进电机）、负载电机以及针对准直透镜的聚焦/跟踪/倾斜执行器和步进电机。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPIC2050	HTSSOP (56)	6.10mm x 14.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

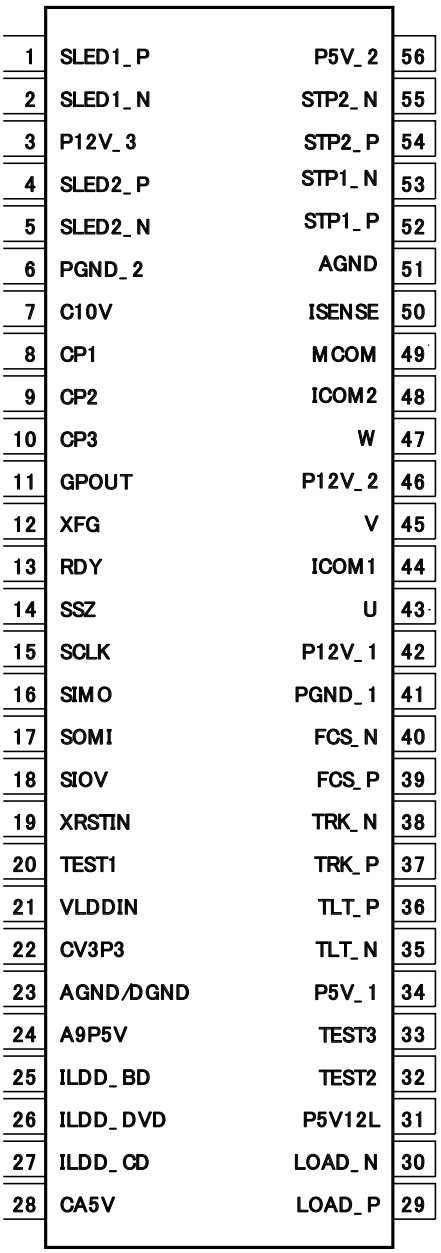
日期	修订版本	注释
2015 年 8 月	*	最初发布。

5 说明 （续）

主轴电机驱动器部分内置无传感器逻辑，可确保以低噪声启动和运行。启动电路可实现自启动或通过 BEMF 执行位置检测，无需使用电机或传感器，例如霍尔器件。由于所有通道的输出级均在高效的 PWM 驱动下工作，因此可通过 PWM 控制实现低功率运行。可以对聚焦/跟踪/倾斜执行器驱动器进行无中性点区域控制。此外，该器件还内置有主轴部件输出电流限制电路、热关断电路、滑动结束位置检测电路、准直透镜结束检测电路、执行器保护和三波束激光驱动器。新增的内置温度计可测量 IC 温度。

6 Pin Configuration and Functions

DFD Package
56-Pin HTSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SLED1_P	1	OUT	Sled1 positive output terminal
SLED1_N	2	OUT	Sled1 negative output terminal
P12V_3	3	PS	Power supply terminal for 12-V drivers output
SLED2_P	4	OUT	Sled2 positive output terminal
SLED2_N	5	OUT	Sled2 negative output terminal
PGND_2	6	PS	GND terminal for 12-V drivers
C10V	7	MISC	Capacitance connection terminal for internal regulator
CP1	8	MISC	Capacitance connection for charge pump
CP2	9	MISC	Capacitance connection for charge pump
CP3	10	MISC	Capacitance connection for charge pump
GPOUT	11	OUT	General-purpose output (test monitor)
XFG	12	OUT	Motor speed signal output
RDY	13	OUT	Device ready signal. Internally pulled up to SIOV
SSZ	14	IN	SIO slave select low active input terminal
SCLK	15	IN	SIO serial clock input terminal
SIMO	16	IN	SIO slave input master output terminal
SOMI	17	OUT	SIO slave output master input terminal
SIOV	18	PS	Power-supply terminal for serial port. 3.3-V typical
XRSTIN	19	IN	RESET input terminal to disable the driver IC
TEST1	20	MISC	Test pin. Should be open
VLDDIN	21	IN	Laser diode control analog signal input 0 to 3-V terminal. Required to set register when using VLDDIN input. Open in case of non-use analog input.
CV3P3	22	MISC	Capacitance terminal for internal 3.3-V core (typical 0.1 μF)
AGND/DGND	23	PS	Ground terminal for internal digital and analog
A9P5V	24	PS	Power-supply terminal 9.5-V laser diode for BD
ILDD_BD	25	OUT	Laser diode for BD output terminal
ILDD_DVD	26	OUT	Laser diode for DVD output terminal
ILDD_CD	27	OUT	Laser diode for CD output terminal
CP5V	28	MISC	Capacitance connection terminal for control system power supply. Connect a ≥0.1-μF decoupling capacitor.
LOAD_P	29	OUT	Load positive output terminal
LOAD_N	30	OUT	Load negative output terminal
P5V12L	31	PS	Power-supply terminal (5 or 12 V) for load driver output stages.
TEST2	32	MISC	Test pin. Should be open
TEST3	33	MISC	Test pin. Should be connected to P5V.
P5V_1	34	PS	Power-supply terminal for tilt/focus/tracking drivers
TLT_N	35	OUT	Tilt negative output terminal
TLT_P	36	OUT	Tilt positive output terminal
TRK_P	37	OUT	Tracking positive output terminal
TRK_N	38	OUT	Tracking negative output terminal
FCS_P	39	OUT	Focus positive output terminal
FCS_N	40	OUT	Focus negative output terminal
PGND_1	41	PS	GND terminal for tilt/focus/tracking channel drivers
P12V_1	42	PS	Power-supply terminal for 12-V driver output stage
U	43	OUT	U-phase output terminal for spindle motor
ICOM1	44	MISC	Current sense resistor terminal for spindle driver
V	45	OUT	V-phase output terminal for spindle motor

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
P12V_2	46	PS	Power-supply terminal for 12-V driver output stage
W	47	OUT	W-phase output terminal for spindle motor
ICOM2	48	MISC	Current sense resistor terminal for spindle driver
MCOM	49	IN	Motor center tap connection
ISENSE	50	IN	Current sense input terminal for spindle drivers
AGND	51	PS	Ground terminal for internal analog
STP1_P	52	OUT	STP1 positive output terminal for collimator
STP1_N	53	OUT	STP1 negative output terminal for collimator
STP2_P	54	OUT	STP2 positive output terminal for collimator
STP2_N	55	OUT	STP2 negative output terminal for collimator
P5V_2	56	PS	Power supply terminal for 5-V driver output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	5-V supply voltage P5V		6	V
	12-V supply voltage P12V		15	
	9.5-V supply voltage A9P5V		15	
	Load supply P5V12 voltage		15	
	Spindle output peak voltage		15	
	Spindle output current		2.5	A
	Spindle output peak current, (PW ≤ 2 ms, Duty ≤ 30%)		3.5	
	Sled output peak current		1.0	
	Focus/tracking/tilt driver output peak current		1.0	
	Load driver output peak current		1.0	
	Laser diode driver output peak current		247(2)	mA
	Input/output voltage	–0.3	V_{CC} + 0.3	V
	Power dissipation(3)		1344	mW
	Operating temperature	–20	75	°C
	Lead temperature 1.6 mm from case for 10 s		260	
T_{stg}	Storage temperature	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The LDD output time of the maximum current should maintain 25% or less of the xsleep total ON time.
(3) A lower $R_{\theta JC}$ is attainable if the exposed pad is connected to a large copper ground plane. $R_{\theta JC}$ and $R_{\theta JA}$ are values for 56-pin TSSOP without a exposed heat slug (HSL) on bottom. Actual thermal resistance would be better than the above values.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
P5V	Operating supply voltage (apply for P5V)	4.5	5.0	5.5	V
P12V	Driver 12-V supply voltage (apply for P12V(1))	10.8	12.0	13.2	
A9P5V	Power supply laser diode for BD (apply for A9P5V)	7.65	9.5	10.45	
P5V12L	Load operating supply voltage (apply for P5V12L)	4.5	5.0	5.5	
		10.8	12.0	13.2	
VSIOV	SIOV voltage	3.0	3.3	36	
T_{ope}	Operating temperature range	–20	25	75	°C
Fck	SCLK frequency	30	33.8688	35	MHz
VSIFH	SIMO, SSZ, SCLK pin 'H' level input voltage range	2.2		SIOV + 0.2	V
VSIFL	SIMO, SSZ, SCLK pin 'L' level input voltage range	–0.2		0.8	
VIHB	XRSTIN pin 'H' level input voltage	2.2		P5V + 0.1	
VILB	XRSTIN pin 'L' level input voltage range	–0.1		0.8	
ISPMOA	Spindle output average current U,V,W Total)		0.5	1.7	A
ISPMO	Spindle output current			1.7	
ISLDOA	Sled output average current		0.25	0.8	
IACTOA	Focus/ tracking/ tilt/ loading output average current		0.5	0.8	
ISTPOA	STP output average current		300		mA

(1) (P5V = 4.5 to 5.5 V, P12V = 10.8 to 13.2 V, CATA ≈ –20℃ to 75℃, unless otherwise noted)

7.4 Thermal Information

THERMAL METRIC(1)		TPIC2050 DFD (HTSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.7	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	0.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PART						
I_{STBY}	Standby supply current	Standby mode		0.6	1.2	mA
V_{CV3}	CV3P3 output voltage	I_{load} = 25 mA	3.1	3.3	3.4	V
R_{XM}	XRSTIN pulldown resistor		100	200	300	kΩ
R_{RDY}	RDY pullup resistor		1.5	33	49.5	
V_{RDY}	RDY low level output voltage	SIOV = 3.3 V, I_{OL} = –100 µA			0.3	V
R_{XFG}	XFG output resistor		100	200	300	Ω
V_{XFGH}	XFG high-level output voltage	SIOV = 3.3 V, XSLEEP = 1, I_{OH} = 100 µA	SIOV – 0.3			V
V_{XFGL}	XFG low-level output voltage	SIOV = 3.3 V, XSLEEP = 1, I_{OL} = 100 µA			0.3	
R_{GPO}	GPOUT output resistor		100	200	300	Ω
V_{GPOH}	GPOUT high-level output voltage	SIOV = 3.3 V, XSLEEP = 1, GPOUT_ENA = 1, GPOUT_HL = 1, I_{OH} = 100 µA	SIOV – 0.3			V
V_{GPOL}	GPOUT low-level output voltage	SIOV = 3.3 V, XSLEEP = 1, GPOUT_ENA = 1, GPOUT_HL = 0, I_{OH} = 100 µA			0.3	
T_{TSD}	Thermal protection on temperature	Design value	135	150	165	°C
TSD_{hys}	Thermal protection hysteresis temperature		5	15	25	
V_{onvcc}	P5V reset on voltage		3.6	3.7	3.8	V
V_{offvcc}	P5V reset off voltage		3.8	3.9	4.0	V
V_{onvcc}	P12V reset on voltage		7.9	8.4	8.9	V
V_{offcc}	P12V reset off voltage		8.3	8.8	9.3	V
V_{onCV3}	CV3P3 reset on voltage		2.6	2.7	2.8	V
V_{offCV3}	CV3P3 reset off voltage		2.7	2.8	2.9	V
$V_{ovpPspmOn}$	OVP predetection voltage (spindle)		13.4	14.1	14.8(1)	V
$V_{ovpPspmOff}$	OVP prerelease voltage (spindle)		13.1	13.8	14.5(1)	V
$V_{ovpspmOn}$	OVP detection voltage (spindle)		14.2	14.9	15.6(1)	V
$V_{ovpspmOff}$	OVP release voltage (spindle)		13.9	14.6	15.3(1)	V
V_{ovpOn}	OVP detection voltage (except spindle)		6.0	6.2	6.4(1)	V
V_{ovpOff}	OVP release voltage (except spindle)		5.8	6.0	6.2(1)	V
CHARGE PUMP PART						
F_{CHGP}	Frequency	XSLEEP = 1	132.6	156	179.4	kHz
V_{CHGP}	Output voltage	Ccp1 = Ccp3 = 0.1 µF Io = –1 mA	15.6	18.5	21.4	V
SPINDLE MOTOR DRIVER PART						
R_{ttlSPM}	Total output resistance high side + low side	I_{OUT} = 500 mA		0.3	0.6	Ω
V_{Isns}	Spindle current limit reference voltage		160	170	180	mV
V_{IsnsP}		For flash peak current detection	179	194	209	
R_{esSPM}	Resolution			12		bit
V_{outSPM}	Spindle gain	Magnification to 1.0 inputs	12.4	14.0	15.6	times

(1) These value are protection functions only, and stress beyond those listed under *Recommended Operating Conditions* may cause permanent damage to the device.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
WidDZSPM	Spindle dead band	Forward	12h	52h	92h	
		Reverse	–92h	–52h	–12h	
SLED MOTOR DRIVER PART						
R_{ttlSLD}	Total output resistance high side + low side	P12V = 10.8 to 13.2 V, IO = 500 mA		1.6	2.5	Ω
ResSLD	Resolution			10		bit
WidDZSLD	Input dead band	Forward	+4h	+33h	+62h	
		Reverse	–62h	–33h	–4h	
G_{nSLD}	Sled current gain	P5V = 5 V, P12V = 12 V VSLED = 7FFh	760	880	1000	mA
$V_{thEdetSLD}$	END_DET BEMF threshold voltage	ENDDET_SLCT = 0, SLEDENDTH<1:0> = ,SLED Enable	62	124	186	mV
FOCUS/TILT/TRACKING DRIVER PART						
R_{ttlAct}	Each channel total output resistance high side + low side	P5V = 4.5 V to 5.5 V, IO = 500 mA		0.7	1.1	Ω
ResACT	Resolution			12		bit
$V_{OfstACT}$	Each channel output offset voltage	DAC_code = 000h	–30	0	30	mV
G_{nAct}	Each channel voltage gain	Magnification to 1.0 inputs	4.7	6.0	7.6	times
LOAD DRIVER PART						
R_{ttlLOD}	Total output resistance high side + low side	P5V12L = 4.5 to 5.5 V, I_O = 500 mA		1.2	1.9	Ω
		P5V12L = 10.8 to 13.2 V, I_O = 500 mA				
ResLOD	Resolution			12		bit
G_{nLOD}	Voltage gain	P5V12L = 4.5 to 5.5 V	4.7	6.0	7.6	V
		P5V12L = 10.8 to 13.2 V	11.1	14.0	17.6	
WidDZLOD	Dead band	Forward		20h		
		Reverse		–21h		

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LockDth	Tray lock detect threshold current	P5V12L = 5 V, TRAY_LOCKDET[2:0] = 1	80	100	120	mA
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 1	80	100	120	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 2	120	150	180	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 2	120	150	180	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 3	160	200	240	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 3	160	200	240	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 4	212	250	287	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 4	212	250	287	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 5	255	300	345	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 5	255	300	345	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 6	297	300	345	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 6	297	300	345	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 7	340	400	460	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 7	340	400	460	
STEPPING MOTOR DRIVER PART						
R_{ttlSTP}	Total output resistance high side + low side	I_O = 100 mA		1.0	1.5	Ω
ResSTP	Resolution			8		bit
I_{ocpSTP}	Overcurrent protection level		595	850	1148 (1)	mA
$t_{DlyocpSTP}$	OCP monitor delay time		0.7	1.0	1.3 (1)	µs
$t_{hlocpSTP}$	OCP hold time		17	25	32 (1)	ms
$V_{thEdetSTP}$	END_DET threshold level	ENDDET_SLCT = 1, STPDENDTH<1:0> = 00, STP Enable	19	39	59	mV
LDD DRIVER PART						
AV (2)	LDD current gain in digital mode VLDD = 0x7FF IUP = 00	LDD_MSEL:01(CD), 10(DVD) A9P5V = 7.65 to 10.45 V	102	120	138	mA
		LDD_MSEL:11(BD) A9P5V = 8.55 to 10.45 V	102	120	138	
		LDD_MSEL:11(BD) A9P5V = 7.65 to 8.55 V	98	120	141	
AV (2)	LDD current gain in analog mode VLDDIN input voltage = 3 V IUP = 00	LDD_MSEL:01(CD), 10(DVD) A9P5V = 7.65 to 10.45 V	102	120	138	mA
		LDD_MSEL:11(BD) A9P5V = 8.55 to 10.45 V	102	120	138	
		LDD_MSEL:11(BD) A9P5V = 7.65 to 8.55 V	98	120	141	

(2) ILDD_BD = 4.5 V, ILDD_CD = 2.1 V ILDD_DVD = 2.1 V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AV(2)(3)	LDD current gain by IUP setting (digital mode only) LDD_MSEL: 01(CD), 10(DVD)	VLDD = 0x7FF, LDD_IUP = 00	102	120	138	mA
		VLDD = 0, LDD_IUP = 00	–10	0	10	
		VLDD = 0x7FF, LDD_IUP = 01	119	149	178	
		VLDD = 0x7FF, LDD_IUP = 10	141	177	212	
		VLDD = 0x7FF, LDD_IUP = 11	164	206	247	
AV(2)(3)	LDD current gain by IUP setting (digital mode only) LDD_MSEL:11(BD) at A9P5V = 8.55 to 10.45 V	VLDD = 0x7FF, LDD_IUP = 00	102	120	138	mA
		VLDD = 0, LDD_IUP = 00	–10	0	10	
		VLDD = 0x7FF, LDD_IUP = 01	119	149	178	
		VLDD = 0x7FF, LDD_IUP = 10	141	177	212	
		VLDD = 0x7FF, LDD_IUP = 011	164	206	247	
AV(2)(3)	LDD current gain by IUP setting (digital mode only) LDD_MSEL:11(BD) at A9P5V = 7.65 to 8.55 V	VLDD = 0x7FF, LDD_IUP = 00	98	120	141	mA
		VLDD = 0, LDD_IUP = 00	–10	0	10	
		VLDD = 0x7FF, LDD_IUP = 01	114	149	183	
		VLDD = 0x7FF, LDD_IUP = 10	136	177	217	
		VLDD = 0x7FF, LDD_IUP = 11	158	206	253	
ResLDD	LDD current gain	P5V = 4.5 V to 5.5 V, A9P5V = 9.5 V		11		bit
t_r	Rise time of ILDD	P5V = 5 V VLDDIN = 0 → 0x7FF 120 mA	162	203	243	µs
t_f	Fall time of ILDD	P5V = 5 V VLDDIN = 0x7FF → 0 50 mA	162	203	243	
I_Z	VLDDIN input impedance		100	200	300	kΩ
LDDdbA	Low voltage dead band		140	200	260	mV
LDDdbA				0x3F		bit
THERMOMETER PART						
ResTEMP	Resolution			6		bit
T_{rng}	Temperature range	CHIPTEMP[5:0] = 00	8	15	22	°C
		CHIPTEMP[5:0] = 3Fh	155	165	175	
F_{TEMP}	Update cycle			10		kHz
ACTUATOR PROTECTION						
$t_{intACTTEMP}$	Update cycle			26		ms
SERIAL PORT VOLTAGE LEVELS						
SOMI	High-level output voltage, V_{OH}	I_{OH} = 1 mA	80% SIOV			V
SOMI	Low-level output voltage, V_{OL}	I_{OL} = 1 mA			20% SIOV	V
SIMO	High-level input voltage, V_{IH}		70% SIOV			V
SIMO	Low-level input voltage, V_{IL}				20% SIOV	V
t_{SIMO}	Input rise/fall time	20% ⇔ 80% SIOV			3.5	ns
t_{SOMI}	Output rise/fall time(4)	Cload = 30 pF, 20% ⇔ 80% SIOV			10	ns
R_{SCLK}	Internal pulldown resistance		100	200	300	kΩ
R_{SSZ}	Internal pullup resistance		100	200	300	kΩ

(3) LDD_IUP settings are only for digital mode.
(4) Specified by design

7.6 Serial I/F Write Timing Requirements

			MIN	NOM	MAX	UNIT
f_{ck}	SCLK clock frequency	SIOV = 3.3 V			35	MHz
t_{ckl}	SCLK low time		11			ns
t_{ckh}	SCLK high time		11			ns
t_{sens}	SSZ setup time		7			ns
t_{senh}	SSZ hold time		7			ns
t_{sl}	SSZ disable high time		11			ns
t_{ds}	SIMO setup time (Write)		7			ns
t_{dh}	SIMO hold time (Write)		7			ns

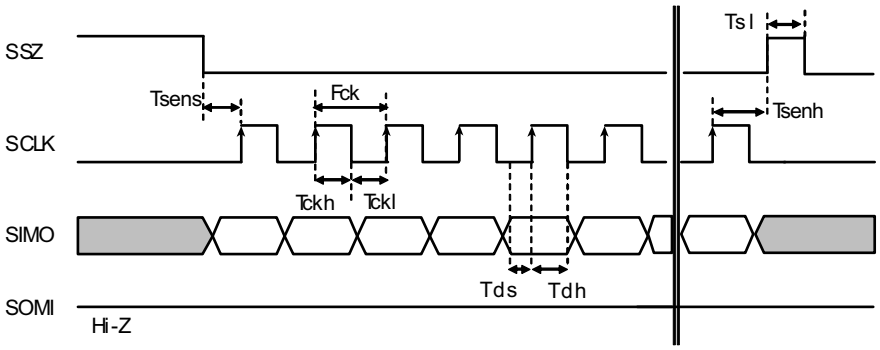


Figure 1. Serial Port Write Timing

7.7 Serial I/F Read Timing Requirements

			MIN	NOM	MAX	UNIT
f_{ck}	SCLK clock frequency	SIOV = 3.3 V			35	MHz
t_{ckl}	SCLK low time		11			ns
t_{ckh}	SCLK high time		11			ns
t_{sens}	SSZ setup time		7			ns
t_{senh}	SSZ hold time		7			ns
t_{sl}	SSZ disable high time		11			ns
t_{ds}	SIMO setup time (Write)		7			ns
t_{dh}	SIMO hold time (Write)		7			ns
t_{rdly}	SOMI delay time (Read)	CLOAD = 10 pF, SIOV = 3.3 V	2		9	ns
t_{sendl}	SOMI hold time (Read)	CLOAD = 10 pF, SIOV = 3.3 V	2		9	ns
t_{rls}	SOMI release time (Read)	CLOAD = 10 pF, SIOV = 3.3 V from SSZ rise to SOMI HIZ	0		9	ns

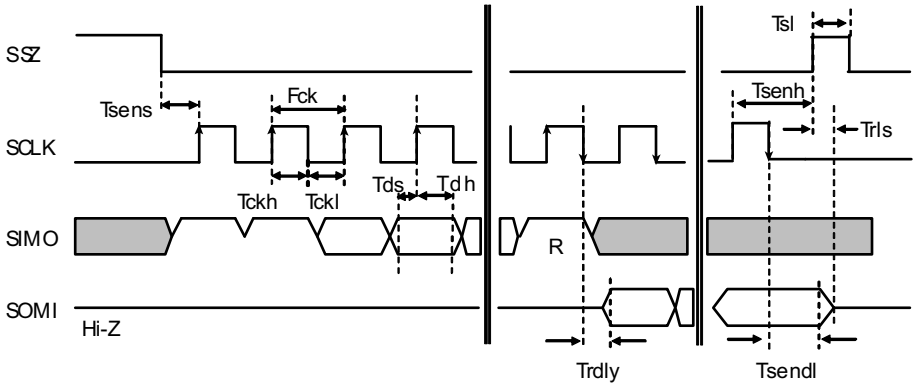


Figure 2. Serial Port Read Timings

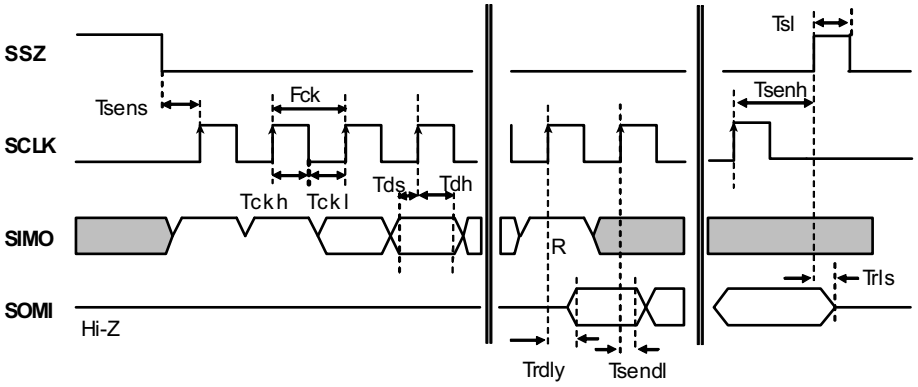


Figure 3. Serial Port Read Timings (Advanced Read Mode)

7.8 Typical Characteristics

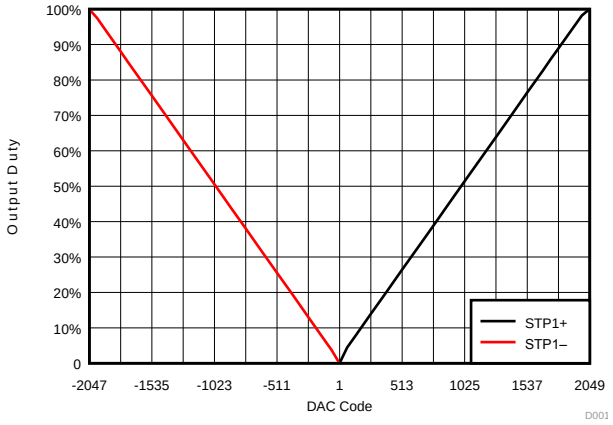


Figure 4. STP1 Driver: DAC Code vs Output On Duty

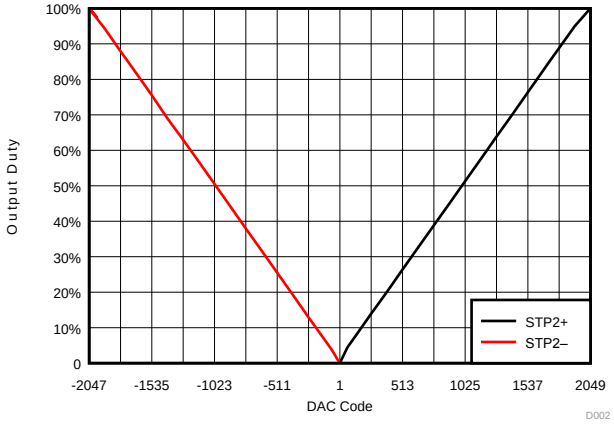


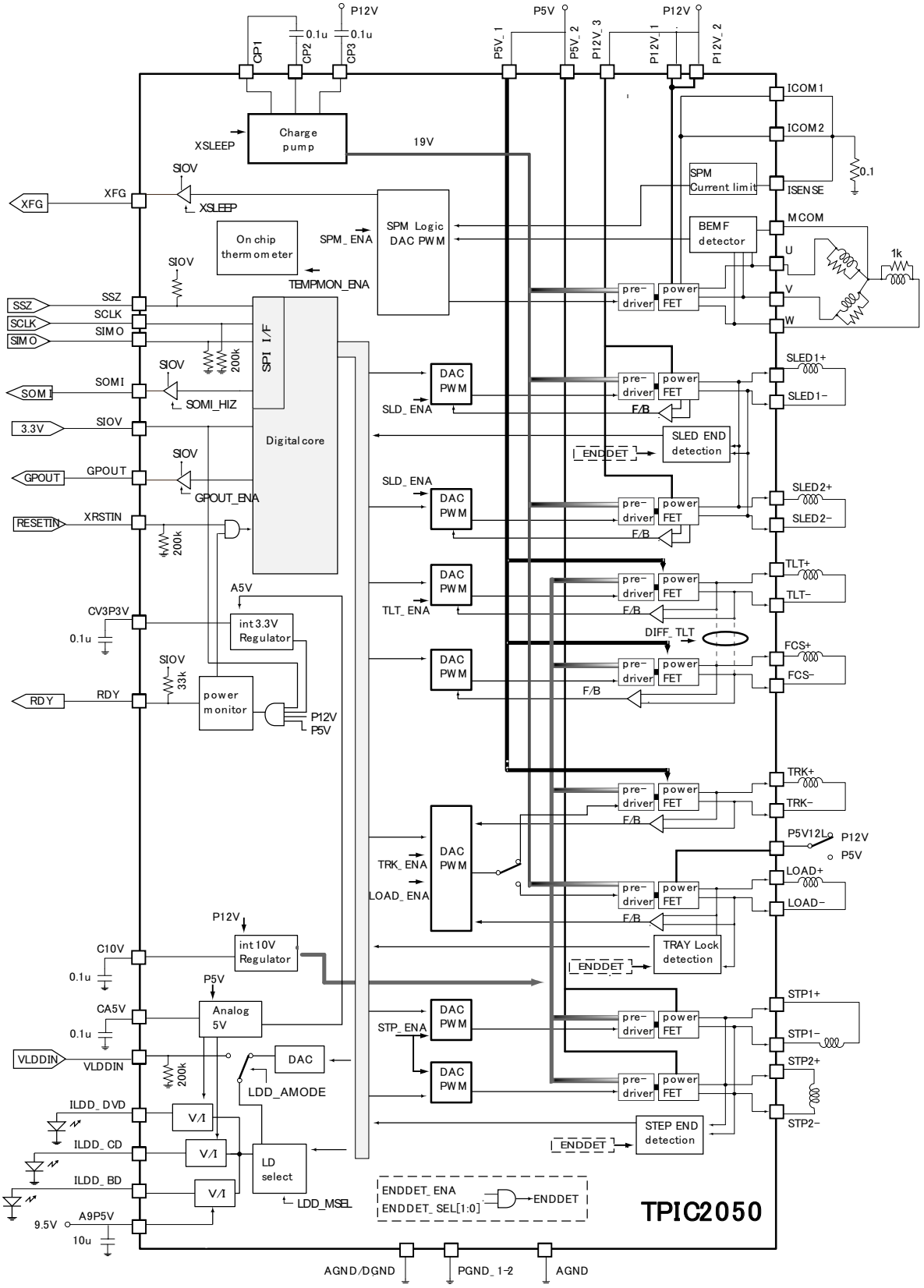
Figure 5. STP2 Driver: DAC Code vs Output On Duty

8 Detailed Description

8.1 Overview

TPIC2050 is very-low noise type motor driver IC suitable for 12V ODD. The 9-channels driver IC controlled by serial I/F is optimum for driving a spindle motor, a sled motor (stepping motor applicable), a load motor, and Focus / Tracking / Tilt actuators and stepping motor for collimator lens. This IC's integrated current sense resistance which measures SPM current then it is able to reduce drive system cost in drastically. The spindle motor driver part builds in the sensor less logic which attained low noise-operation at the time of starting and run. In order to carry out self-starting by the starting circuit and to perform position detection by BEMF of a motor, sensors, such as a Hall device, are not needed. As the output stage of all channels works in efficient PWM driving, it is possible to attain low power operation by PWM control. Dead zone less control is possible for a Focus / Tracking / Tilt actuator driver. In addition, the spindle part output current limiting circuit, the thermal shut down circuit, the sled end detection circuit, collimator lens end detection circuit, actuator protection.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Protect Functions

The TPIC2050 has five protection features to protect target equipment: overvoltage protection (OVP), short-circuit protection (SCP), overcurrent protection (OCP), thermal protection (TSD), and actuator temperature protection (ACTTIMER).

8.3.1.1 OVP

OVP function protects the unit from the supplying high voltage. When the supply voltage exceeds 6.2 V (for P5V), all driver output goes to Hi-Z. The SPM, sled, and load channels go to Hi-Z when P12V is over 14.9 V. When power supply exceeds 14.1 V, the SPM channel enters short brake mode. This operation occurs after a rise in voltage in the motor BEMF. Regardless of the input voltage of the P5V12L, the load channel becomes Hi-Z when OVP_P5V or OVP_P12V. When the supply voltage falls below 6 V, all outputs start to operate again (14.6 V for 12-V driver channel). The OVP and POR (RDY) functions do not interlock. This function is intended to protect the device in the evaluation stage as a temporary and back-up solution.

8.3.1.2 OCP and SCP

The OCP and SCP protect the device from a breakdown caused by a large current. The OCP is provided only for the step channel, and SCP is provided for all driver channels other than the LDD driver. Table 1 indicates each behavior.

Table 1. Protection Threshold Table

BLOCK	FUNCTION	DETECTION CURRENT	DETECT TIME	HI-Z HOLD TIME
STEP driver	OCP	850 mA	1 µs	25 ms
STEP driver (low-side FET only)	SCP	Monitor driver output voltage High-side FET output V = GND Low-side FET output V = Supply V	0.8 to 1.6 µs	1.6 ms
SPM driver				
Sled driver				
Load driver				
Actuator driver				

When a large current is detected on each block, the device puts the output FET to Hi-Z.

When OCP or SCP occurs, it returns automatically after the set Hi-Z hold time expires. The OCPSCPERR (REG7F) and OCP, SCP flags (REG7B) are set at detection.

8.3.1.2.1 OCP for Step Driver

The STP1 and STP2 channels have current trip function. The output of the STEP channel is changed to Hi-Z if the current exceeds the current limit threshold (850 mA typical). When the trip period (25 ms) expires, the trip state is automatically released.

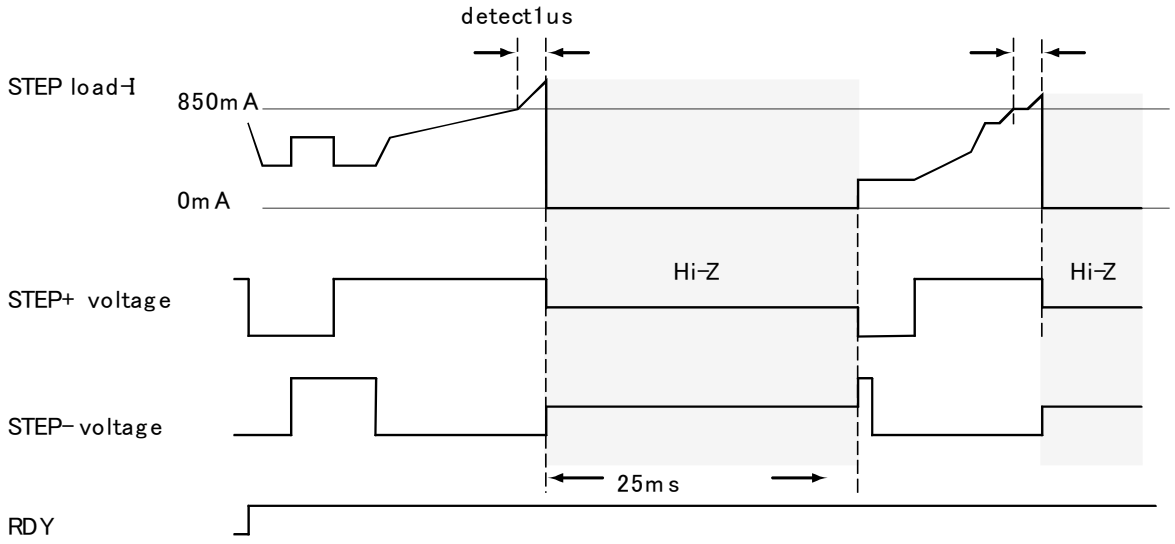


Figure 6. Overcurrent Protection Step

8.3.1.2.2 SCP

The SCP function monitors the output voltage of the high-side and low-side FET of the output driver, and when the setting voltage is not outputted, it recognizes it as 'SCP' and changes the output to Hi-Z. It automatically returns to the original state after 1.6 ms.

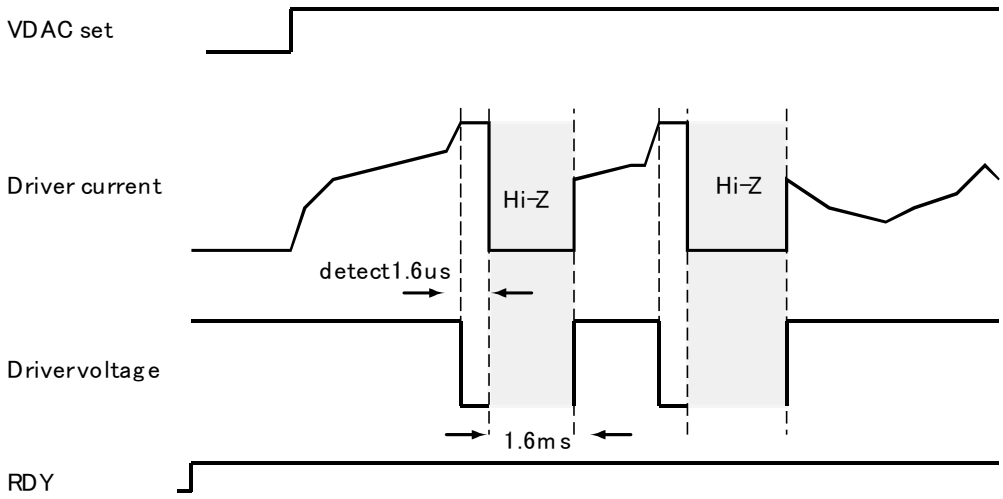


Figure 7. Example of SCP (Driver Short to GND)

8.3.1.3 Thermal Protection (TSD)

The TSD is a protection function which intercepts an output and suspends an operation when the IC temperature exceeds a maximum permissible safe temperature. TSD creates an output Hi-Z when the temperature rises up and a threshold value is exceeded. The two levels for the threshold are alert and trip. An alarm is given by status register TSD_FAULT_ on Alert level at 135°C. If the temperature continues to rise, the register TSD_ is set at 150°C and the driver output changes to Hi-Z. If the temperature falls and reaches 135°C, it outputs again. The TPIC2050 has 11 temperature sensors in each circuit block. The particular sensor assigned to the appropriate status flag is listed in Table 2.

Table 2. Thermal Sensor Assignment

CIRCUIT	ALERT (°C)	TRIP (°C)	RELEASE (°C)	ALERT FLAG	TRIP FLAG
U	135	150	135	TSD_FAULT_SPM	TSD_SPM
V	135	150	135	TSD_FAULT_SPM	TSD_SPM
W	135	150	135	TSD_FAULT_SPM	TSD_SPM
TLT	135	150	135	TSD_FAULT_ACT	TSD_ACT
FCS	135	150	135	TSD_FAULT_ACT	TSD_ACT
TRK	135	150	135	TSD_FAULT_ACT	TSD_ACT
SLED1	135	150	135	TSD_FAULT_ACT	TSD_ACT
SLED2	135	150	135	TSD_FAULT_ACT	TSD_ACT
STP	135	150	135	TSD_FAULT_ACT	TSD_ACT
LOAD	135	150	135	TSD_FAULT_ACT	TSD_ACT
LDD	135	150	135	TSD_FAULT_LDD	TSD_LDD

8.3.1.4 Actuator Temperature Protection (ACTTIMER)

The TPIC2050 has an actuator protect function, ACTTIMER. This function sets the actuator channel output to Hi-Z when the actuator coil current exceeds a specific value. This new protection calculates heat accumulation and judges appropriately. When this function operates, the LDD and load driver channel outputs are Hi-Z, and the spindle channel is forced to auto short brake, stopping the disc motor.

The user can know if protection occurred by checking the Fault register ACTTIMER_FAULT (REG7F) and ACT_TIMER_PROT (REG78). ACTTIMER_FAULT sets a character of advance notice, before detecting ACT_TIMER_PROT. After an ACT_TIMER_PROT is set, even if the temperature falls, it does not automatically release protection. The user must clear the flag by setting the RST_ERR_FLAG (REG77) or setting 0 to ACTTEMPTH (REG72). The ACTTIMER function is disabled by setting H to ACTPROT_OFF (REG72) or setting 0 to ACTTEMPTH (REG72). To acquire the optimal value for ACTTEMPTH, set the device into the condition of the detection level and read the value of ACTTEMP, as the present value can be read from ACTTEMP (REG78). The ACTTEMP data is updated on the register in ACTPROT_OFF = 0 and ACTTEMPTH > 0.

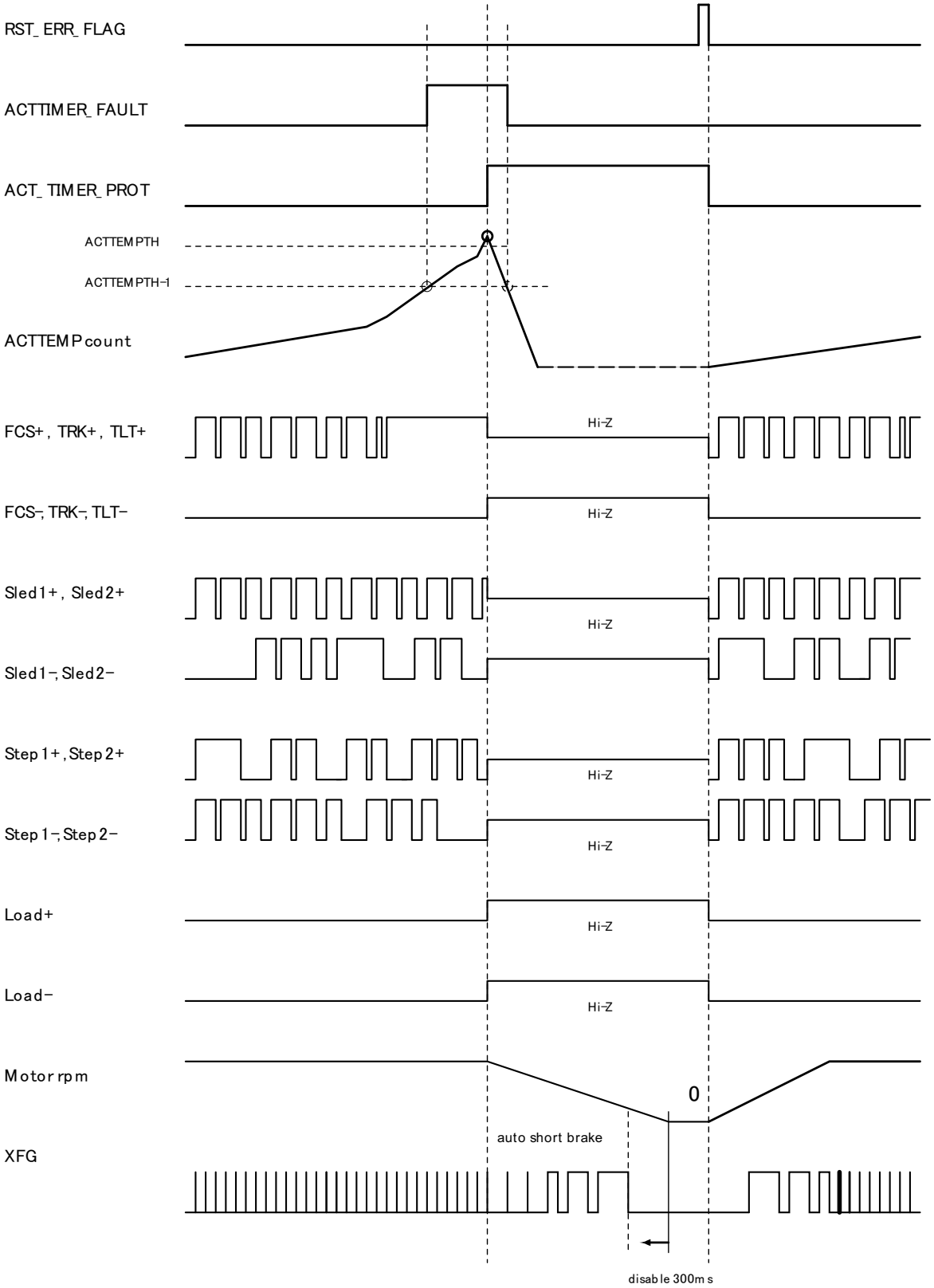


Figure 8. Actuator Temperature Protections

8.3.1.5 Prevent OVP 12 V (PREOVP-12V)

When using the power supply unit without current-sinking capability for 12-V supply, the P12V voltage goes up with the motor BEMF at slowdown. As a result, 12-V OVP is detected if this voltage exceeds the threshold value. To prevent this detection, the TPIC2050 provides a PREOVP-12V function. The SPM driver output is forced into three-phase short brake mode if P12V is over the threshold voltage. The PREOVP-12V function is disabled by OVPPRE12V_OFF = 1 (REG6B[0]).

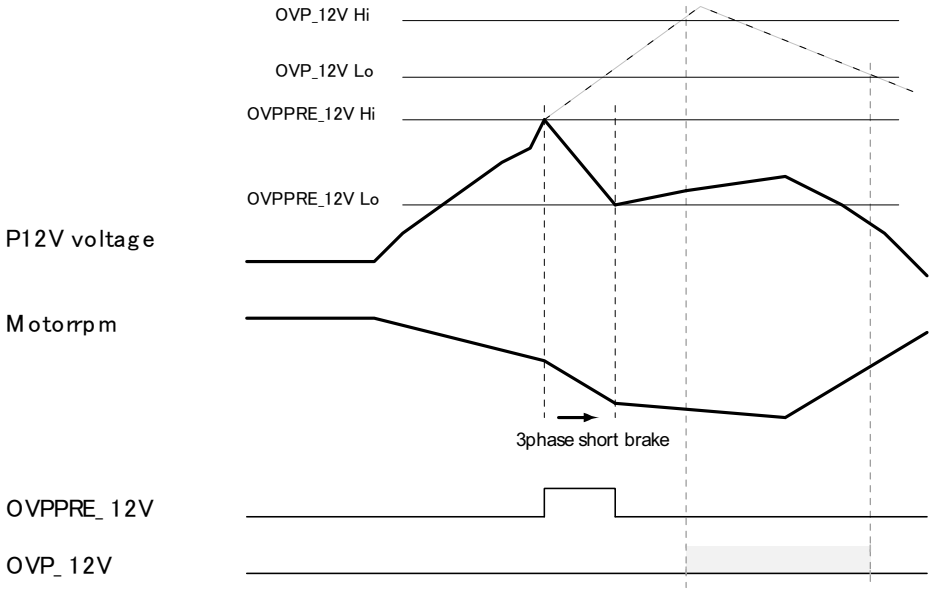


Figure 9. OVPPRE_12V

8.3.2 DAC Type

The TPIC2050 has nine channel drivers and one LDD driver. Each channel is assigned to the most suitable DAC engine with a different type. ACT (focus/tracking/tilt) has a 12-bit DAC. Upper 8 (MSB sign bit) are converted one at a time in 5 MHz, and LSB 4 bits are output in sequence with a 1.25 MHz PWM. SPIN and Load DAC have the same types and sampling rate of 312 kHz. The SPM channel has x14 gain, and other channels (except for SLED and STP) have x6 gain. The DAC for STP is 8-bits resolution output with 40-kHz PWM, and no feedback. The gain for STP is x5 relative to P5V voltage. Table 3 shows the configuration of each driver.

Table 3. DAC Type

	FCS/TRK/TLT	SLED	SPIN	LOAD	STP	LDD
Resolution	12 bit	10 bit	12 bit	12 bit	8 bit	11 bit
Type	8-bit oversampling	10-bit voltage DAC	8-bit over sampling	8-bit over sampling	1-bit direct duty PWM	11-bit voltage DAC
Sampling	1.25M / 10 bit 312K / 12 bit		312K	312K	40 kHz	
PWM frequency	312 kHz	About 156 kHz (variable)	156 kHz	312 kHz	40 kHz	
Out range	±6 V	±880 mA	±14 V	±6 V	±(P5V*1)	0 to 120 mA
Feedback	Voltage F/B	Current F/B	Power supply compensation	Voltage F/B shared with TRK	Direct PWM no F/B	No F/B

8.3.3 Example of 12-Bit DAC Sampling Rate for FCS/TRK/TLT

The input data is separated in the upper 8 bits and the lower 4 bits. Upper 8 bits (MSB sign 1 bit) are put into an 8-bit current DAC in every 5 MHz. The lower 4 bits are put into one bit current DAC in sequence, from the upper to lower bit. This is a one bit DAC output with PWM in 1.25 MHz. At any PWM duty, 100%, 75%, 50%, 25% or 0% is summed in 8-bit current DAC every 1.25 MHz. Therefore, it takes 3.2 µs for all lower 4 bits to sum to the PWM output. As a result, 12-bit data is sampled in every PWM cycle. An example of the sampling rate for FCS/TRK/TLT is in Figure 10.

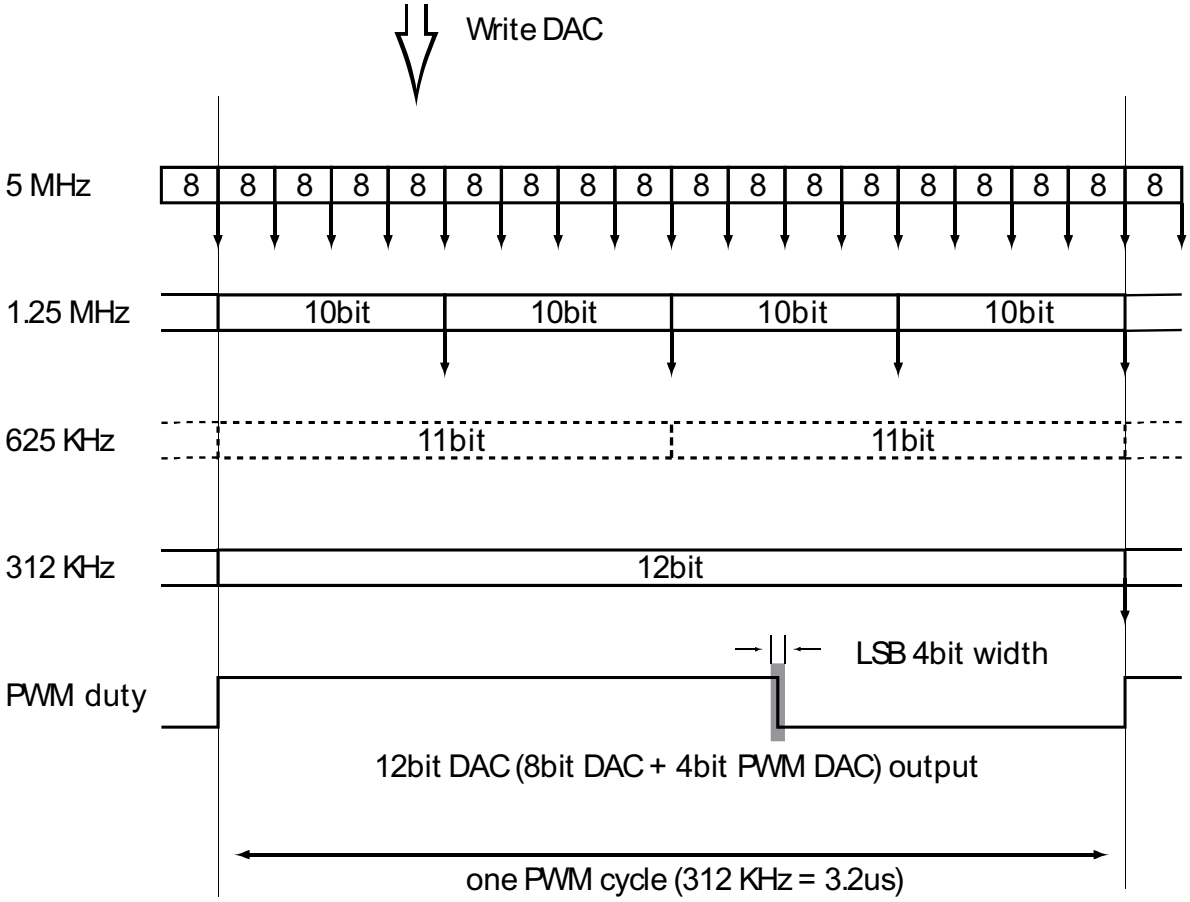


Figure 10. Example of 12-Bit DAC Conversion Time (FCS/TRK/TLT)

8.3.4 Digital Input Coding

The output voltage (current) is commanded via programming to the DAC. All of the DAC input format is 12 bit in complement of 2's, though some DAC has a low resolution. When 12 bits data is inputted as 8-bits DAC, the TPIC2050 recognizes four subordinate position bits (LSB) as 0. To arrange for 12-bit DAC format, the DSP should shift 8-bit or 10-bit data to an appropriate bit position. The full scale is ±1.0 V, and the driver gain is set to 6 or 14. The output voltage (V_{out}) is given by the following equation:

$$Vout = DACcode \times \frac{6.0}{2048}$$

$$VSPMout = DACcode \times \frac{14.0}{2048}$$

Calculation by fixed point number :

$$Vdac = 1.0 \times \left(bit[10] \times 0.5^{1} + bit[9] \times 0.5^{2} + bit[8] \times 0.5^{3} + ... + bit[0] \times 0.5^{11}\right)$$

$$Vdac = (-1.0) \times \left(bit[10] \times 0.5^{1} + bit[9] \times 0.5^{2} + bit[8] \times 0.5^{3} + ... + bit[0] \times 0.5^{11} + 0.5^{12}\right)$$

$$Vout = Vdac \times 6.0 \ (V)$$

$$VSPMout = Vdac \times 14.0 \ (V)$$

$$STPVout = Vdac \times (P5V) \ (V)$$

$$SLEDIout = Vdac \times 0.88 \ (A)$$

where

- bit[11:0] is the digital input value, range 000000000000b to 111111111111b (1)

Table 4. DAC Format

MSB DIGITAL INPUT (BIN) LSB	HEX	DEC	VDAC	ANALOG OUTPUT (5 V)	ANALOG OUTPUT (12 V)
1000_0000_0000	0x800	–2048	–0.9995	–5.997	–13.993
1000_0000_0001	0x801	–2047	–0.9995	–5.997	–13.993
1111_1111_1111	0xFFF	–1	–0.0005	–0.003	–0.007
0000_0000_0000	0x000	0	0	0.000	0.000
0000_0000_0001	0x001	1	0.0005	0.003	0.007
0111_1111_1110	0x7FE	2046	0.9990	5.994	13.986
0111_1111_1111	0x7FF	2047	0.9995	5.997	13.993

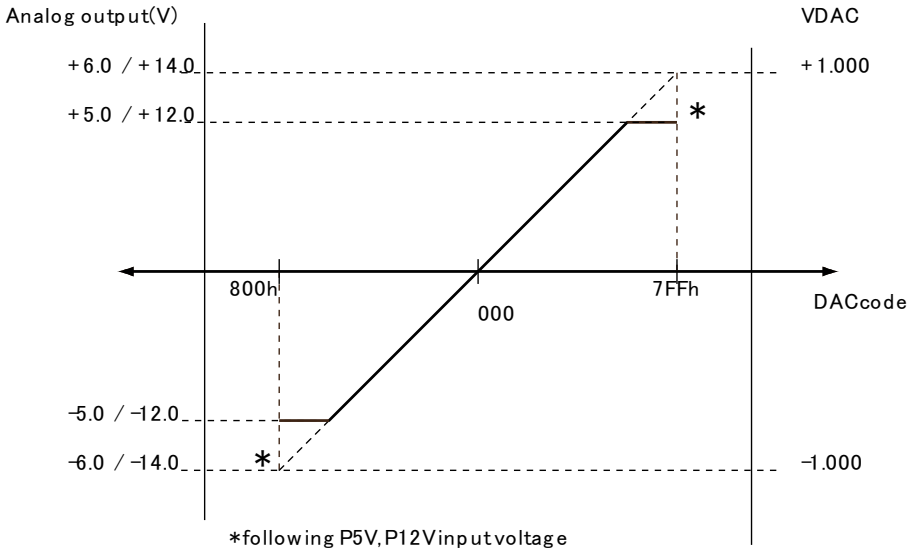


Figure 11. Output Voltage vs DAC Code

8.4 Device Functional Modes

8.4.1 Differential Tilt Mode

The TPIC2050 supports differential tilt mode, which outputs the value calculated from focus and tilt. Focus and tilt can be set in differential mode by DIFF_TLT (REG74) = 1. Because focus and tilt are updated at the same time, the update interval of tilt can be thinned out. Output data changes after writing the VFCS data; therefore, write VFCS data when setting VTLT. In differential mode, the output value is calculated as follows:

FCS_OUT = (VFCS + VTLT) × 6 (2)

TLT_OUT = (VFCS – VTLT) × 6 (3)

8.4.2 Power-On Reset (POR)

8.4.2.1 RDY (Power Ready)

The TPIC2050 prepares the RDY pin to show a power status to the host controller. A device sets RDY output to high (= POR) if the supply voltage and internal regulator voltage reach a rated value. All registers initialize at the time of the POR operation. Figure 12 shows the behavior of RDY.

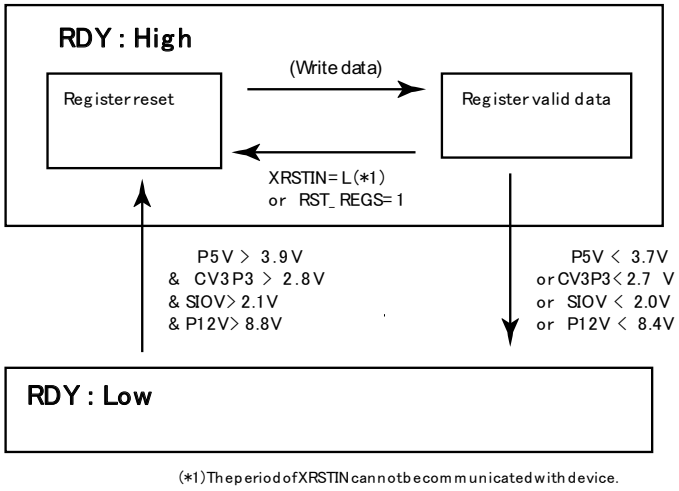


Figure 12. RDY Pin Behavior

8.5 Programming

8.5.1 Serial Port Functional Description

The serial communication of the TPIC2050 is based on an SPI communications protocol. The TPIC2050 is put on the slave side. All 16-bit transmission data is effective in SSZ = L period.

The bit stream sent through SIMO from a master (DSP) is latched to an internal shift register by the rising edge of SCLK. All the data is transmitted in a 16-bit command and data format. A format has two types of data, 8 bits and 12 bits in length. To access specific registers, an address and R/W flag are specified as a command part. In addition, 12-bit data does not have an R/W flag in the packet, because the DAC registers (= 12-bit data form) are Write only. A transfer packet (command and data) is transmitted sequentially from MSB to LSB. A packet is distinguished in MSB by 2 bits of command. In the case of 11, it handles a packet for control register access, and the other is processed as a packet for a DAC data setting.

The four kinds of serial-data communication packets are:

- Write 12 bits DAC data (MSB two bit ≠ 11)
- Write 8 bits control register (MSB two bit = 11)
- Read 8 bits control register (MSB two bit = 11)
- Write 12 bits focus DAC data + Read 8 bits status register at the same time (MSB two bit ≠ 11)

8.5.2 Write Operation

For write operations, the DSP transmits 16-bit (command + address + data) data in order from MSB. Only the 16-bit data, which means 16 SCLK sent from the master during SSZ = L, becomes effective. If more than 17 or less than 15 SCLK pulses are received during the time that SSZ is low, the whole packet is ignored. For all valid write operations, the data of the shift register is latched into its designated internal register at the rising edge of the 16th SCLK. All internal register bits, except indicated otherwise, are reset to their default states upon power-on reset.

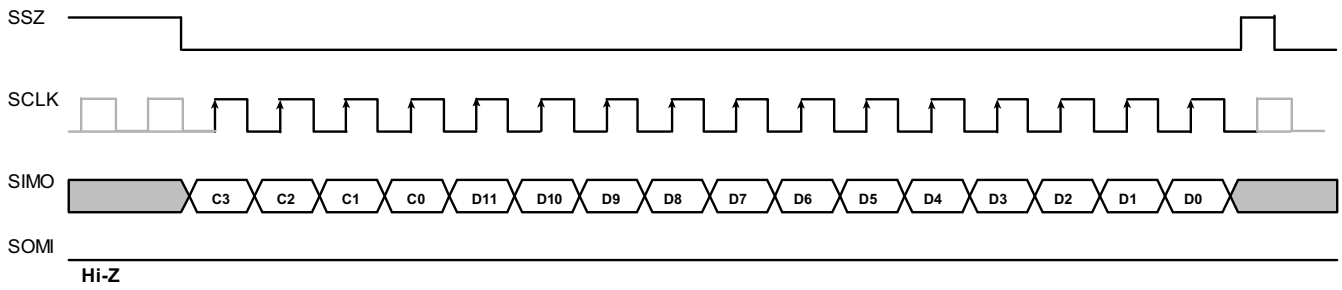


Figure 13. Write 12-Bits DAC Data

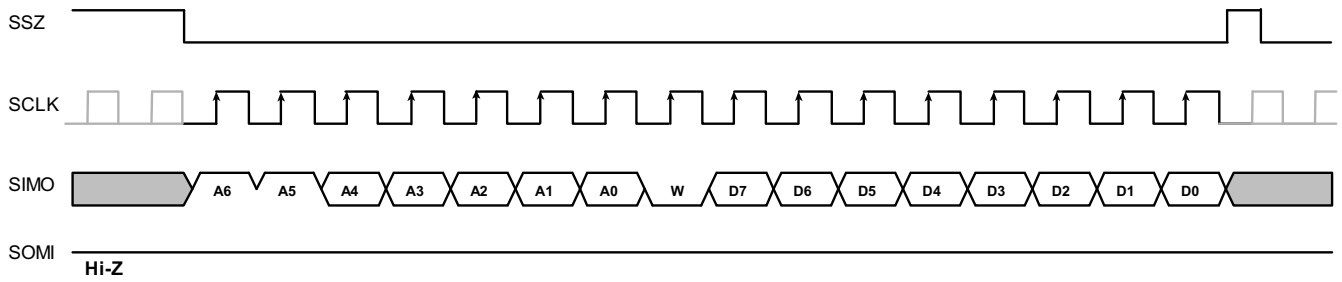


Figure 14. Write 8-Bits Control Register

Programming (continued)

8.5.3 Read Operation

The DSP sends an 8-bit header through SIMO to perform a Read operation. The TPIC2050 starts to drive the SOMI line upon the eighth falling edge of SCLK and shifts out eight data bits. The master DSP inputs 8-bit data from SOMI after the ninth rising edge of SCLK.

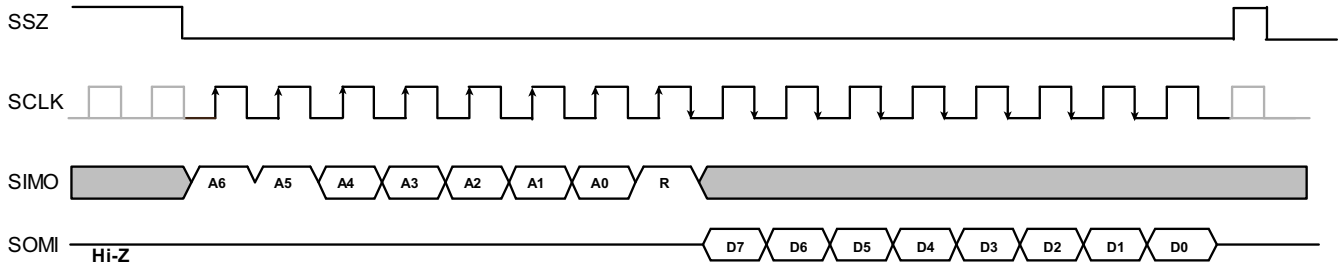


Figure 15. Read 8-Bits Control Register

8.5.4 Write and Read Operation

Optionally, the master DSP can read the Status register while writing the 12 bits DAC (Focus DAC) packet. This is enabled by setting the bit RDSTAT_ON_VFCS (REG74) = H.

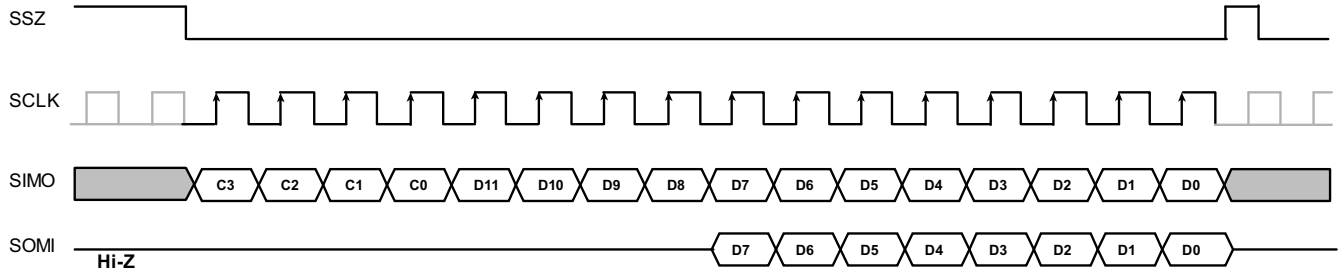


Figure 16. Write 12-Bits Focus DAC Data + Read 8-Bits Status Data

8.6 Register Maps

All registers are in WRITE-protect mode after XRSTIN release. WRITE_ENA bit (REG76) = 1 is required before writing data in the register.

8.6.1 Register State Transition

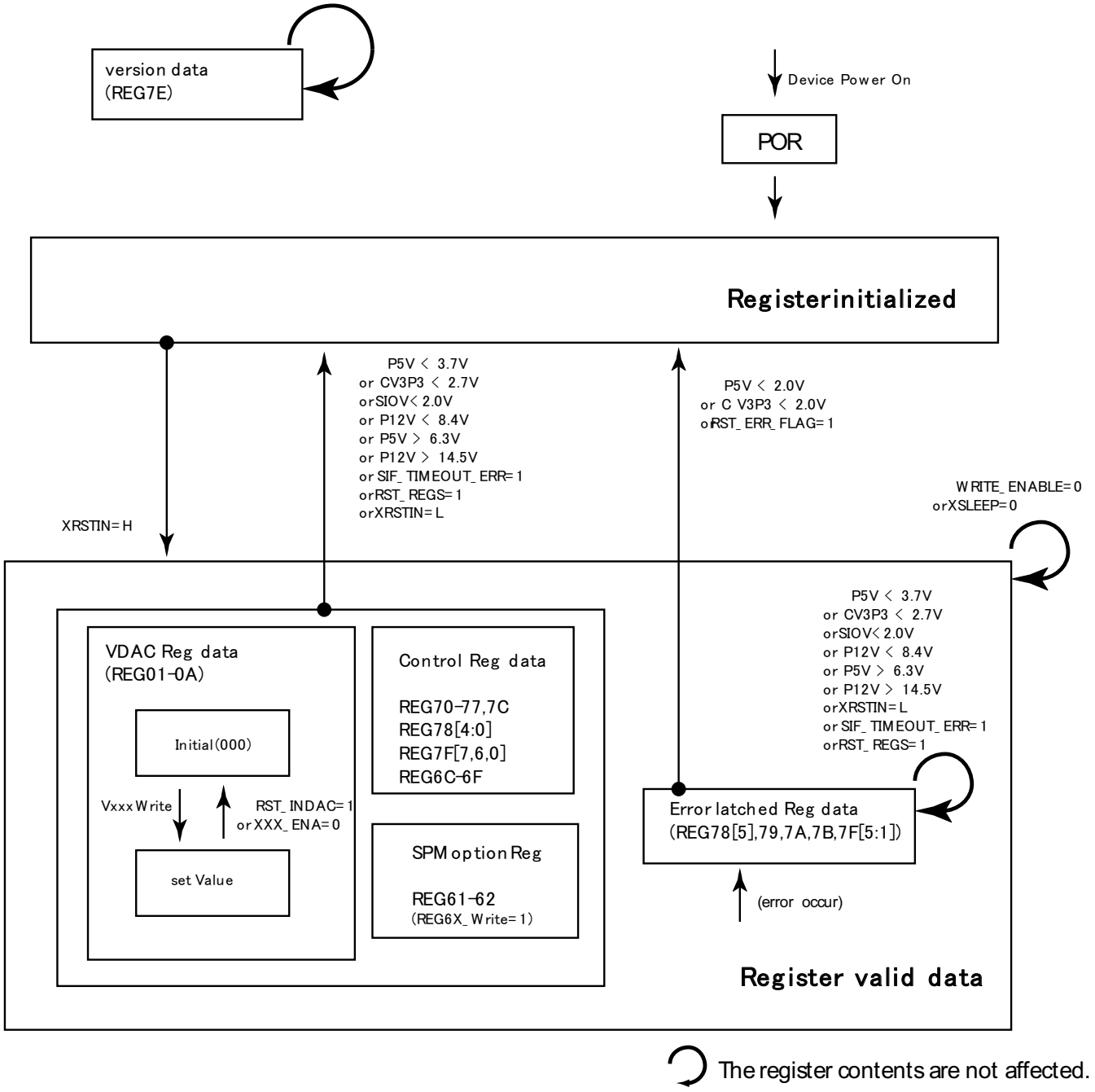


Figure 17. Register Behavior

Register Maps (continued)

8.6.2 DAC Register (12-Bit Write Only)

Two different forms apply to the 12-bit DAC registers. The forms can be selected by setting VDAC_MAPSW (REG74h).

Table 5. DAC Register (VDAC_MAPSW = 0)

Reg	Name	11	10	9	8	7	6	5	4	3	2	1	0
00h	N/A	N/A											
01h	VTLT	VTLT [11]	VTLT [10]	VTLT [9]	VTLT [8]	VTLT [7]	VTLT[6]	VTLT[5]	VTLT[4]	VTLT[3]	VTLT[2]	VTLT[1]	VTLT[0]
02h	VFCS	VFCS [11]	VFCS [10]	VFCS [9]	VFCS [8]	VFCS [7]	VFCS[6]	VFCS[5]	VFCS[4]	VFCS[3]	VFCS[2]	VFCS[1]	VFCS[0]
03h	VTRK	VTRK [11]	VTRK [10]	VTRK [9]	VTRK [8]	VTRK [7]	VTRK[6]	VTRK[5]	VTRK[4]	VTRK[3]	VTRK[2]	VTRK[1]	VTRK[0]
04h	VSLD1	VSLD1 [11]	VSLD1 [10]	VSLD1 [9]	VSLD1 [8]	VSLD1 [7]	VSLD1 [6]	VSLD1 [5]	VSLD1 [4]	VSLD1[3]	VSLD1[2]	VSLD1[1](1)	VSLD1[0](1)
05h	VSLD2	VSLD2 [11]	VSLD2 [10]	VSLD2 [9]	VSLD2 [8]	VSLD2 [7]	VSLD2 [6]	VSLD2 [5]	VSLD2 [4]	VSLD2[3]	VSLD2[2]	VSLD2[1](1)	VSLD2[0](1)
06h	VSTP1	VSTP1 [11]	VSTP1 [10]	VSTP1 [9]	VSTP1 [8]	VSTP1 [7]	VSTP1 [6]	VSTP1 [5]	VSTP1 [4]	VSTP1[3](1)	VSTP1[2](1)	VSTP1[1](1)	VSTP1[0](1)
07h	VSTP2	VSTP2 [11]	VSTP2 [10]	VSTP2 [9]	VSTP2 [8]	VSTP2 [7]	VSTP2 [6]	VSTP2 [5]	VSTP2 [4]	VSTP2[3](1)	VSTP2[2](1)	VSTP2[1](1)	VSTP2[0](1)
08h	VSPM	VSPM [11]	VSPM [10]	VSPM [9]	VSPM [8]	VSPM [7]	VSPM[6]	VSPM[5]	VSPM[4]	VSPM[3]	VSPM[2]	VSPM[1]	VSPM[0]
09h	VLOAD	VLOAD [11]	VLOAD [10]	VLOAD [9]	VLOAD [8]	VLOAD [7]	VLOAD [6]	VLOAD [5]	VLOAD [4]	VLOAD[3]	VLOAD[2]	VLOAD[1]	VLOAD[0]
0Ah	VLDD	VLDD [11]	VLDD [10]	VLDD [9]	VLDD [8]	VLDD [7]	VLDD[6]	VLDD[5]	VLDD[4]	VLDD[3]	VLDD[2]	VLDD[1]	VLDD[0]
0Bh	N/A	N/A											

(1) TPIC2050 processes as 0 even if set to 1

Table 6. DAC Register (VDAC_MAPSW = 1)

Reg	Name	11	10	9	8	7	6	5	4	3	2	1	0
00h	N/A	N/A											
01h	VTRK	VTRK [11]	VTRK [10]	VTRK[9]	VTRK[8]	VTRK[7]	VTRK[6]	VTRK[5]	VTRK[4]	VTRK[3]	VTRK[2]	VTRK[1]	VTRK[0]
02h	VFCS	VFCS [11]	VFCS [10]	VFCS[9]	VFCS[8]	VFCS[7]	VFCS[6]	VFCS[5]	VFCS[4]	VFCS[3]	VFCS[2]	VFCS[1]	VFCS[0]
03h	VTLT	VTLT [11]	VTLT [10]	VTLT[9]	VTLT[8]	VTLT[7]	VTLT[6]	VTLT[5]	VTLT[4]	VTLT[3]	VTLT[2]	VTLT[1]	VTLT[0]
04h	VSLD1	VSLD1 [11]	VSLD1 [10]	VSLD1 [9]	VSLD1 [8]	VSLD1 [7]	VSLD1 [6]	VSLD1 [5]	VSLD1 [4]	VSLD1 [3]	VSLD1 [2]	VSLD1 [1](1)	VSLD1 [0](1)
05h	VSLD2	VSLD2 [11]	VSLD2 [10]	VSLD2 [9]	VSLD2 [8]	VSLD2 [7]	VSLD2 [6]	VSLD2 [5]	VSLD2 [4]	VSLD2 [3]	VSLD2 [2]	VSLD2 [1](1)	VSLD2 [0](1)
06h	VSPM	VSPM [11]	VSPM [10]	VSPM[9]	VSPM[8]	VSPM[7]	VSPM[6]	VSPM[5]	VSPM[4]	VSPM[3]	VSPM[2]	VSPM[1]	VSPM[0]
07h	VLDD	VLDD [11]	VLDD [10]	VLDD[9]	VLDD[8]	VLDD[7]	VLDD[6]	VLDD[5]	VLDD[4]	VLDD[3]	VLDD[2]	VLDD[1]	VLDD[0]
08h	N/A	N/A											
09h	VLOAD	N/A				VLOAD [11]	VLOAD [10]	VLOAD [9]	VLOAD [8]	VLOAD [7]	VLOAD [6]	VLOAD [5]	VLOAD [4]
0Ah	VSTP1	N/A				VSTP1 [11]	VSTP1 [10]	VSTP1 [9]	VSTP1 [8]	VSTP1 [7]	VSTP1 [6]	VSTP1 [5]	VSTP1 [4]
0Bh	VSTP2	N/A				VSTP2 [11]	VSTP2 [10]	VSTP2 [9]	VSTP2 [8]	VSTP2 [7]	VSTP2 [6]	VSTP2 [5]	VSTP2 [4]

(1) TPIC2050 processes as 0 even if set to 1

8.6.3 Control Register (8-Bit Read/Write)

Table 7. Control Register (8-Bit Read/Write)

Reg	Name	F	7	6	5	4	3	2	1	0
70h	DriverEna	R/W	TLT_ENA	FCS_ENA	TRK_ENA	SPM_ENA	SLD_ENA	STP_ENA	LOAD_ENA	XSLEEP
71h	FuncEna	R/W	TI Rsvd	ENDDET_ENA	ENDDET_SEL		LDD_ENA	LDD_MSEL		TEMPMON_ENA
72h	ACTCfg	R/W	P12VMUTE_NORST	RSTIN_OFF	ACTPROT_OFF	ACTTEMPTH				
73h	Parm0	R/W	SIF_TIMEOUT_TH		SLEDEND_HZTIME	SLDENDTH		STPEND_HZTIME	STPENDTH	
74h	SIFCfg	R/W	DIFF_TLT	LDD_AMODE	STATUS_ON_VFCS	VSLD2_POL	VSTP2_POL	ADVANCE_RD	SOMI_HIZ	VDAC_MAPSW
75h	Parm1	R/W	TRAY_LOCKDET			TI Reserved		SPM_FAST_BRK	SPM_SLNT_BRK	SPM_HIZMODE
76h	WriteEna	R/W	WRITE_ENABLE	TI Reserved						REG6X_Write
77h	ClrReg	W	RST_INDAC	RST_REGS	RST_ERR_FLAG	TI Reserved				
78h	ActTemp	R	TI Reserved		ACT_TIMER_PROT	ACTTEMP				
79h	UVLOMon	R	TI Reserved		UVLO_P5V	UVLO_INT3P3	UVLO_P12V	UVLO_SIOV	OVP_P5V	OVP_P12V
7Ah	TSDMon	R	TI Rsvd	TSD_FAULT_SPM	TSD_FAULT_ACT	TSD_FAULT_LDD	TI Rsvd	TSD_SPM	TSD_ACT	TSD_LDD
7Bh	OCPMon	R	TI Reserved		OCP_STP	SCP_SPM	SCP_SLED	SCP_LOAD	SCP_ACT	SCP_STP
7Ch	TempMon	R	CHIPTEMP_STATUS	CHIPTEMP						
7Dh	Protect	R	TI Reserved							
7Eh	Version	R	Version							
7Fh	Status	R	ACTTIMER_FAULT	ENDDET	SIF_TIMEOUTERR	PWRERR	TSDERR	OCPSCPERR	TSDFAULT	FG
60h	Protect	R/W	TI Reserved							
61h	SPM1	R/W	PWMmaxDuty_R_SEL1	TI Rsvd	OVP_SBRAKE_OFF	TI Reserved		SBRAKE_ON	TI Reserved	
62h	SPM2	R/W	TI Reserved							PWMmaxDuty_R_SEL0
63h	Protect	R/W	TI Reserved							
64h	Protect	R/W	TI Reserved							
65h	Protect	R/W	TI Reserved							
66h	Protect	R/W	TI Reserved							
67h	Protect	R/W	TI Reserved							
68h	Protect	R/W	TI Reserved							
6Bh	DisProt	R/W	SCP_SPM_OFF	SCP_SLED_OFF	SCP_LOAD_OFF	SCP_ACT_OFF	SCP_STP_OFF	OCP_STP_OFF	TI Rsvd	OVPPRE12V_OFF
6Ch	STPCfg	R/W	TI Reserved			LDD_IUP		TI Rsvd	STP_WIND_HIZ	STP_WIND_H
6Dh	Protect	R/W	TI Reserved							
6Eh	UtilCfg	R/W	GPOUT_HL	GPOUT_ENA	TI Reserved					
6Fh	MonitorSet	R/W	ACTTIMER_FLT_MON	ENDDET_MON	SIF_TIMEOUTERR_MON	PWRERR_MON	TSDERR_MON	OCPERR_MON	TSDFAULT_MON	TI Rsvd

VTRK and VLOAD are exclusive, using same DAC circuit block.

8.6.4 Detailed Description of Registers

8.6.4.1 REG01 12-Bit DAC for Tilt (offset = 01h) [reset =]

(VDAC_MAPSW = 0)

Figure 18. REG01 12-Bit DAC for Tilt

				11	10	9	8
				VTLT			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VTLT							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. REG01 12-Bit DAC for Tilt Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VTLT	W	0h	Digital input code for tilt 2's complement format 0x800(-2048) to 0x7ff(+2047) Output is changed by differential tilt mode (REG74[7]) TLT_OUT = VTLT × (6.0 / 2048) (DIFF_TLT = 0) TLT_OUT = (VFCS – VTLT) × (6.0 / 2048) (DIFF_TLT = 1) TLT_OUT should be changed after writing VFCS. In DIFF_TLT mode (DIFF_TLT = 1), TLT_OUT should be changed after writing VFCS.

8.6.4.2 REG02 12-Bit DAC for Focus (offset = 02h) [reset =]

(VDAC_MAPSW=0)

Figure 19. REG02 12-Bit DAC for Focus

				11	10	9	8
				VFCS			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VFCS							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. REG02 12-Bit DAC for Focus Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VFCS	W	0h	Digital input code for focus 2's complement format 0x800(-2048) to 0x7ff(+2047) Output is changed by differential tilt mode (REG74[7]) FCS_OUT = VFCS × (6.0 / 2048) (DIFF_TLT = 0) FCS_OUT = (VFCS + VTLT) × (6.0 / 2048) (DIFF_TLT = 1)

8.6.4.3 REG03 12-Bit DAC for Tracking (offset = 03h) [reset =]

(VDAC_MAPSW=0)

Figure 20. REG03 12-Bit DAC for Tracking

				11	10	9	8
				VTRK			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VTRK							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. REG03 12-Bit DAC for Tracking Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VTRK	W	0h	Digital input code for tracking 2's complement format 0x800(-2048) to 0x7ff(+2047) TRK_OUT = VTRK × (6.0 / 2048)

8.6.4.4 REG04 12-Bit DAC for Sled1 (offset = 04h) [reset =]

(VDAC_MAPSW=0)

Figure 21. REG04 12-Bit DAC for Sled1

				11	10	9	8
				VSLD1			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSLD1							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. REG04 12-Bit DAC for Sled1 Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VSLD1	W	0h	Digital input code for Sled1. 2's complement format 0x800(-2048) to 0x7ff(+2047) Two bits on LSB, VSLD1[1:0], handled with zero. SLD1_OUT = VSLD1 × (880 mA / 2048)

8.6.4.5 REG05 12-Bit DAC for Sled2 (offset = 05h) [reset =]

(VDAC_MAPSW=0)

Figure 22. REG05 12-Bit DAC for Sled2

				11	10	9	8
				VSLD2			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSLD2							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. REG05 12-Bit DAC for Sled2 Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VSLD2	W	0h	Digital input code for Sled2. 2's complement format 0x800(-2048) to 0x7ff(+2047) Two bits on LSB, VSLD2[1:0], are handled with zero. SLD2_OUT = VSLD2 × (880 mA/2048)

8.6.4.6 REG06 12-Bit DAC for Stepping1 (offset = 06h) [reset =]

(VDAC_MAPSW = 0)

Figure 23. REG06 12-Bit DAC for Stepping1

				11	10	9	8
				VSTP1			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSTP1							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. REG06 12-Bit DAC for Stepping1 Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VSTP1	W	0h	Digital input code for Stepping1 2's complement format 0x800(-2048) to 0x7ff(+2047) Although VSTP1 is 12-bit width, MSB 8 bits is effective. Four bits on LSB, VSTP1[3:0], are handled with zero. VSTP1_OUT = VSTP1 × (P5V / 2048)

8.6.4.7 REG07 12-Bit DAC for Stepping2 (offset = 07h) [reset =]

(VDAC_MAPSW=0)

Figure 24. REG07 12-Bit DAC for Stepping2

				11	10	9	8
				VSTP2			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSTP2							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. REG07 12-Bit DAC for Stepping2 Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VSTP2	W	0h	Digital input code for Stepping2 2's complement format 0x800(-2048) to 0x7ff(+2047) Although VSTP2 is 12-bit width, MSB 8 bits is effective. Four bits on LSB, VSTP2[3:0], are handled with zero. VSTP2_OUT = VSTP2 × (P5V / 2048)

8.6.4.8 REG08 12-Bit DAC for Spindle (offset = 08h) [reset =]

(VDAC_MAPSW = 0)

Figure 25. REG08 12-Bit DAC for Spindle

				11	10	9	8
				VSPM			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSPM							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. REG08 12-Bit DAC for Spindle Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VSPM	W	0h	Digital input code for Spindle 2's complement format 0x800(-2048) to 0x7ff(+2047) SPM_OUT = VSPM × (14.0 / 2048)

8.6.4.9 REG09 12-Bit DAC for Load (offset = 09h) [reset =]

(VDAC_MAPSW = 0)

Figure 26. REG09 12-Bit DAC for Load

				11	10	9	8
				VLOAD			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VLOAD							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. REG09 12-Bit DAC for Load Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VLOAD	W	0h	Digital input code for Load. 2's complement format 0x800(-2048) to 0x7ff(+2047) LOAD_OUT = VLOAD × (6.0 / 2048) at P5V12L = 5.0 V LOAD_OUT = VLOAD × (14.0/2048) at P5V12L = 12.0 V

8.6.4.10 REG0A 12-Bit DAC for Laser Diode Driver (offset = 0Ah) [reset =]

(VDAC_MAPSW = 0)

Figure 27. REG0A 12-Bit DAC for Laser Diode Driver

				11	10	9	8
				VLDD			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VLDD							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. REG0A 12-Bit DAC for Laser Diode Driver Field Descriptions

Bit	Field	Type	Reset	Description
11-0	VLDD	W	0h	Digital input code for VLDD. Since VLDD is 11 bit length, VLDD[11] should be set 0. Binary format 0x000 to 0x7ff(+2047) LDD_OUT = VLDD × (120 mA / 2048) MSB (bit 11) is secured in order to unite with other 12-bit form.

8.6.4.11 REG70 8-Bit Control Register for DriverEna (offset = 70h) [reset =]

Figure 28. REG70 8-Bit Control Register for DriverEna

7	6	5	4	3	2	1	0
TLT_ENA	FCS_ENA	TRK_ENA	SPM_ENA	SLD_ENA	STP_ENA	LOAD_ENA	XSLEEP
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. REG70 8-Bit Control Register for DriverEna Field Descriptions

Bit	Field	Type	Reset	Description
7	TLT_ENA	RW	0h	1h = Tilt enable (with XSLEEP = 1)
6	FCS_ENA	RW	0h	1h = Focus enable (with XSLEEP = 1)
5	TRK_ENA	RW	0h	1h = Track enable (with XSLEEP = 1)
4	SPM_ENA	RW	0h	1h = Spindle enable (with XSLEEP = 1)
3	SLD_ENA	RW	0h	1h = Sled enable (with XSLEEP = 1)
2	STP_ENA	RW	0h	1h = Step enable (with XSLEEP = 1)
1	LOAD_ENA	RW	0h	1h = LOAD enable (with XSLEEP = 1) Track (bit5:TRK_ENA) will be disabled at LOAD_ENA = 1 because of sharing the DAC PWM module. Load priority is higher than TRK_ENA.
0	XSLEEP	RW	0h	1h = Operation mode (need 1 ms) 0h = Power save mode Charge pump enable bit All driver enable bit (Bit[7:1]) change disabled and output change to Hi-Z (regardless of setting xxx_ENA bit is 1) when setting XSLEEP to 0. Therefore, set 1 to XSLEEP before setting each enable bits.

8.6.4.12 REG71 8-Bit Control Register for FuncEna (offset = 71h) [reset =]

Figure 29. REG71 8-Bit Control Register for FuncEna

7	6	5	4	3	2	1	0
TI reserved	ENDDET_ENA	ENDDET_SEL		LDD_ENA	LDD_MSEL		TEMPMON_ENA
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0		rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. REG71 8-Bit Control Register for FuncEna Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	
6	ENDDET_ENA	RW	0h	1h = Use sled/step_End, load tray lock detection enable (with STP_ENA = 1, or SLD_ENA = 1, or LOAD_ENA = 1)
5-4	ENDDET_SEL	RW	0h	00 : Sled end detection monitor 01 : Step end detection monitor 10 : Load tray lock detection monitor
3	LDD_ENA	RW	0h	1h = LDD enable (with XSLEEP = 1)
2-1	LDD_MSEL	RW	0h	Laser diode driver output selection 00: No select 01: CD 10: DVD 11: BD
0	TEMPMON_ENA	RW	0h	1h = Enable chip temperature monitoring (with XSLEEP = 1)

8.6.4.13 REG72 8-Bit Control Register for ACTCfg (offset = 72h) [reset =]

Figure 30. REG72 8-Bit Control Register for ACTCfg

7	6	5	4	3	2	1	0
P12VMUTE_NORST	RSTIN_OFF	ACTPROT_OFF	ACTTEMPTH				
rw-0	rw-0	rw-0	rw-0				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. REG72 8-Bit Control Register for ACTCfg Field Descriptions

Bit	Field	Type	Reset	Description
7	P12VMUTE_NORST	RW	0h	0h = System reset at P12V low voltage 1h = Output High-Z only at P12V low voltage detection
6	RSTIN_OFF	RW	0h	0h = XRSTIN input enable 1h = Ignored XRSTIN pin input (do not reset device when XRSTIN = L)
5	ACTPROT_OFF	RW	0h	0h = Actuator protection ON 1h = Actuator fault monitor disable (no protection for ACT channel)
4-0	ACTTEMPTH	RW	0h	Actuator thermal protection (= ACT Timer) threshold level ACT Timer Protection enable except ACTTEMPTH[4:0] = 0x00 ACTTEMPTH = 0x00 equal to ACTPROT_OFF = 1 By writing value 0x00, ACTTIMER_PROT flag is cleared.

8.6.4.14 REG73 8-Bit Control Register for Parm0 (offset = 73h) [reset =]

Figure 31. REG73 8-Bit Control Register for Parm0

7	6	5	4	3	2	1	0
SIF_TIMEOUT_TH		SLEDEND_HZTIME	SLDENDTH		STPEND_HZTIME	STPENDTH	
rw-0		rw-0	rw-0		rw-0	rw-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. REG73 8-Bit Control Register for Parm0 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SIF_TIMEOUT_TH	RW	0h	Watch dog timer for serial communication 0h = disable 1h = 1 ms 2h = 100 µs 3h = 10 µs Set SIF_TIMEOUTERR (REG7D) if communication is suspended for this time period. Reset register processing is performed if a SIF_TIMEOUTERR occurs.
5	SLEDEND_HZTIME	RW	0h	Time window for sled end detection. 0h = 400 µs 1h = 200 µs Note: Need to recycle SLD_ENDDET_ENA = 0 → 1 after writing this bit.
4-3	SLDENDTH	RW	0h	Sled end detection sensibility setting. Detection threshold for motor BEMF 00: 124 mV 01: 168 mV 11: 73 mV 10: 0 mV
2	STPEND_HZTIME	RW	0h	Step High-Z detection period in end detection 0h = 400 µs 1h = 200 µs Note: Need to recycle STP_ENDDET_ENA = 0 → 1 after writing this bit.
1-0	STPENDTH	RW	0h	Step end detection sensibility setting 00: 39 mV 01: 60 mV 11: 19 mV 10: 0 mV

8.6.4.15 REG74 8-Bit Control Register for SIFCfg (offset = 74h) [reset =]

Figure 32. REG74 8-Bit Control Register for SIFCfg

7	6	5	4	3	2	1	0
DIFF_TLT	LDD_AMODE	RDSTAT_ON_VFCS	VSLD2_POL	VSTP2_POL	ADVANCE_RD	SOMI_HIZ	VDAC_MAPSW
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. REG74 8-Bit Control Register for SIFCfg Field Descriptions

Bit	Field	Type	Reset	Description
7	DIFF_TLT	RW	0h	1h = Differential tilt mode enable (with TLT_ENA = FCS_ENA = 1) Differential tilt mode (DIFF_TLT = 1), DAC value setting as follows FCS_OUT = (VFCS + VTLT) × 6 / 2048 TLT_OUT = (VFCS – VTLT) × 6 / 2048 In DIFF_TLT mode (DIFF_TLT = 1), TLT_OUT should be changed after writing VFCS.
6	LDD_AMODE	RW	0h	Setting LDD analog mode 0h = VLDD set by VDAC register (REG0A) 1h = VLDD set by voltage input via VLDDIN pin
5	RDSTAT_ON_VFCS	RW	0h	Set Read status data (REG7F) at VFCS write command (REG02) 1h = Enable Write and Read mode (Write 12 bits Focus DAC data + Read 8 bits status data)
4	VSLD2_POL	RW	0h	Change direction of SLED rotation
3	VSTP2_POL	RW	0h	Change direction of STEP rotation
2	ADVANCE_RD	RW	0h	0h = Normal read timing 1h = Read timing is advanced half clock cycle
1	SOMI_HIZ	RW	0h	0h = SOMI line High-Z at bus idling time. 1h = SOMI line pull down at bus idling time.
0	VDAC_MAPSW	RW	0h	1h = Change channel assignments of DAC register (REG01~0A)

8.6.4.16 REG75 8-Bit Control Register for Parm1 (offset = 75h) [reset =]

Figure 33. REG75 8-Bit Control Register for Parm1

7	6	5	4	3	2	1	0
TRAY_LOCKDET			TI reserved		SPM_FAST_BRK	SPM_SLNT_BRK	SPM_HIZMODE
rw-0			rw-0		rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. REG75 8-Bit Control Register for Parm1 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	TRAY_LOCKDET	RW	0H	Load tray locking detection control 0h = Disable detection 1-7: Detection threshold 1h = 100 mA 2h = 150 mA 3h = 200 mA 4h = 250 mA 5h = 300 mA 6h = 350 mA 7h = 400 mA
4-3	Reserved	RW	0h	
2	SPM_FAST_BRK	RW	0h	Fast brake mode selection 0h = Normal brake mode perform auto short brake sequence in specific speed 1h = No short brake under 5500 rpm
1	SPM_SLNT_BRK	RW	0h	Silent brake mode selection 0h = Normal brake mode 1h = No active brake under 5500 rpm Active brake mode is not performed inputting any value into VSPIN.
0	SPM_HIZMODE	RW	0h	Spindle output Hi-Z mode 0h = Normal operation 1h = Spindle output (UVW) put Hi-Z (use for test purpose)

8.6.4.17 REG76 8-Bit Control Register for WriteEna (offset = 76h) [reset =]

Figure 34. REG76 8-Bit Control Register for WriteEna

7	6	5	4	3	2	1	0
WRITE_ENABLE	TI reserved						REG6X_Write
rw-0	rw-0						rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. REG76 8-Bit Control Register for WriteEna Field Descriptions

Bit	Field	Type	Reset	Description
7	WRITE_ENABLE	RW	0h	0h = Register Write disable except REG76 1h = Write enable for registers REG01~09, REG70~7F
6-1	Reserved	RW	0h	
0	REG6X_Write	RW	0h	0h = Disable Write access REG6X bank 1h = Enable Write access REG6X bank

8.6.4.18 REG77 8-Bit Control Register for ClrReg (offset = 77h) [reset =]

Figure 35. REG77 8-Bit Control Register for ClrReg

7	6	5	4	3	2	1	0
RST_INDAC	RST_REGS	RST_ERR_FLAG	TI reserved				
w-0	w-0	w-0	w-0				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. REG77 8-Bit Control Register for ClrReg Field Descriptions

Bit	Field	Type	Reset	Description
7	RST_INDAC	W	0h	1h = Reset all 12-bit input DAC register (REG01~09) *Self clear bit
6	RST_REGS	W	0h	1h = Reset all 8-bit R/W Registers (REG70h~77h, 60h-6Fh) *Self clear bit
5	RST_ERR_FLAG	W	0h	1h = Reset Fault Flag Latch (REG7F, REG79~REG7D) *Self clear bit
4-0	Reserved	W	0h	

8.6.4.19 REG78 8-Bit Control Register for ActTemp (offset = 78h) [reset =]

Figure 36. REG78 8-Bit Control Register for ActTemp

7	6	5	4	3	2	1	0
TI reserved		ACT_TIMER_PROT	ACTTEMP				
r-0		r-0	r-0				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. REG78 8-Bit Control Register for ActTemp Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	
5	ACT_TIMER_PROT	R	0h	ACT timer protection flag 1h = ACT timer protection has detected and latched. (ACTTEMP > ACTTEMPTH) This bit holds data after temperature change to low since this is a latch bit. Also driver output keep Hi-Z until setting RST_ERR_FLAG or ACTTEMPTH = 0.
4-0	ACTTEMP	R	0h	An integrated value of ACT_TIMER counters at present

8.6.4.20 REG79 8-Bit Control Register for UVLOMon (offset = 79h) [reset =]

Figure 37. REG79 8-Bit Control Register for UVLOMon

7	6	5	4	3	2	1	0
TI Reserved		UVLO_P5V	UVLO_INT3P3	UVLO_P12V	UVLO_SIOV	OVP_P5V	OVP_P12V
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. REG79 8-Bit Control Register for UVLOMon Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	
5	UVLO_P5V	R	0h	UVLO flag for detection Low P5V supply (1)
4	UVLO_INT3P3	R	0h	UVLO flag for detection Low internal 3.3 V regulator(1)
3	UVLO_P12V	R	0h	UVLO flag for detection Low P12V supply (1)
2	UVLO_SIOV	R	0h	UVLO flag for detection Low SIOV supply (1)
1	OVP_P5V	R	0h	Overvoltage protection flag for P5V supply (1)
0	OVP_P12V	R	0h	Overvoltage protection flag for P12V supply (1)

(1) Latched first reset event only. Cleared by RST_ERR_FLG (REG77)

8.6.4.21 REG7A 8-Bit Control Register for TSDMon (offset = 7Ah) [reset =]

Figure 38. REG7A 8-Bit Control Register for TSDMon

7	6	5	4	3	2	1	0
TI reserved	TSD_FAULT _SPM	TSD_FAULT _ACT	TSD_FAULT _LDD	TI reserved	TSD_SPM	TSD_ACT	TSD_ LDD
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. REG7A 8-Bit Control Register for TSDMon Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	
6	TSD_FAULT_SPM	R	0h	Pre alert of thermal protection of Spindle block(1)
5	TSD_FAULT_ACT	R	0h	Pre alert of thermal protection of focus, track, tilt, sled1, sled2, step1, step2, load(1)
4	TSD_FAULT_LDD	R	0h	Prealert of thermal protection of LDD(1)
3	Reserved	R	0h	
2	TSD_SPM	R	0h	Thermal protection flag for Spindle(1) SPM output Hi-Z until temperature falls on release level 1h = Detect (latch)
1	TSD_ACT	R	0h	Thermal protection flag for focus, track, tilt, sled1, sled2, step1, step2, load(1) Actuator output Hi-Z until temperature falls on release level 1h = Detect (latch)
0	TSD_ LDD	R	0h	Thermal protection flag for LDD(1) LDD output Hi-Z until temperature falls on release level 1h = Detect (latch)

(1) Cleared by RST_ERR_FLAG bit (REG77)

8.6.4.22 REG7B 8-Bit Control Register for OCPMon (offset = 7Bh) [reset =]

Figure 39. REG7B 8-Bit Control Register for OCPMon

7	6	5	4	3	2	1	0
TI reserved		OCP_STP	SCP_SPM	SCP_SLED	SCP_LOAD	SCP_ACT	SCP_STP
r-0		r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. REG7B 8-Bit Control Register for OCPMon Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	
5	OCP_STP	R	0h	Overcurrent protection flag bit for step block(1)
4	SCP_SPM	R	0h	Short protection flag bit for spindle block(1)
3	SCP_SLED	R	0h	Short protection flag bit for sled block(1)
2	SCP_LOAD	R	0h	Short protection flag bit for load block(1)
1	SCP_ACT	R	0h	Short protection flag bit for actuator block(1)
0	SCP_STP	R	0h	Short protection flag bit for step block(1)

(1) Cleared by RST_ERR_FLAG bit (REG77)

8.6.4.23 REG7C 8-Bit Control Register for TempMon (offset = 7Ch) [reset =]

Figure 40. REG7C 8-Bit Control Register for TempMon

7	6	5	4	3	2	1	0
TI Reserved	CHIPTEMP _STATUS	CHIPTEMP					
r-0	r-0	r-0					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. REG7C 8-Bit Control Register for TempMon Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	
6	CHIPTEMP_STATUS	R	0h	1h = New data CHIPTEMP[5:0] is updated It will be cleared after reading.
5-0	CHIPTEMP	R	0h	Chip temperature monitor (2.38°/LSB) 15(0) to 165(63) degrees. For monitoring, TEMPMON_ENA = 1 and XSLEEP = 1 is required

8.6.4.24 REG7E 8-Bit Control Register for Version (offset = 7Eh) [reset =]

Figure 41. REG7E 8-Bit Control Register for Version

7	6	5	4	3	2	1	0
Version							
r-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. REG7E 8-Bit Control Register for Version Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Version	R	0h	Version[7:4] = Revision number of TPIC2050 Version[3:0] = Option

8.6.4.25 REG7F 8-Bit Control Register for Status (offset = 7Fh) [reset =]

Figure 42. REG7F 8-Bit Control Register for Status

7	6	5	4	3	2	1	0
ACTTIMER_FAULT	ENDDET	SIF_TIMEOUTERR	PWRERR	TSDERR	OCPERR	TSDFAULT	FG
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. REG7F 8-Bit Control Register for Status Field Descriptions

Bit	Field	Type	Reset	Description
7	ACTTIMER_FAULT	R	0h	Status flag of ACTTIMER protection 1h = Prealert of ACTTIMER protection. It is close to the threshold level. The user can get the current ACTTIMER value in REG78. Both this bit and ACT_TIMER_PROT (REG78) are set when over the threshold.
6	ENDDET	R	0h	Status flag of END detection 1h = End position detected (not latch bit) for step/sled. (ENDDET_SEL = 10) Load motor current exceeds threshold at using load tray lock detection. (ENDDET_SEL = 10)
5	SIF_TIMEOUTERR	R	0h	Error flag of serial interface watch dog timer 1h = SIF communication was interrupted, expired watch dog timer
4	PWRERR	R	0h	Error flag of power 1h = Voltage problem occurred, details in REG79
3	TSDERR	R	0h	Error flag of any overthermal protections 1h = Dispatched thermal protection, details in REG7A
2	OCPERR	R	0h	Error flag of any short-circuit protection 1h = Dispatched SCP, details in REG7Bh
1	TSDFAULT	R	0h	Warning of TSD of any thermal protection 1h = Detect pre thermal protection, details in REG7A
0	FG	R	0h	FG signal. Spindle rotation pulse for speed monitor

8.6.4.26 REG61 8-Bit Control Register for SPM1 (offset = 61h) [reset =]

Figure 43. REG61 8-Bit Control Register for SPM1

7	6	5	4	3	2	1	0
PWMmaxDuty_R_SEL1	TI reserved	OVP_SBRAKE_OFF	TI reserved		SBRAKE_ON	TI reserved	
rw-0	rw-0	rw-0	rw-0		rw-0	rw-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. REG61 8-Bit Control Register for SPM1 Field Descriptions

Bit	Field	Type	Reset	Description
7	PWMmaxDuty_R_SEL1	RW	0h	PWM duty maximum setting in active brake mode (upper bit of PWMmaxDuty_R_SEL[1:0]) 00: Maximum PWM duty 12.5% 01: Maximum PWM duty 25% 10: Maximum PWM duty 37.5% 11: Maximum PWM duty 37.5% (TI recommends to set to 0X in case of use in no-disk, because it may not stop in a specific motor setting 37.5%.)
6	Reserved	RW	0h	
5	OVP_SBRAKE_OFF	RW	0h	Select short brake mode of P12V pre-OVP 0h = 3-phase short brake mode 1h = 2-phase short brake mode
4-3	Reserved	RW	0h	
2	SBRAKE_ON	RW	0h	Force short brake 0h = No brake 1h = Perform 3-phase short brake in any state
1-0	Reserved	RW	0h	

8.6.4.27 REG62 8-Bit Control Register for SPM2 (offset = 62h) [reset =]

Figure 44. REG62 8-Bit Control Register for SPM2

7	6	5	4	3	2	1	0
TI reserved							PWMmaxDuty_R_SEL0
rw-0				rw-0			rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. REG62 8-Bit Control Register for SPM2 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	RW	0h	
0	PWMmaxDuty_R_SEL0	RW	0h	PWM duty maximum setting in active brake mode (lower bit of PWMmaxDuty_R_SEL[1:0])

8.6.4.28 REG6B 8-Bit Control Register for DisProt (offset = 6Bh) [reset =]

Figure 45. REG6B 8-Bit Control Register for DisProt

7	6	5	4	3	2	1	0
SCP_SPM_OFF	SCP_SLED_OFF	SCP_LOAD_OFF	SCP_ACT_OFF	SCP_STP_OFF	OCP_STP_OFF	TI reserved	OVPPRE12V_OFF
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. REG6B 8-Bit Control Register for DisProt Field Descriptions

Bit	Field	Type	Reset	Description
7	SCP_SPM_OFF	RW	0h	Control bit of short-circuit protection function for spindle block 0h = Enable SCP function 1h = Disable SCP function Caution(1): TI recommends using it only for test purposes.
6	SCP_SLED_OFF	RW	0h	For sled driver block Caution(1): TI recommends using it only for test purposes.
5	SCP_LOAD_OFF	RW	0h	For load driver block Caution(1): TI recommends using it only for test purposes.
4	SCP_ACT_OFF	RW	0h	For actuator driver block Caution(1): TI recommends using it only for test purposes.
3	SCP_STP_OFF	RW	0h	For step driver block Caution(1): TI recommends using it only for test purposes.
2	OCP_STP_OFF	RW	0h	Control bit of overcurrent protection function for stepper block 0h = Enable OCP function 1h = Disable OCP function Caution(1): TI recommends using it only for test purpose.
1	Reserved	RW	0h	
0	OVPPRE12V_OFF	RW	0h	Disable short brake function at P12V pre-OVP condition. 0h = Enable function which perform short brake at 12-V pre-OVP 1h = Disable short brake at 12-V pre-OVP TI recommend to set to 0

(1) CAUTION: Device will be fatally damaged if short circuit occurs in the xxx_OFF = 1.

8.6.4.29 REG6C 8-Bit Control Register for STPCfg (offset = 6Ch) [reset =]

Figure 46. REG6C 8-Bit Control Register for STPCfg

7	6	5	4	3	2	1	0
TI Reserved			LDD_IUP		TI Reserved	STP_WIND_HIZ	STP_WIND_H
rw-0			rw-0		rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. REG6C 8-Bit Control Register for STPCfg Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	RW	0h	
4-3	LDD_IUP	RW	0h	Extend LDD maximum current 00: 120 mA 01: 1.24× an initial value 10: 1.48× an initial value (*1) 11: 1.72× an initial value (*2) *1) The LDD output time of the maximum current should maintain 50% or less of the xsleep total ON time. *2) The LDD output time of the maximum current should maintain 25% or less of the xsleep total ON time.
2	Reserved	RW	0h	
1	STP_WIND_HIZ	RW	0h	0h = Normal end detection 1h = When detecting BEMF, set STP1 and STP2 FET Hi-Z to reduce mutual noise.
0	STP_WIND_H	RW	0h	0h = Normal end detection 1h = When detecting BEMF, set driving phase to Hi (detecting phase Hi-Z) to reduce mutual noise.

8.6.4.30 REG6E 8-Bit Control Register for UtilCfg (offset = 6Eh) [reset =]

Figure 47. REG6E 8-Bit Control Register for UtilCfg

7	6	5	4	3	2	1	0
GPOUT_HL	GPOUT_ENA	TI reserved					
rw-0	rw-0	rw-0					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. REG6E 8-Bit Control Register for UtilCfg Field Descriptions

Bit	Field	Type	Reset	Description
7	GPOUT_HL	RW	0h	GPOUT (general-purpose output) pin output selection 0h = Low output 1h = High output Valid only if REG6F = 00h
6	GPOUT_ENA	RW	0h	Enable monitor signal output to GPOUT pin 0h = No signal output, Hi-Z 1h = Output signal selected in REG6F with CMOS output Output is logical OR when selected two more signals
5-0	Reserved	RW	0h	

8.6.4.31 REG6F 8-Bit Control Register for MonitorSet (offset = 6Fh) [reset =]

Figure 48. REG6F 8-Bit Control Register for MonitorSet

7	6	5	4	3	2	1	0
ACTTIMER_FLT_MON	ENDDET_MON	SIF_TIMEOUTERR_MON	PWRERR_MON	TSDERR_MON	OCPERR_MON	TSDFAULT_MON	TI Rsvd
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. REG6F 8-Bit Control Register for MonitorSet Field Descriptions

Bit	Field	Type	Reset	Description
7	ACTTIMER_FLT_MON	RW	0h	1h = ACTTIMER fault output to GPOUT pin
6	MONITOR_MON	RW	0h	1h = ENDDET monitor output to GPOUT pin
5	SIF_TIMEOUTERR_MON	RW	0h	1h = SIF timeout monitor output to GPOUT pin
4	PWRERR_MON	RW	0h	1h = PWRERR monitor output to GPOUT pin
3	TSDERR_MON	RW	0h	1h = TSDERR fault output to GPOUT pin
2	SCPERR_MON	RW	0h	1h = OCPERR fault output to GPOUT pin
1	TSDFAULT_MON	RW	0h	1h = TSDFAULT fault output to GPOUT pin
0	Reserved	RW	0h	

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Voltage Monitoring

Power faults are reported in the UVLOMon register. Each UVLOMon bit initializes to 0 upon a cold power up. After a fault is detected, the appropriate fault bit is latched high. Writing to the RST_ERRFLG (REG77) clears all UVLOMon bits. Table 39 summarizes the power device faults and actions.

Table 39. Power Fault Monitor

FAULT TYPE	LATCHED REGISTER	POR	CRITERIA	DRIVER OUTPUT AT DETECTION					
				SPM	SLED	LOAD	STEP	ACT	LDD
P5V under voltage	UVLO_P5V	Yes	<3.7 V	Hi-Z					
Internal 3.3-V under voltage	UVLO_INT3P3	Yes	<2.7 V	Hi-Z					
P12V under voltage	UVLO_P12V	Yes(1)	<8.4 V	Hi-Z					
SIOV under voltage	UVLO_SIOV	Yes	<2.0 V	Hi-Z					
P5V over voltage	OVP_P5V		>6.2 V	Hi-Z					
P12V over voltage	OVP_P12V		>14.9 V	Hi-Z			—	—	—

(1) P12VMUTE_NORST = 0: force POR, P12VMUTE_NORST=1: no POR

9.1.2 Spindle Motor Driver Operating Sequence

When the VSPM is set to a positive DAC code, it enters into acceleration mode. Initial position sense (IS) mode then operates, as the start-up circuits offer the start-up pattern sequence to the driver, then switch to spin-up mode by detecting the rotor position using the BEMF signal from the spindle motor coil.

The spin-down and brake function are also controlled by the DAC value VSPM. When it has set the brake command to the VSPM, the driver goes into active-brake mode, then switches to short-brake mode in slow revolution speed, and then stops automatically. EXOR of a three-phase signal comprises the FG signal and is output from the XFG pin as shown in Figure 49.

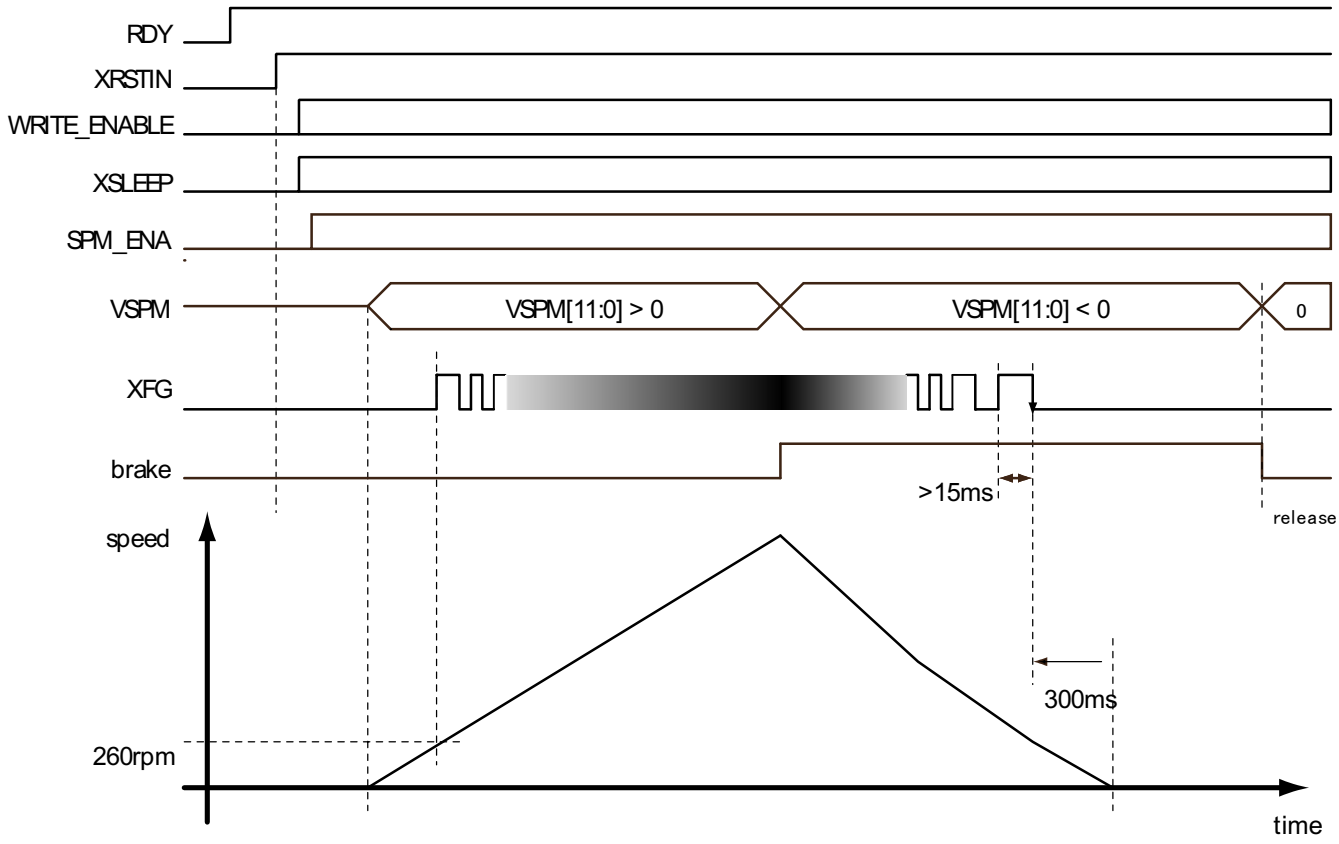


Figure 49. Spindle Operating Sequence

Use the down-edge of the FG signal for monitoring FG frequency.

Short brake mode asserts after 300 ms if the FG signal stays L-level in deceleration.

This value is the nominal number of using a 12-poles motor.

The internal circuit starts 800 µs (typical) after the RDY pin changes to 'H'. Recommended marginal delay value is 1 ms.

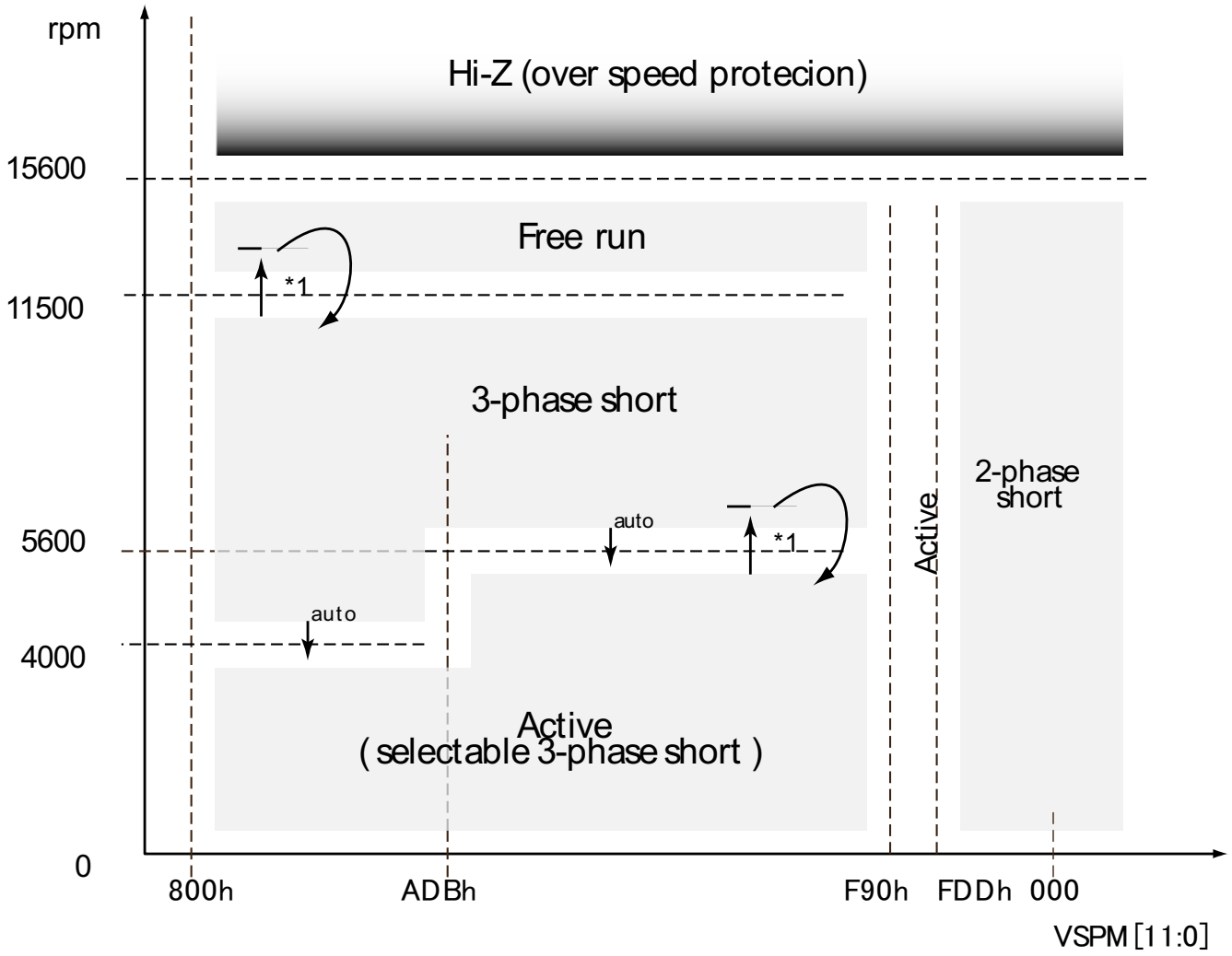
9.1.3 Auto Short Brake Function

The TPIC2050 provides an auto short brake function that selects a brake mode automatically by motor speed. Auto short brake includes two modes: short brake and active brake. If a value of 0xF90 or less is set to the VSPM, the brake mode automatically changes at rotation speed. This function enables low-power consumption and silent braking. Figure 50 shows the relation between brake mode and speed. The over-speed protect function suspends the SPM driver output at 15000 or more revolutions.

Table 40. Brake Mode

VSPM[11:0]	MODE	APPROXIMATE ROTATION SPEED (RPM)(1)			
		11500	11500 TO 5600	5600 TO 4000	4000 TO 0
0x000 to 0xFDD	Manual	2-phase short brake			
0xFDC to 0xF90	Manual	Active brake			
0xF8F to 0xADB	Auto short	Free run	3-phase short Brake(2)	Active brake	
0xADA to 0x800	Auto short	Free run	3-phase short brake(3)		Active brake

(1) Typical value using a 12-pole motor
(2) Active brake is chosen when it does not exceed 6400 rpm once from a rotation start.
(3) Active brake is chosen when it does not exceed 4600 rpm once from a rotation start.



Each threshold value has hysteresis.
Brake mode will change to specific mode at the threshold speed after it reaches a speed about 15% higher than a threshold speed.

NOTE: These speed values are the nominal number of using a 12-pole motor. In applying to a 16-pole motor, the rotation speed becomes 75% of indicated rpm values.

Figure 50. Brake Mode Selection

9.1.4 Spindle PWM Control

The output PWM duty of the spindle is controlled by the DAC code (VSPM). The gain in acceleration setting is always 14 times, but the maximum output is restricted to P12V voltage. A dead band with an output = 0 exists in the width between ±0x52 focusing on zero.

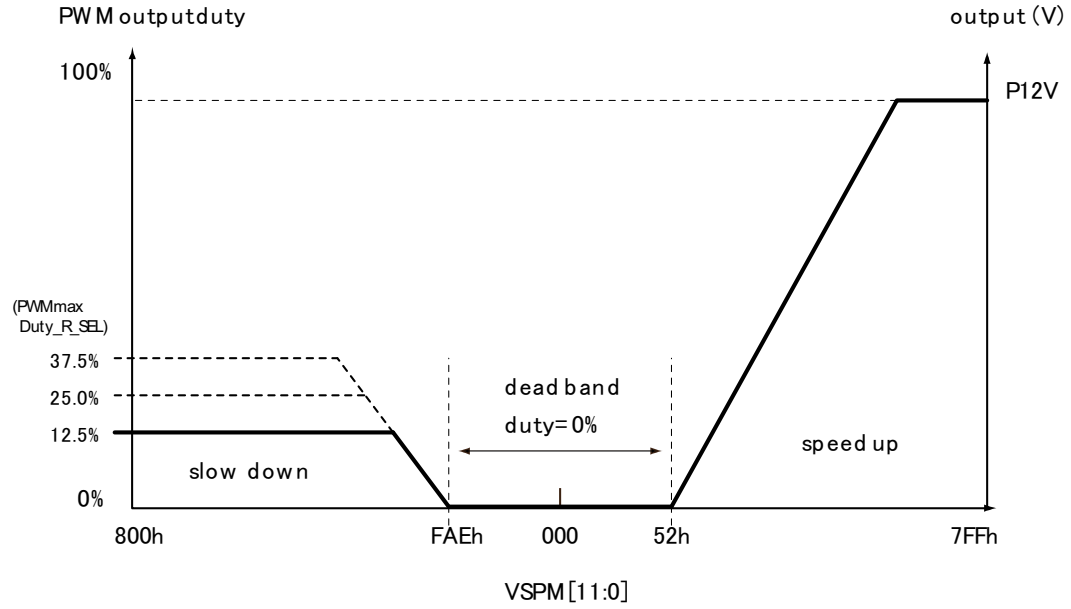


Figure 51. Spindle PWM Control

9.1.5 Spindle Driver Current Limiting Circuit

The current limit circuit monitors the RCS voltage at the ICOM pin and limits the output current by reducing the PWM duty when detecting overcurrent conditions.

9.1.6 Sled Driver Part

The sled driver outputs the PWM pulse set as DAC code (VSLDx) with current feedback. The maximum output is restricted to 880 mA at 0x7FF and 0x800. A dead band with an output = 0 exists in the width of ±0x33 focusing on zero.

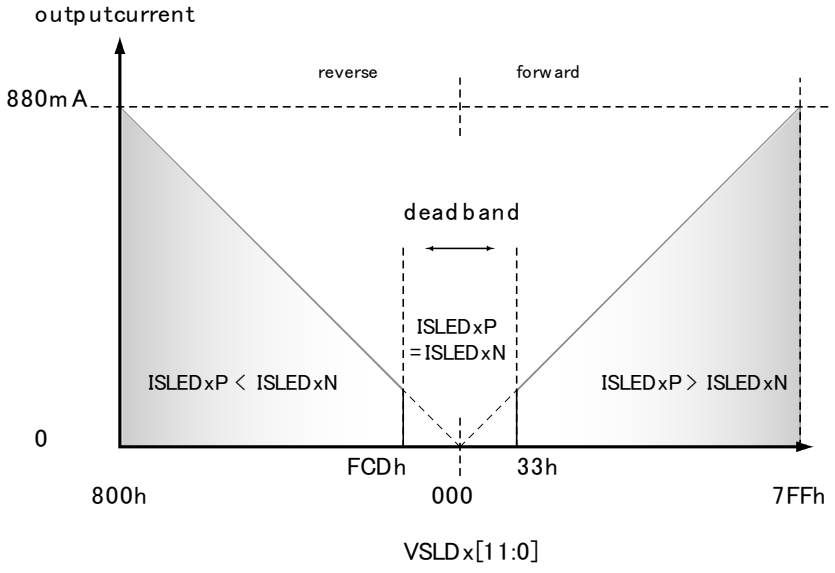


Figure 52. Sled Output Current

Both outputs of SLED1/2 are 'H' when the input code is in the dead band.

9.1.7 Stepping Driver Part

The step driver outputs the PWM pulse, set as an 8-bit DAC code (VSTPx) using VSTP[11:4]. There is no feedback monitor for output. The pulse width is output according to the P5V power supply voltage.

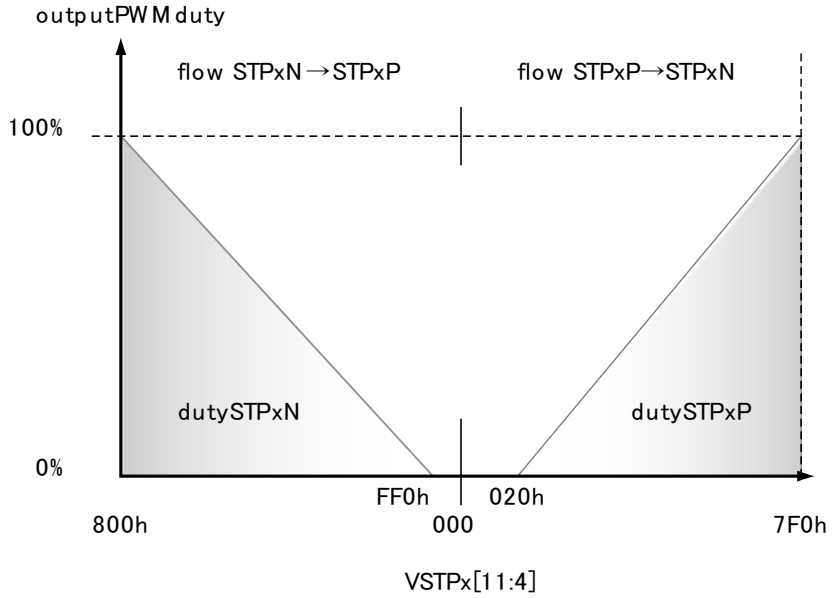


Figure 53. Step Output Duty

9.1.8 Focus/Track/Tilt Driver Part

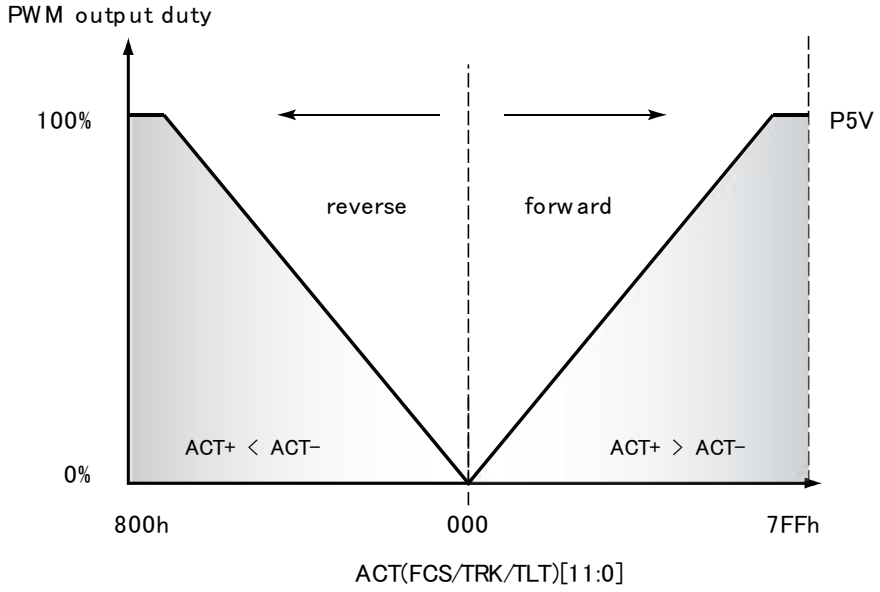


Figure 54. FCS/TRK/TLT Output Duty

9.1.9 Load Driver Part

The load driver outputs the voltage with the voltage feedback corresponding to the input DAC value. This channel has power voltage compensation, and is thus suited for slot-in type load control. This channel becomes active exclusively to other actuator channels. The load driver is shared with the TRK driver.

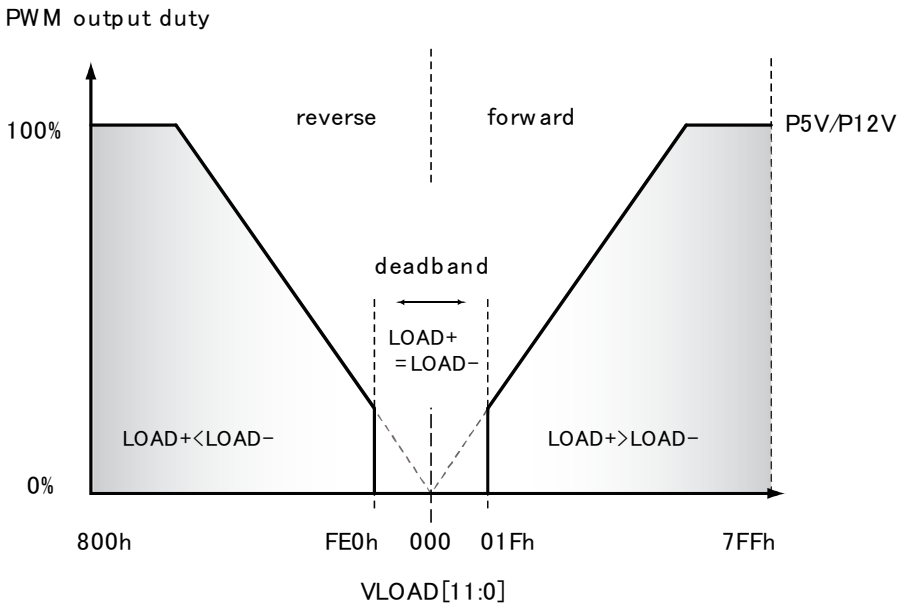


Figure 55. Load Output Duty

9.1.10 End Detect Function

This device has end position detection for the sled and collimator lens. This function eliminates the position switch at the PUH inner and collimator lens end positions. This function is enabled by ENDDET_ENA = 1, setting the object actuator (ENDDET_SEL = 00: for sled / ENDDET_SEL = 01: for step). When this function is enabled, internal logic detects the sled out zero-cross point, then the internal BEMF detect circuit measures the BEMF level of the stepping motor. There are four threshold levels. If the BEMF is lower than the selected threshold, the device recognizes the motor at stop and sets the ENDDET bit to 1. The ENDDET bit is then cleared at the BEMF voltage exceed threshold.

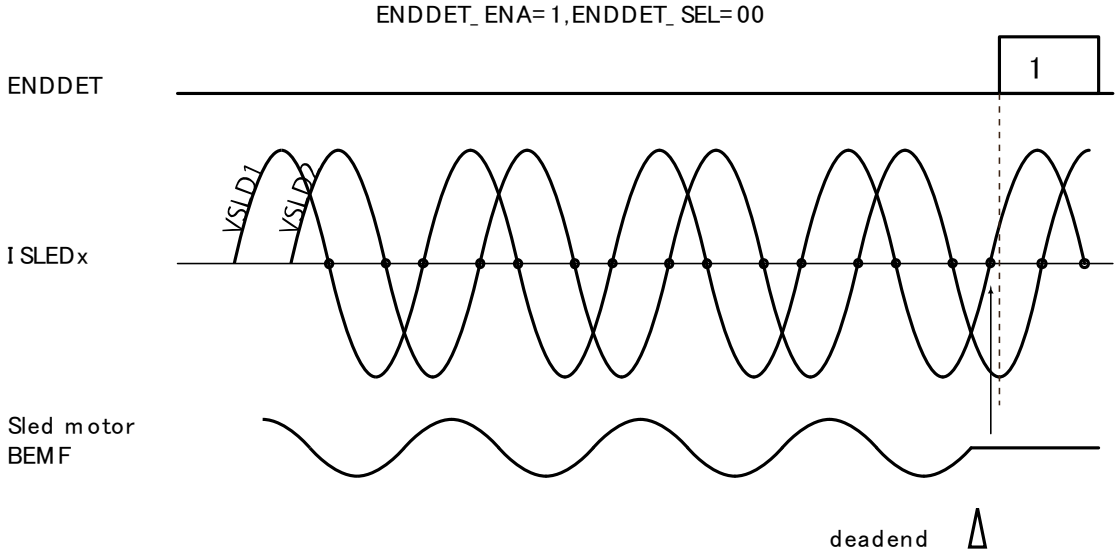


Figure 56. Timing of Sled End Detection

For the purpose of getting the correct stepping motor BEMF, choose a control frequency higher than 110 Hz (440 pps). This control frequency depends on the stepping motor characteristics.

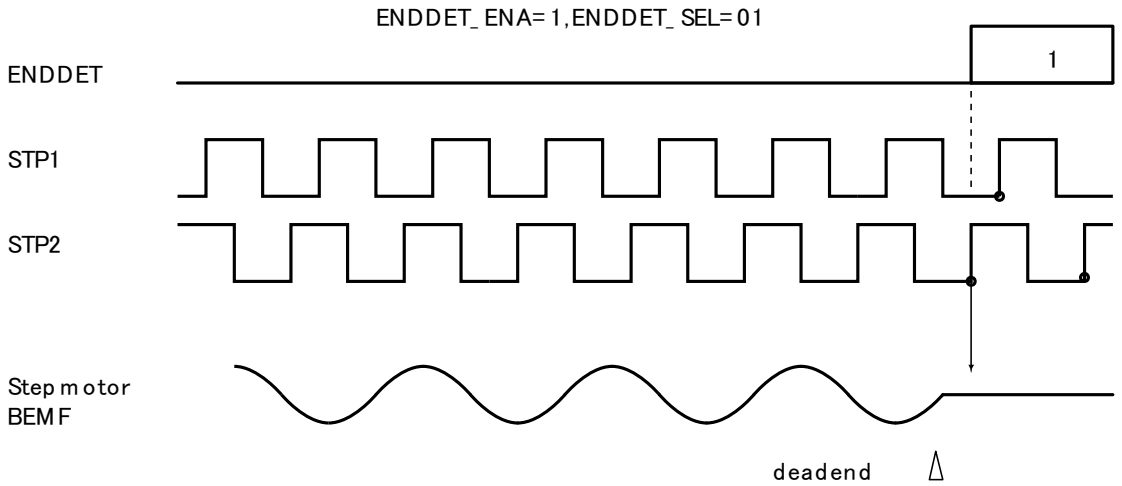


Figure 57. Timing of Step End Detection

The recommended control speed is around 1200 pps for getting the correct BEMF level. This depends on the stepping motor characteristic. Evaluate your condition appropriately.

9.1.11 Load Tray Lock Detect Function

The tray lock detect function detects an inserted obstacle when the tray opens and closes, using the load motor BEMF. Adjusting TRAY_LOCKDET [2:0] (REG75) by the characteristic of a motor is required for an optimal threshold level. The designer can set a threshold level from 100 to 400 mA, with a 50-mA step, using TRAY_LOCKDET.

Observe the lock detection by reading the ENDDET (REG7F) flag where ENDDET_SEL = 2 or 3 is set.

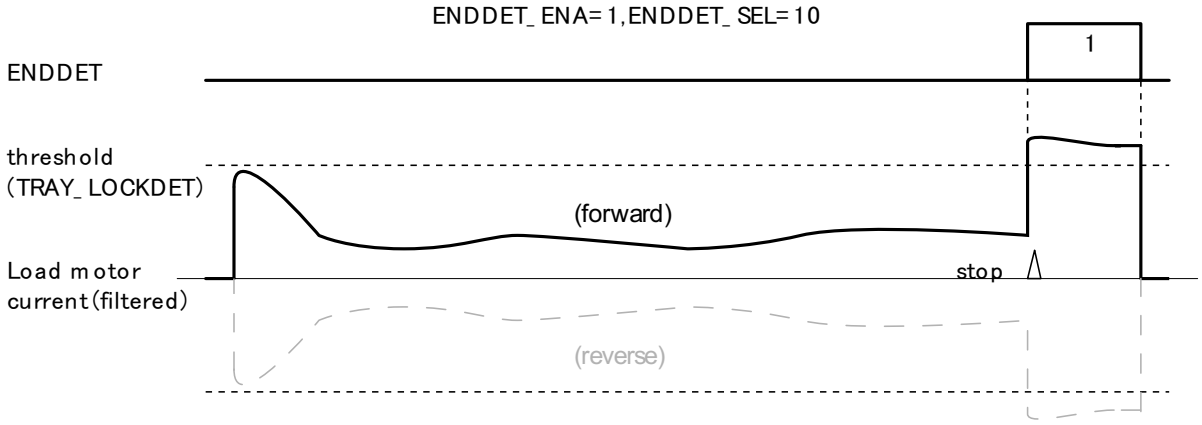


Figure 58. Load Tray Lock Detect

9.1.12 Three-Beam Laser Diode Driver

The device has a circuit for the three-beam laser diode drivers containing Blu-ray™. The output is chosen with LDD_MSEL (REG71), and the LD drive current is outputted by input 11-bit DAC code to VLDD[10:0] and VLDDIN with analog input. The change in analog mode and digital mode is set up by LDD_AMODE (REG74). The MSB of VLDD is the sign bit and is ignored if it set to 1. All output, including BD, DVD, and CD, has an internal pulldown 3 kΩ.

The mode change delay circuit and LVP are integrated to prevent a rush of current when the mode changes. When the LDD mode is changed, VLDD<10:0> is cleared to 0 to prevent the selected laser diode from breaking, as LDD sets the current value according to each kind.

Table 41. LDD Mode

LDD_MSEL[1:0]	ENABLE	CURRENT OUTPUT
11	BD	ILDD_BD
10	DVD	ILDD_DVD
01	CD	ILDD_CD

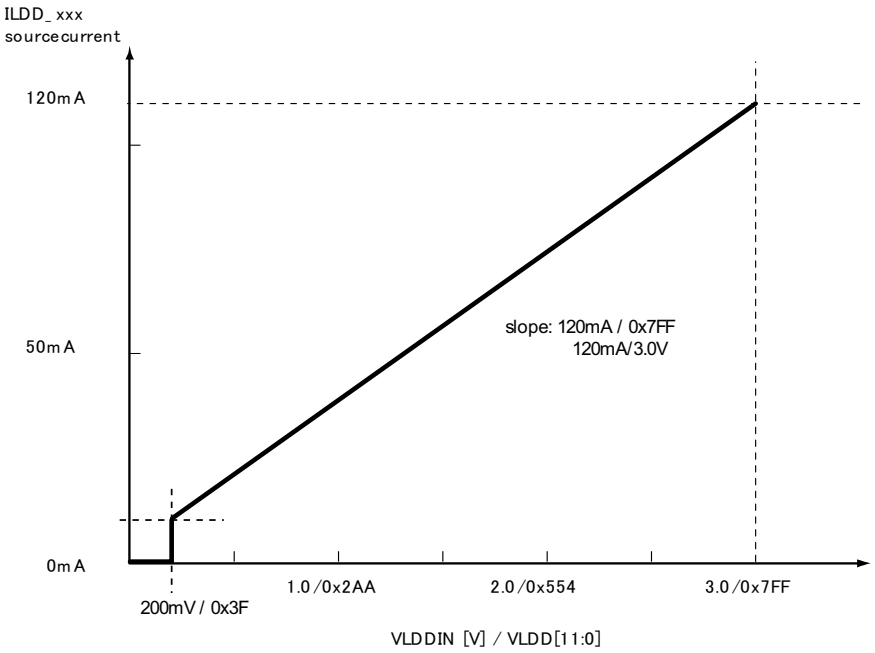


Figure 59. VLDD vs Output Average Current

9.1.13 Monitor Signal on GPOUT

The device can output a specific signal to the GPOUT pin. To output a signal, choose a signal from REG6F by enabling it first, then enabling GPOUT_ENA. When two or more signals are set for GPOUT, the output is a logical sum.

9.1.14 Example Timing of Target Control System

The TPIC2050 is designed to meet the requirements for updating control data in 400 kHz. Table 42 lists examples of the control system parameters. It takes 0.51 µs to transmit a 16-bit data packet to the TPIC2050 with a 35-MHz SCLK. Therefore, DSP can be sent in four packets at a 400-kHz interval. If the SCLK is lower than 28.8 MHz, the user must reduce the packet quantity to less than three. For example, the Focus/Truck command updates every 2.5 µs (400 kHz), and is able to send another two kinds of packets in this same slot. Figure 60 shows an example of the control timing when using the TPIC2050.

Table 42. Example Timing of Target Control System

SIGNAL	BIT	UPDATE CYCLE (kHz)
Focus	12	400
Track	12	400
Tilt	12	100
Sled1	10	100
Sled2	10	100
Spindle	12	100
Load	12	—
Step1	8	40
Step2	8	40

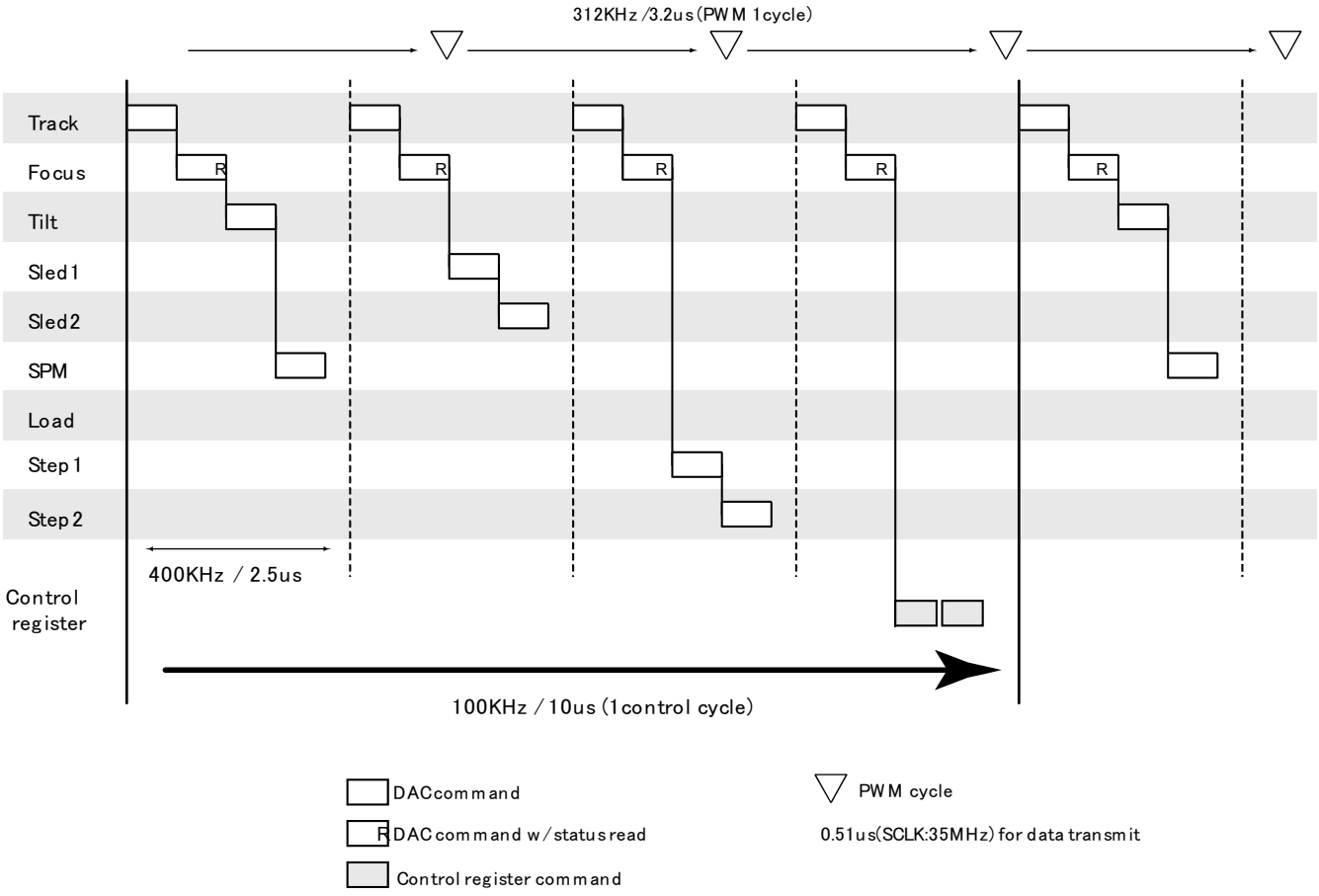


Figure 60. Example DAC Control

9.2 Typical Application

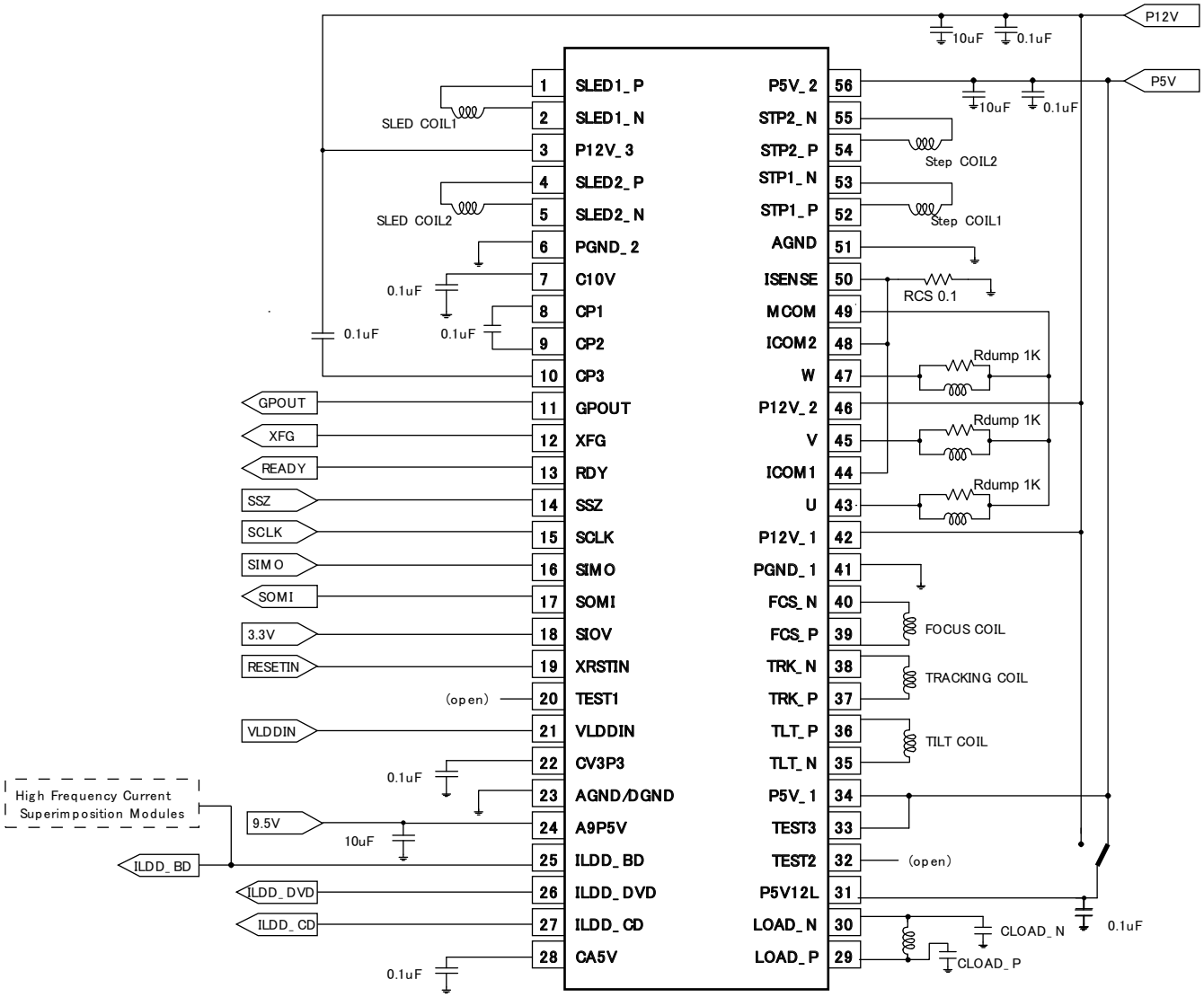


Figure 61. Example Application Circuit

9.2.1 Design Requirements

To begin the design process, determine the following:

1. Motor configuration: The user can use all motor channels or part of them.
2. Usage for ILDD: BD, DVD, or CD
3. RDY pin can be connected to Host CPU, then Host CPU can know the power supply status of TPIC2050.

9.2.2 Detailed Design Procedure

After power up on 5-V and 12-V supply, register can be changed following way and enabling motors.

1. Set WRITE_ENABLE = 1 on REG76 via SPI.
2. Set XSLEEP = 1 at REG70
3. Enable motor channel by ENA_XXX bits on REG70
4. Change the DAC settings for the motor on REG01-0B. Then, output channels start driving load.

Typical Application (continued)

9.2.3 Application Curves

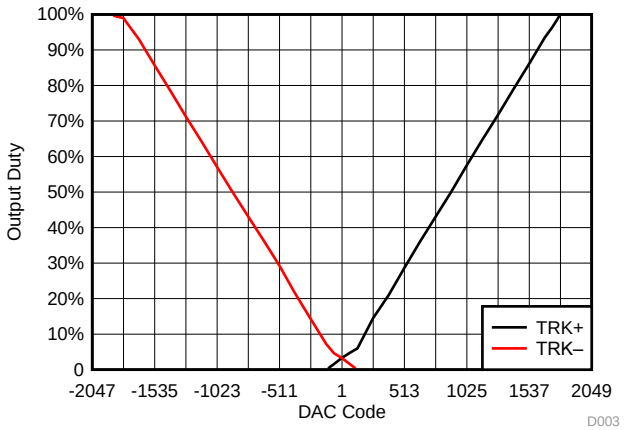


Figure 62. TRK Driver: DAC Code vs Output On Duty

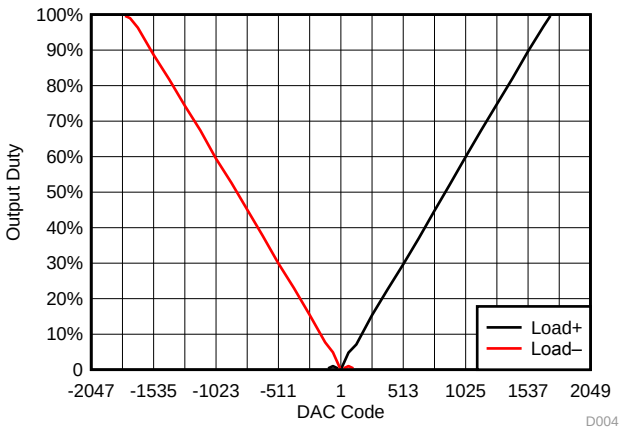


Figure 63. Load Driver: DAC Code vs Output On Duty

10 Power Supply Recommendations

All driver channels should only be operated after the required power is supplied and stable.

To calculate the spindle motor driver overcurrent limit (I_{Limit}), use Equation 4.

$$I_{Limit} = \text{Internal REF voltage} / R_{CS} = 194\ mV / 0.1\ \Omega \approx 1940\ mA \quad (4)$$

The capacity of the decoupling capacitor requires a value over 10 µF to reduce the influence of the PWM switching noise. The P5V pin must connect to a filter of 1 µF. Place a bypass capacitor (about 0.1 µF) near the power pin P5V, P5V12L, or P12V) for PWM switching noise reduction on the power and GND lines.

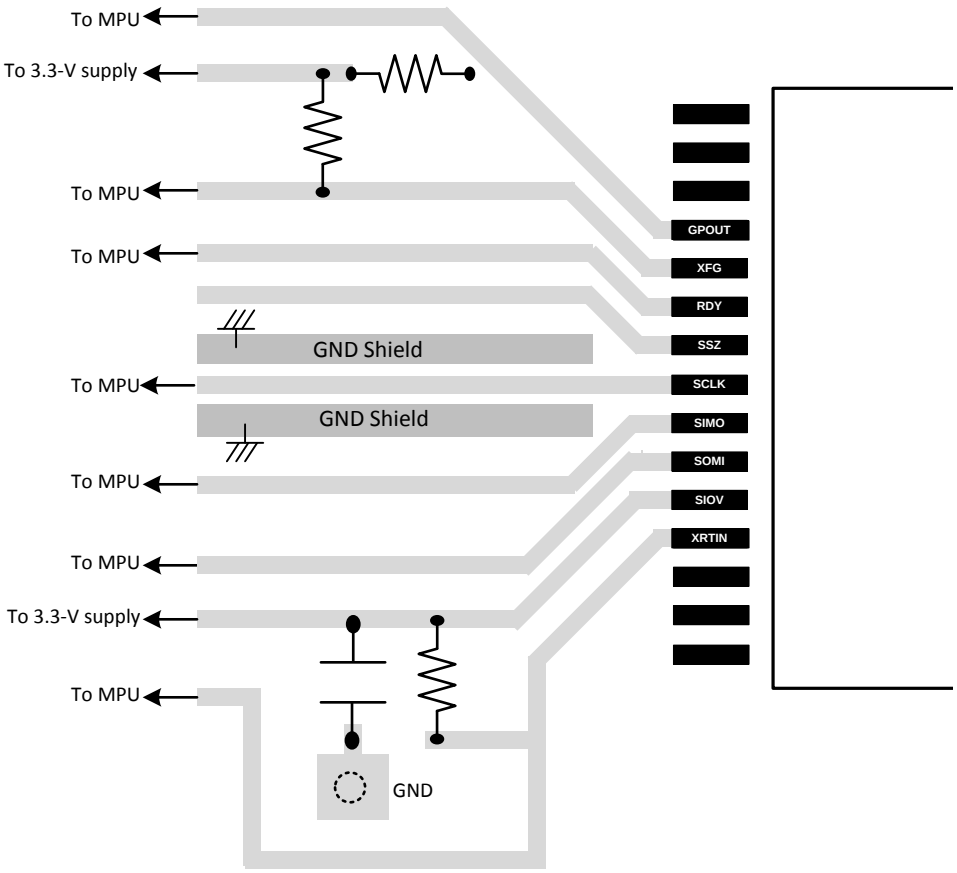
The current flow to the driver circuits depends on the pattern layout, line impedance, and noise influence from the supply line.

11 Layout

11.1 Layout Guidelines

1. CV3P3V, CA5V, and C10V requires external capacitor. Because these are reference voltage for device, locate the capacitor as close to device as possible. Keep away from noise source.
2. SCLK ground shielding is recommended.

11.2 Layout Example



A. GND shield is recommended for SCLK.

Figure 64. Layout Example Between TPIC2050 and MPU

12 器件和文档支持

12.1 社区资源

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12.3 静电放电警告

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC2050RDFDRG4	ACTIVE	HTSSOP	DFD	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-20 to 75	2050	Samples

(1) The marketing status values are defined as follows:
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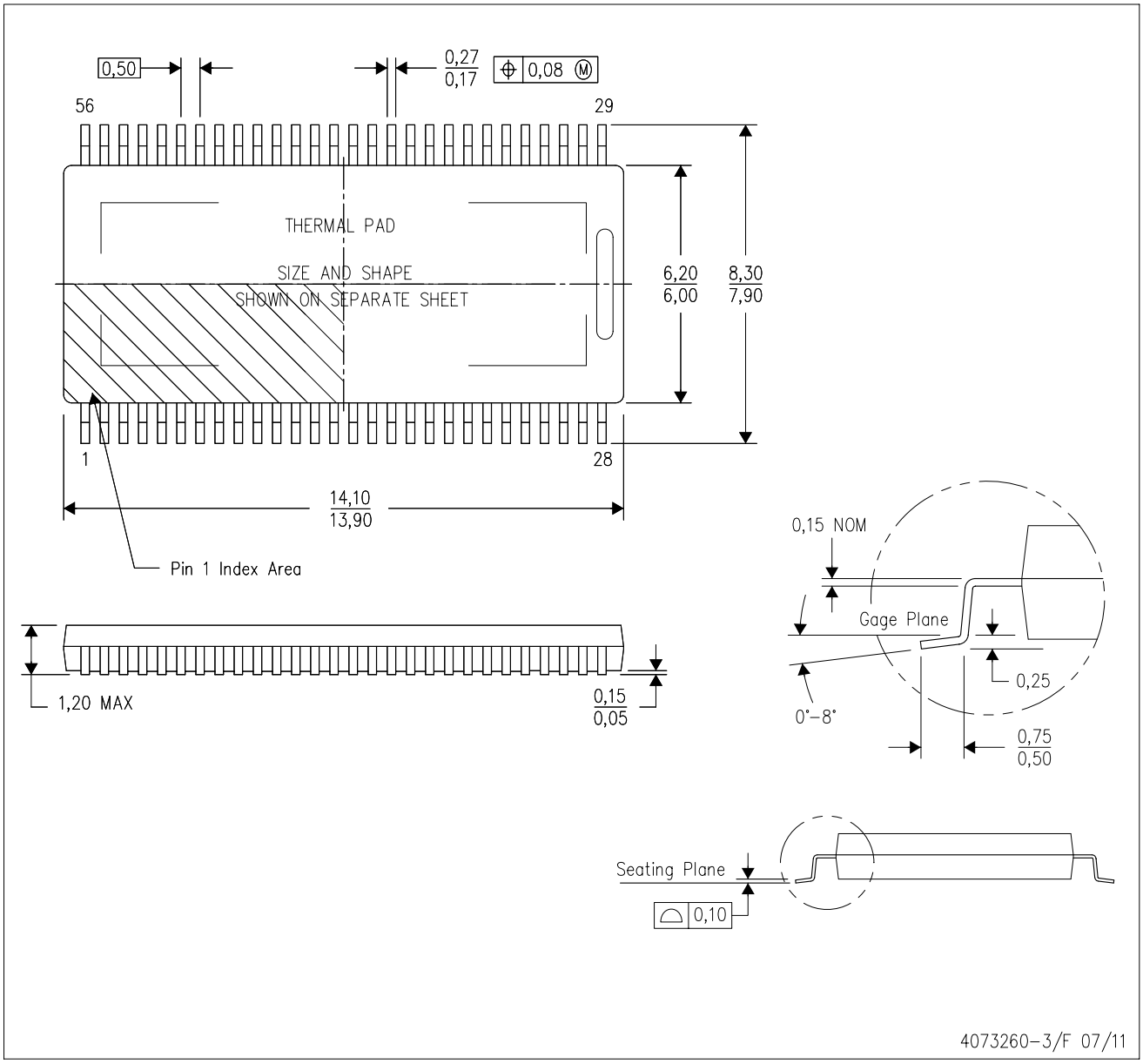

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

DFD (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

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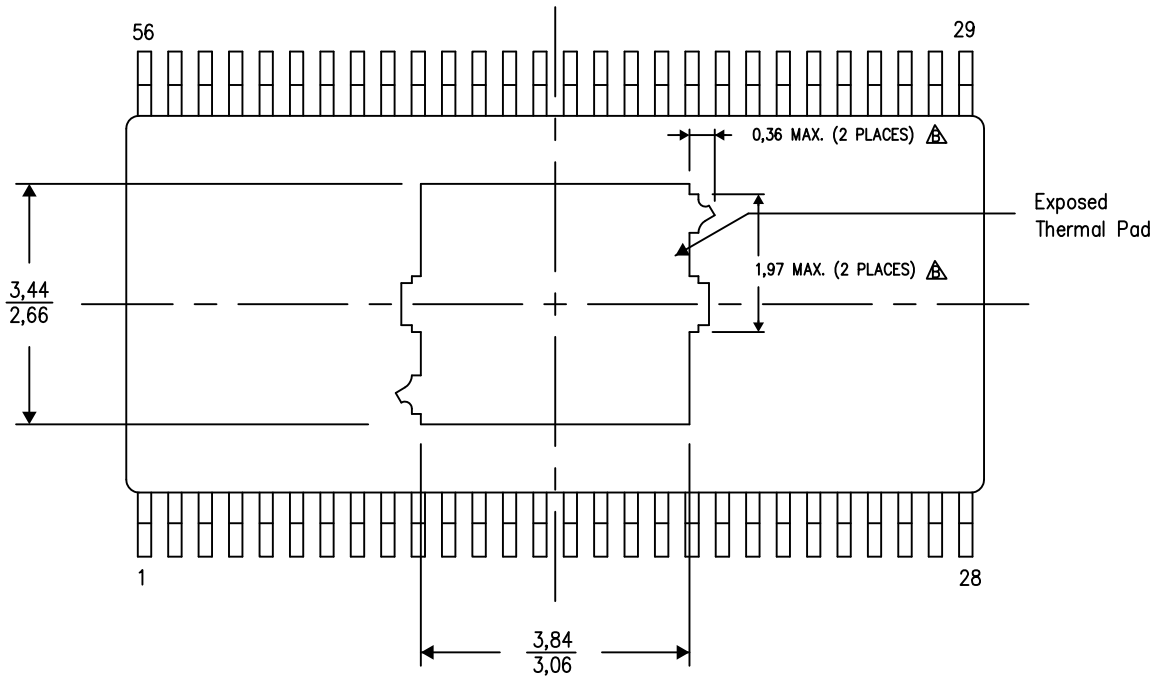
For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4210501–2/G 07/12

NOTES: A. All linear dimensions are in millimeters

B Keep–out features are identified to prevent board routing interference.
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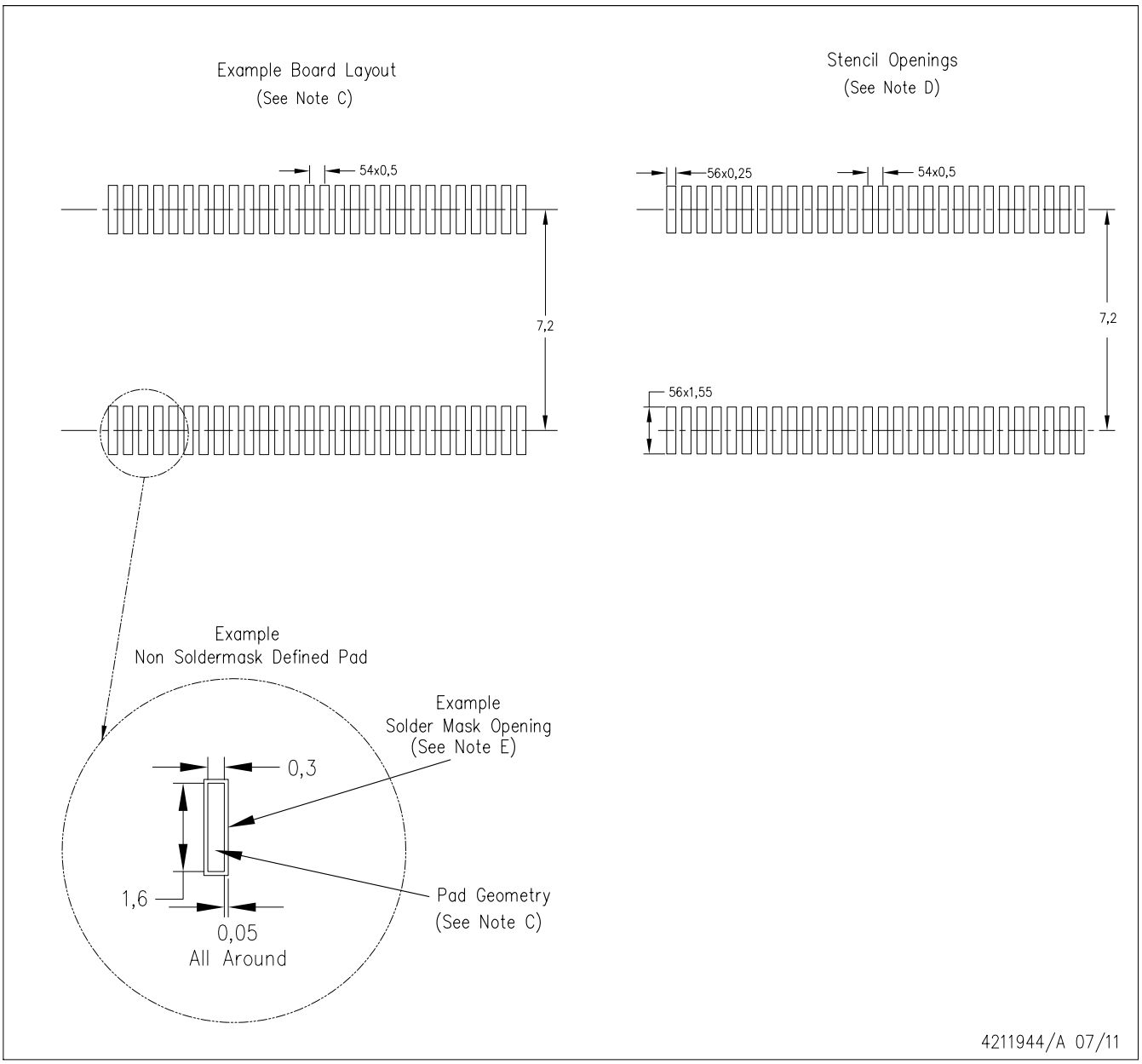

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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