TPS2388 IEEE 802.3at 8 通道以太网供电 PSE 控制器

1 特性

- 完全符合 IEEE 802.3at 标准
- 端口重映射
- 1 位和 3 位快速端口关断输入
- “永不受骗”4 点检测
- 1 类和 2 类 PD 分类
- 具有折返功能的可编程电流限制
- 直流断开检测
- 灵活的处理器控制运行模式
  - 半自动
  - 手动
- 14 位端口电流和电压监控
  - 100ms 滚动端口电流平均
  - 2% 电流感应精度
  - 具有开尔文感应功能的 0.255Ω 感应电阻器
- I^2C 通信
  - 用于实现失效防护运行的 I^2C 看门狗
  - 可选择 8 位和 16 位访问模式
- –40°C 至 125°C 工作温度
- 56 引线 VQFN 封装

2 应用

- 企业交换机和路由器
- SoHo 交换机和路由器
- PoE 直通电源模块
- 网络录像机 (NVR)

3 说明

TPS2388 是一款 8 通道电源设备 (PSE) 控制器，旨在根据 IEEE 802.3at-2012 标准（或 802.3at）向以太网电缆提供电力。PSE 控制器可以检测具有有效签名的通电器件 (PD)，根据分类确定电源要求，以及通过单事件（1 类）或双事件（2 类）物理分类应用电源。TPS2388 还能够灵活地支持 UPoE 和其他非标准负载。

利用端口重映射和器件引脚，设计人员可以实现 2 层 PCB 设计并简化从上一代 PSE 器件进行的迁移。借助外部 FET 架构，设计人员可以进一步平衡尺寸、效率、散热和解决方案成本要求。电流折返可在启动和过载情况期间降低外部 MOSFET 上的热应力，从而允许使用较便宜的 FET。

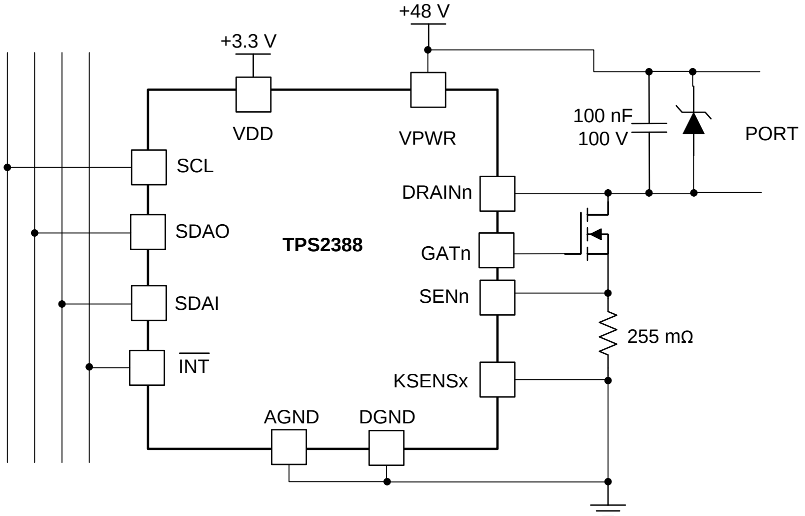
快速关断 (OSS) 输入可以为要求立即禁用多个端口的应用 提供多达八个级别的逐端口关断。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TPS2388	VQFN (56)	8.00mm x 8.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化电路原理图



Note: Only port n shown

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

日期	修订版本	说明
2017 年 8 月	*	首次公开发布的产品说明书。

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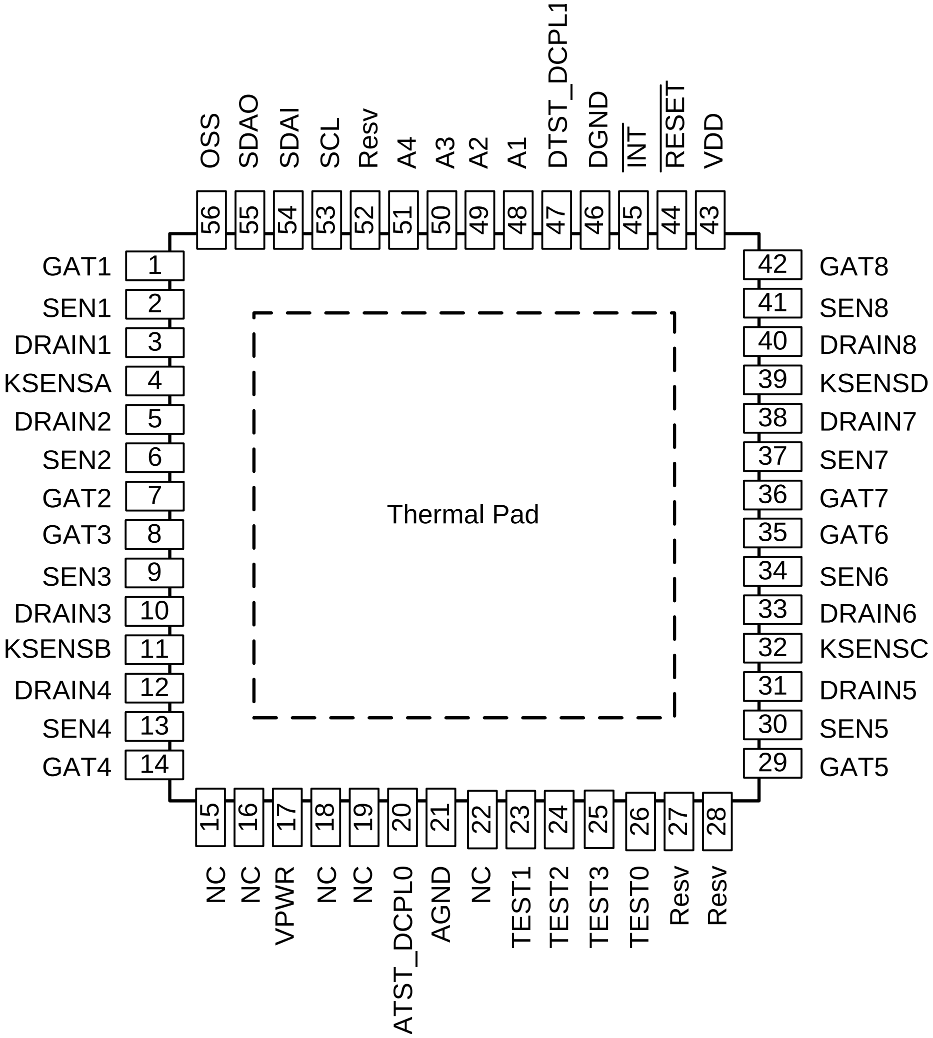
5 Pin Configuration and Functions

RTQ Package
VQFN 56 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1-4	48–51	I	I^2C A1-A4 address lines. These pins are internally pulled up to VDD.
AGND	21	—	Analog ground. Connect to GND plane and exposed thermal pad.
ATST_DCPL0	20	O	Used for internal test purposes, no bypass capacitor is needed.
DGND	46	—	Digital ground. Connect to GND plane and exposed thermal pad.
DRAIN1-8	3, 5, 10, 12, 31, 33, 38, 40	I	Port 1-8 output voltage monitor.
DTST_DCPL1	47	O	Used for internal test purposes, no bypass capacitor is needed.
GAT1-8	1, 7, 8, 14, 29, 35, 36, 42	O	Port 1-8 gate drive output.
$\overline{\text{INT}}$	45	O	Interrupt output. This pin asserts low when a bit in the interrupt register is asserted. This output is open-drain.
KSENSA/B	4, 11	I	Kelvin point connection for SEN1-4
KSENSC/D	32, 39	I	Kelvin point connection for SEN5-8

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	15, 16, 18, 19	O	No connect pins. These pins are internally biased at 1/3 and 2/3 of VPWR in order to control the voltage gradient from VPWR. Leave open.
	22	—	No connect pin. Leave open.
OSS	56	I	Port 1-8 fast shutdown. This pin is internally pulled down to DGND.
Thermal pad	—	—	The DGND and AGND terminals must be connected to the exposed thermal pad for proper operation.
$\overline{\text{RESET}}$	44	I	Reset input. When asserted low, the TPS2388 is reset. This pin is internally pulled up to VDD.
Resv	27, 28, 52	—	Reserved. No connect pins. Leave open.
SCL	53	I	Serial clock input for I^2C bus.
SDAI	54	I	Serial data input for I^2C bus. This pin can be connected to SDAO for non-isolated systems.
SDAO	55	O	Serial data output for I^2C bus. This pin can be connected to SDAI for non-isolated systems. This output is open-drain.
SEN1-8	2, 6, 9, 13, 30, 34, 37, 41	I	Port 1-8 current sense input.
TEST0-3	23, 24, 25, 26	I/O	Used internally for test purposes only. Leave open.
VDD	43	—	Digital supply. Bypass with 0.1 µF to DGND pin.
VPWR	17	—	Analog 48-V positive supply. Bypass with 0.1 µF to AGND pin.

5.1 Detailed Pin Description

The following descriptions refer to the pinout and the functional block diagram.

DRAIN1-DRAIN8: Port 1-8 output voltage monitor and detect sense. Used to measure the port output voltage, for port voltage monitoring, port power good detection and foldback action. Detection probe currents also flow into this pin.

The TPS2388 uses an innovative 4-point technique to provide reliable PD detection. The discovery is performed by sinking two different current levels via the DRAINn pin, while the PD voltage is measured from VPWR to DRAINn. The 4-point measurement provides the capability to avoid powering a capacitive or legacy load. Also, while in semiauto mode, if prior to starting a new detection cycle the port voltage is >2.5 V, an internal 100-kΩ resistor is connected in parallel with the port and a 400-ms detect backoff period is applied to allow the port capacitor to be discharged before the detection cycle starts.

There is an internal resistor between each DRAINn pin and VPWR in any operating mode except during detection or while the port is ON. If the port n is not used, DRAINn can be left floating or tied to AGND.

GAT1-GAT8: Port 1-8 gate drive output is used for external N-channel MOSFET gate control. At port turn on, it is driven positive by a low current source to turn the MOSFET on. GATn is pulled low whenever any of the input supplies are low or if an overcurrent timeout has occurred. GATn is also pulled low if its port is turned off by use of manual shutdown inputs. Leave floating if unused.

For a robust design, a current foldback function limits the power dissipation of the MOSFET during low resistance load or a short-circuit event. During inrush, the foldback mechanism measures the port voltage across VPWR and DRAINn to reduce the current limit threshold as shown in Figure 17.

When I_{CUT} threshold is exceeded while a port is on, a timer starts. During that time, linear current limiting ensures the current does not exceed I_{LIM} combined with current foldback action. When the timer reaches its t_{OVLD} (or t_{START} if at port turn on) limit, the part shuts off. When the port current goes below I_{CUT}, the counter counts down at a rate 1/16th of the increment rate and it must reach a count of 0 before the port can be turned on again.

The fast overload protection is for major faults like a direct short. This forces the MOSFET into current limit in less than a microsecond.

The circuit leakage paths between the GATn pin and any nearby DRAINn pin, GND or Kelvin point connection must be minimized (<250 nA), to ensure correct MOSFET control.

$\overline{\text{INT}}$: This interrupt output pin asserts low when a bit in the interrupt register is asserted. This output is open-drain.

KSENSA, KSENSB, KSENSC, KSENSD: Kelvin point connection used to perform a differential voltage measurement across the associated current sense resistors.

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Detailed Pin Description (continued)

Each KSENS is shared between two neighbor SEN pins as following: KSENSA with SEN1 and SEN2, KSENSB with SEN3 and SEN4, KSENSC with SEN5 and SEN6, KSENSD with SEN7 and SEN8. To optimize the accuracy of the measurement, take care with the PCB layout to minimize the impact of the PCB traces' resistance.

OSS: Fast shutdown, active high. This pin is internally pulled down to DGND, with an internal 1-µs to 5-µs deglitch filter.

The Port Power Priority/ICUT Disable register is used to determine which port is shut down in response to an external assertion of the OSS fast shutdown signal. The turn off procedure is similar to a port reset using Reset command (1Ah register).

$\overline{\text{RESET}}$: Reset input, active low. When asserted, the TPS2388 resets, turning off all ports and forcing the registers to their power-up state. This pin is internally pulled up to VDD, with internal 1-µs to 5-µs deglitch filter. The designer can use an external RC network to delay the turn-on. There is also an internal power-on-reset which is independent of the $\overline{\text{RESET}}$ input.

NOTE

During the first 5 ms after $\overline{\text{RESET}}$ has been asserted, if a port is turned on using the Power Enable command (0x19), TI recommends to wait for the expiration of that 5-ms initial period before sending any subsequent Detect/Class Restart or Detect/Class Enable command.

SCL: Serial clock input for I^2C bus.

SDAI: Serial data input for I^2C bus. This pin can be connected to SDAO for non-isolated systems.

SDAO: Open-drain I^2C bus output data line. Requires an external resistive pull-up. The TPS2388 uses separate SDAO and SDAI lines to allow optoisolated I^2C interface. SDAO can be connected to SDAI for non-isolated systems.

A4-A1: I^2C bus address inputs. These pins are internally pulled up to VDD. See *Pin Status Register* for more details.

SEN1-8: Port current sense input relative to KSENSn (see KSENSn description). A differential measurement is performed using KSENSA-D Kelvin point connection. Monitors the external MOSFET current by use of a 0.255-Ω current sense resistor connected to DGND. Used by current foldback engine and also during classification. Can be used to perform load current monitoring via A/D conversion.

Note that a classification is done while using the external MOSFET so that doing a classification on more than one port at same time is possible without overdissipation in the TPS2388. For the current limit with foldback function, there is an internal 2-µS analog filter on the SEN1-8 pins to provide glitch filtering. For measurements through an A/D converter, an anti-aliasing filter is present on the SEN1-8 pins. This includes the port-powered current monitoring, port policing, and DC disconnect.

If the port is not used, tie SENn to AGND.

VDD: 3.3-V logic power supply input.

VPWR: High voltage power supply input. Nominally 48 V.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VPWR	–0.3	70	V
	VDD	–0.3	4	V
	OSS, $\overline{\text{RESET}}$, A1-A4	–0.3	4	V
	SEN1-8, (2) KSENSA, KSENSB, KSENSC, KSENSD	–0.3	3	V
Output voltage	GATE1-8 (3) (4)	–0.3	12	V
Voltage	SDAI, SDAO (5) , SCL, $\overline{\text{INT}}$	–0.3	4	V
	DRAIN1-8 (5) (6)	–0.3	70	V
	TEST0-3, ATST_DCPL0, DTST_DCPL1 (5)	–0.3	4	V
	AGND	–0.3	0.3	V
Sink current	$\overline{\text{INT}}$, SDAO		20	mA
Lead temperature 1.6 mm (1/16-inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) SEN1-8 are tolerant to 15-V transients to avoid fault propagation when a MOSFET fails in short-circuit
(3) Application of voltage is not implied; these are internally driven pins.
(4) If the external MOSFET fails short between its drain and gate, the GATE pin may internally permanently disconnect to prevent cascade damage. The three other ports continue to operate.
(5) Do not apply external voltage sources directly
(6) Short transients (µs range) up to 80 V are allowed

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}		3	3.3	3.6	V
V_{VPWR}		44	48	57	V
	Voltage slew rate on VPWR			1	V/µs
T_J	Operating junction temperature	–40		125	°C
T_A	Operating free-air temperature	–40		85	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS2388	UNIT
		VQFN (56 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.7	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	3.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C unless otherwise noted. V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA, KSENSB, KSENSC, and KSENSD connected to AGND, and all outputs are unloaded, unless otherwise noted. PoEPn = 0. Positive currents are into pins. R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25°C. All voltages are with respect to AGND, unless otherwise noted. Operating registers loaded with default values, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VPWR						
I_{VPWR}	VPWR current consumption	V_{VPWR} = 50 V		10	12.5	mA
		V_{VPWR} < 8 V			100	µA
V_{UVLOPW_F}	VPWR UVLO falling threshold		14.5		17.5	V
V_{UVLOPW_R}	VPWR UVLO rising threshold		15.5		18.5	V
V_{PUV_F}	VPWR undervoltage falling threshold	VPUV threshold	25	26.5	28	V
TOTAL DEVICE POWER DISSIPATION						
P_T	VPWR and VDD consumption	V_{VPWR} = 50 V			0.67	W
INPUT SUPPLY VDD						
I_{VDD}	VDD Current consumption			6	12	mA
V_{UVDD_F}	VDD UVLO falling threshold	For port deassertion	2.1	2.25	2.4	V
V_{UVDD_R}	VDD UVLO rising threshold		2.45	2.6	2.75	V
V_{UVDD_HYS}	Hysteresis VDD UVLO			0.35		V
V_{UVW_F}	VDD UVLO warning threshold		2.6	2.8	3.0	V
DETECTION						
I_{DISC}	Detection current	First detection point, V_{VPWR} – V_{DRAINn} = 0 V	145	160	190	µA
		Second detection point, V_{VPWR} – V_{DRAINn} = 0 V	235	270	300	
		High-current detection point, V_{VPWR} – V_{DRAINn} = 0 V	490	540	585	
V_{detect}	Open-circuit detection voltage	V_{VPWR} – V_{DRAINn}	23.5	26	29	V
R_{REJ_LOW}	Rejected resistance low range		0.86		15	kΩ
R_{REJ_HI}	Rejected resistance high range		33		100	kΩ
R_{ACCEPT}	Accepted resistance range		19	25	26.5	kΩ
R_{SHORT}	Shorted port threshold				360	Ω
R_{OPEN}	Open port threshold		400			kΩ

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C unless otherwise noted. V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA, KSENSB, KSENSC, and KSENSD connected to AGND, and all outputs are unloaded, unless otherwise noted. PoEPn = 0. Positive currents are into pins. R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25°C. All voltages are with respect to AGND, unless otherwise noted. Operating registers loaded with default values, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLASSIFICATION						
V_{CLASS}	Classification voltage	V_{VPWR} – V_{DRAINn}, V_{SENn} ≥ 0 mV, I_{port} ≥ 180 µA	15.5	18.5	20.5	V
I_{CLASS_Lim}	Classification current limit	VVPWR – VDRAINn = 0 V	65	75	90	mA
I_{CLASS_TH}	Classification threshold current	Class 0-1	5		8	mA
		Class 1-2	13		16	mA
		Class 2-3	21		25	mA
		Class 3-4	31		35	mA
		Class 4-Class overcurrent	45		51	mA
V_{MARK}	Mark voltage	4 mA ≥ Iport ≥ 180 µA, VVPWR – VDRAINn	7		10	V
I_{MARK_Lim}	Mark sinking current limit	V_{VPWR} – V_{DRAINn} = 0 V	10	70	90	mA
GATE						
V_{GOH}	Gate drive voltage	V_{GATEn} , I_{GATE} = –1 µA	10		12.5	V
I_{GO-}	Gate sinking current with Power-on Reset, OSS detected or port turn off command	V_{GATEn} = 5 V	60	100	190	mA
$I_{GO\ short–}$	Gate sinking current with port short-circuit	V_{GATEn} = 5 V, V_{SENn} ≥ V_{short} (or Vshort2X if 2X mode)	60	100	190	mA
I_{GO+}	Gate sourcing current	V_{GATEn} = 0V	39	50	63	µA
DRAIN INPUT						
V_{PGT}	Power Good threshold	Measured at V_{DRAINn}	1.0	2.13	3	V
V_{SHT}	Shorted FET threshold	Measured at V_{DRAINn}	4	6	8	V
R_{DRAIN}	Resistance from DRAINn to VPWR	Any operating mode except during detection or while the port is ON, including in device RESET state	80	100	190	kΩ
I_{DRAIN}	DRAINn pin bias current	V_{VPWR} – V_{DRAINn} = 30 V, port ON		75	120	µA
A/D CONVERTER						
t_{CONV}	Conversion time, current measurement	All ranges, each port	0.64	0.8	0.96	ms
t_{CONV_V}	Conversion time, voltage measurement	All ranges, each port	0.82	1.03	1.2	ms
t_{GAP}	Gap between adjacent current measurement integrations				5% × t_{CONV}	ms
	Gap between adjacent current averaged results				5% × t_{INT_CUR}	ms
ADC_{BW}	ADC integration bandwidth (–3 db)	Current measurement		320		Hz
t_{INT_CUR}	Integration (averaging) time, current	Each port, port ON current	82	102	122	ms
t_{INT_DET}	Integration (averaging) time, detection		13.1	16.6	20	ms
t_{INT_portV}	Integration (averaging) time, port voltage	Port powered	3.25	4.12	4.9	ms
t_{INT_inV}	Integration (averaging) time, input voltage		3.25	4.12	4.9	ms
	Powered port voltage conversion scale factor and accuracy	At V_{VPWR} – V_{DRAINn} = 57 V	15097	15565	16032	Counts
		At V_{VPWR} – V_{DRAINn} = 44 V	11654	12015	12375	Counts
	Powered port current conversion scale factor and accuracy	At port current = 770 mA	12363	12616	12868	Counts
		At port current = 7.5 mA	100	123	150	Counts
	Input voltage conversion scale factor and accuracy	At V_{VPWR} = 57 V	15175	15565	15955	Counts
		At V_{VPWR} = 44 V	11713	12015	12316	Counts
δ_V/V_{port}	Voltage reading accuracy	At 44 to 57 V	–3%		3%	
σ_V	Voltage reading repeatability	Full scale reading	–18		18	mV
δ_I/I_{port}	Current reading accuracy	At 50 mA	–3%		3%	
		At 770 mA	-2%		2%	
σ_I	Current reading repeatability	Full scale reading	–7.5		7.5	mA

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C unless otherwise noted. V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA, KSENSB, KSENSC, and KSENSD connected to AGND, and all outputs are unloaded, unless otherwise noted. PoEPn = 0. Positive currents are into pins. R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25°C. All voltages are with respect to AGND, unless otherwise noted. Operating registers loaded with default values, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
δ_R/R_{port}	Resistance reading accuracy	15 kΩ ≤ R_{port} ≤ 33 kΩ, C_{port} ≤ 0.25 µF, at 44 to 57 V	–7%		7%	
PORT CURRENT SENSE						
V_{CUT}	I_{CUT} limit	V_{DRAINn} = 0 V, POL(3:0) = 0001b	9.6	10.2	10.8	mV
		V_{DRAINn} = 0 V, POL(3:0) = 0010b	14.53	15.3	16.06	
		V_{DRAINn} = 0 V, POL(3:0) = 0111b	38.76	40.8	42.84	
		V_{DRAINn} = 0 V, POL(3:0) = 1111b	77.5	81.6	85.6	
		V_{DRAINn} = 0 V, POL(3:0) = 0000b, PoEPn = 1	77.5	81.6	85.6	
		V_{DRAINn} = 0 V, POL(3:0) = 1111b, PoEPn = 1	222.8	234.6	246.3	
δ_V/V_{police}	Police setting resolution		–6.3%		6.3%	
δ_{icut}/I_{CUT}	I_{CUT} tolerance	All settings except POL(3:0) = 0000b and 0001b while PoEPn = 0	–5%		5%	
V_{Inrush}	I_{Inrush} limit, 1x or 2x mode	V_{VPWR} – V_{DRAINn} = 1 V	10	23	31	mV
		V_{VPWR} – V_{DRAINn} = 10 V	20	33	46	
		V_{VPWR} – V_{DRAINn} = 30 V	102		114.7	
		V_{VPWR} – V_{DRAINn} = 55 V	102		114.7	
V_{LIM}	I_{LIM} limit in 1x mode	V_{DRAINn} = 1 V	102		114.7	mV
		V_{DRAINn} = 13 V	102		114.7	
		V_{DRAINn} = 30 V	15	23	31	
		V_{DRAINn} = 48 V	15	23	31	
V_{LIM2X}	I_{LIM} limit in 2X mode (PoEPn = 1)	V_{DRAINn} = 1 V	260	270.3	285	mV
		V_{DRAINn} = 10 V	127	140	153	
		V_{DRAINn} = 30 V	15	23	31	
		V_{DRAINn} = 48 V	15	23	31	
V_{short}	I_{short} threshold in 1X mode and during inrush	Threshold for GATE to be less than 1 V, 2 µS after application of pulse	234		306	mV
$V_{short2X}$	I_{short} threshold in 2X mode		357		408	
I_{bias}	Sense pin bias current	Port ON or during class	–2.5		0	µA
V_{IMIN}	DC disconnect threshold		1.275		2.55	mV
DIGITAL INTERFACE AT V_{VDD} = 3.3 V						
V_{IH}	Digital input high		2.1			V
V_{IL}	Digital input low				0.9	V
V_{IT_HYS}	Input voltage hysteresis (SCL, SDAI, A1-A4, $\overline{\text{RESET}}$, OSS)		0.17			V
V_{OL}	Digital output Low, SDAO	At 9 mA			0.4	V
	Digital output Low, $\overline{\text{INT}}$	At 3 mA			0.4	V
R_{pullup}	Pullup resistor to VDD	$\overline{\text{RESET}}$, A1-A4, TEST0	30	50	80	kΩ
$R_{pulldown}$	Pulldown resistor to DGND	OSS	30	50	80	kΩ
		TEST1, 2	30	50	80	
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature	Temperature rising	135	146		°C
	Hysteresis			7		°C

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6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency		10		400	kHz
t_{LOW}	LOW period of the clock		1.3			µs
t_{HIGH}	HIGH period of the clock		0.6			µs
t_{fo}	SDAO output fall time	SDAO, 2.3 → 0.8 V, Cb = 10 pF, 10 kΩ pull-up to 3.3 V	21		250	ns
		SDAO, 2.3 → 0.8 V, Cb = 400 pF, 1.3 kΩ pull-up to 3.3 V	21		250	ns
C_{I2C}	SCL capacitance				10	pF
C_{I2C_SDA}	SDAI, SDAO capacitance (each)				6	pF
$t_{SU,DATW}$	Data set-up time (Write operation)		100			ns
$t_{SU,DATR}$	Data set-up time (Read operation)	SDAO, Cb = 10 pF, 1.3 kΩ pull-up to 3.3V	600			ns
$t_{HD,DATW}$	Data hold time (Write operation)		0			ns
$t_{HD,DATR}$	Data hold time (Read operation)		150		600	ns
t_{fSDA}	Input fall times of SDAI	2.3 → 0.8 V	20		250	ns
t_{rSDA}	Input rise times of SDAI	0.8 → 2.3 V	20		300	ns
t_r	Input rise time of SCL	0.8 → 2.3 V	20		300	ns
t_f	Input fall time of SCL	2.3 → 0.8 V	20		200	ns
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{HD,STA}$	Hold time after (repeated) Start condition		0.6			µs
$t_{SU,STA}$	Repeated Start condition set-up time		0.6			µs
$t_{SU,STO}$	Stop condition set-up time		0.6			µs
t_{FLT_INT}	Fault to $\overline{\text{INT}}$ assertion	Time to internally register an Interrupt fault, from port turn off		50	500	µs
t_{DG}	Suppressed spike pulse width, SDAI and SCL		50			ns
t_{RDG}	$\overline{\text{RESET}}$ input minimum pulse width (deglitch time)				5	µs
t_{bit_OSS}	3-bit OSS bit period	MbitPrty = 1	24	25	26	µs
t_{OSS_IDL}	Idle time between consecutive shutdown code transmission in 3-bit mode	MbitPrty = 1	48	50		µs
t_{r_OSS}	Input rise time of OSS in 3-bit mode	0.8 → 2.3 V, MbitPrty = 1	1		300	ns
t_{f_OSS}	Input fall time of OSS in 3-bit mode	2.3 → 0.8 V, MbitPrty = 1	1		300	ns
t_{WDT_I2C}	I^2C Watchdog trip delay		1.1	2.2	3.3	s

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6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
δI_{fault}	Duty cycle of Iport with current fault		5.5%		6.7%	
t_{OVLD}	ICUT time limit (DCUTn = 0)	TOVLD = 00	50		70	ms
		TOVLD = 01	25		35	
		TOVLD = 10	100		140	
		TOVLD = 11	200		280	
t_{ICUT_INT}	ICUT Interrupt time limit when ICUT is disabled (DCUTn = 1)(1)	I_{CUT} limit exceeded but not I_{LIM}, TLIM = 01, PoEPn = 1		$t_{LIM/2}$	$t_{LIM/2}$ + 6	ms
t_{LIM}	ILIM time limit		50		70	ms
		TLIM = 00, PoEPn = 1	50		70	
		TLIM = 01, PoEPn = 1	14.5	15	15.75	
		TLIM = 10, PoEPn = 1	11.5	12	12.5	
		TLIM = 11, PoEPn = 1	9.5	10	10.5	
t_{START}	Maximum current limit duration in port start-up	TSTART = 00	50		70	ms
		TSTART = 01	25		35	
		TSTART = 10	100		140	
t_{DET}	Detection duration, 4-point discovery	Time to complete a detection	275	350	425	ms
t_{DET_BOFF}	Detect backoff pause between discovery attempts	$V_{VPWR} – V_{DRAINn}$ > 2.5 V	300	400	500	ms
		$V_{VPWR} – V_{DRAINn}$ < 2.5 V	15		100	
t_{DET_DLY}	Detection delay	From command or PD attachment to port detection complete			590	ms
t_{CLE}	Classification duration, first and second class event	Semiauto mode. From detection complete	6.5		12	ms
t_{pdc}	Classification duration, 1-event physical layer class timing	Semiauto mode. From detection complete	6.5		12	ms
		Manual mode. From beginning of class	6.5		14	
t_{ME}	Mark Duration, first and second mark event	Semiauto mode. From Class 4 complete	6		12	ms
t_{pon}	Port Power-On delay, semiauto mode	From end of detection to port turn on using IEEE power enable			200	ms
	Port Power-On delay, manual mode	From port turn on command to port turn on completed, four ports			4	ms
t_{RESET}	Reset time duration from $\overline{\text{RESET}}$ pin		1		5	µs
t_{ed}	Error delay timing. Delay before next attempt to power a port following power removal due to error condition	ICUT , ILIM or IInrush fault, semiauto mode	0.8	1	1.2	s
t_{MPDO}	PD maintain power signature dropout time limit	TMPDO = 00	300		400	ms
		TMPDO = 01	75		100	
		TMPDO = 10	150		200	
		TMPDO = 11	600		800	
t_{MPS}	PD maintain power signature time for validity		13	15	17	ms
$t_{D\_off\_OSS}$	Gate turn off time from 1-bit OSS input	From OSS to V_{GATEn} < 1 V, V_{SENn} = 0 V, MbitPrty = 0	1		5	µs
t_{OSS_OFF}	Gate turn off time from 3-bit OSS input	From Start bit falling edge to V_{GATEn} < 1 V, V_{SENn} = 0 V, MbitPrty = 1	72		104	µs
$t_{P\_off\_CMD}$	Gate turn off time from port off command	From port off command to V_{GATEn} < 1 V, V_{SENn} = 0 V			300	µs
$t_{P\_off\_RST}$	Gate turn off time with $\overline{\text{RESET}}$	From $\overline{\text{RESET}}$ low to V_{GATEn} < 1 V, V_{SENn} = 0 V	1		5	µs
$t_{D\_off\_SEN}$	Gate turn off time from SENn input	V_{DRAINn} = 1 V , From V_{SENn} pulsed to 0.425 V			0.9	µs
	Gate turn off time from SENn input (PoEPn = 1)	V_{DRAINn} = 1 V , From V_{SENn} pulsed to 0.62 V			0.9	
t_{POR}	Device power-on reset delay				20	ms

(1) The t_{ICUT_INT} maximum value shown in the table only applies to a low percentage (< 10%) of occurence. The rest of the time, it becomes $t_{LIM}/2 + 2$ ms.

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6.8 Typical Characteristics

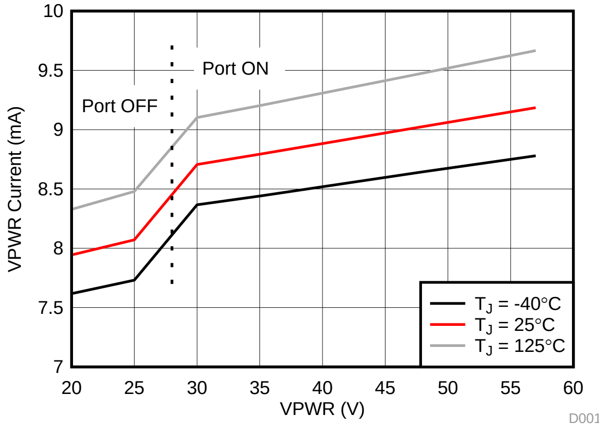

Figure 1. VPWR Current Consumption vs VPWR

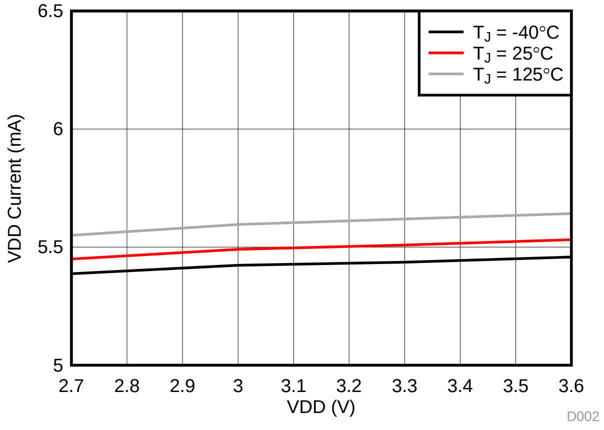

Figure 2. VDD Current Consumption vs VDD

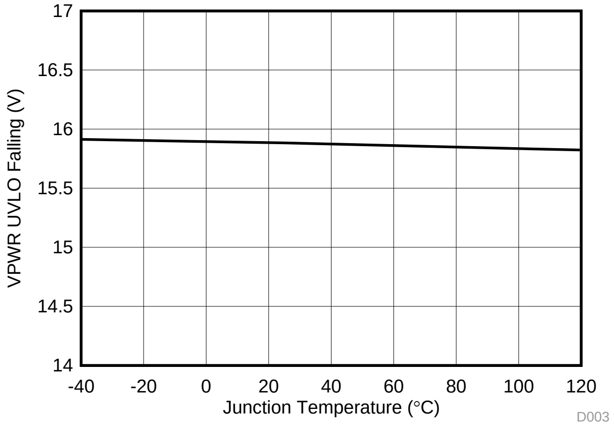

Figure 3. VPWR UVLO Falling Threshold vs Junction Temperature

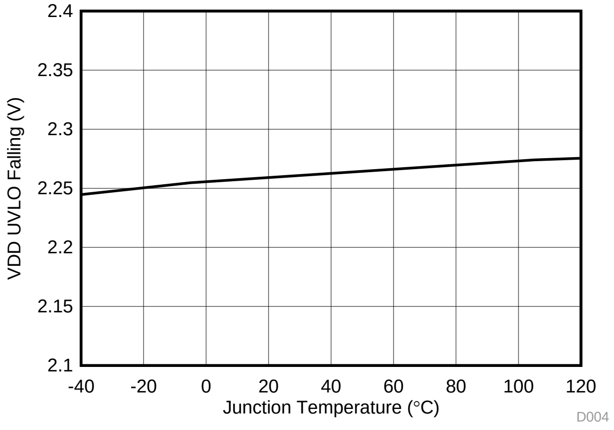

Figure 4. VDD UVLO Falling Threshold vs Junction Temperature

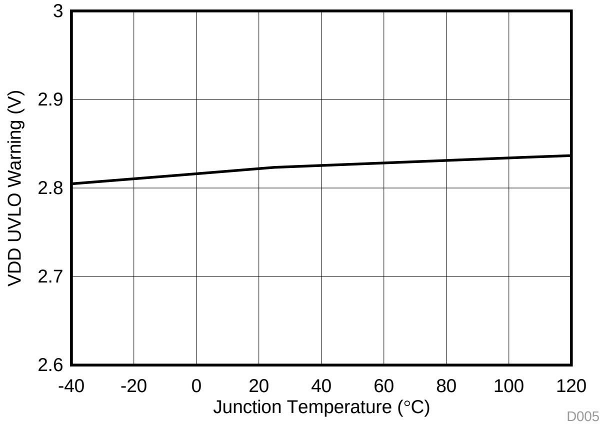

Figure 5. VDD UVLO Warning Threshold vs Junction Temperature

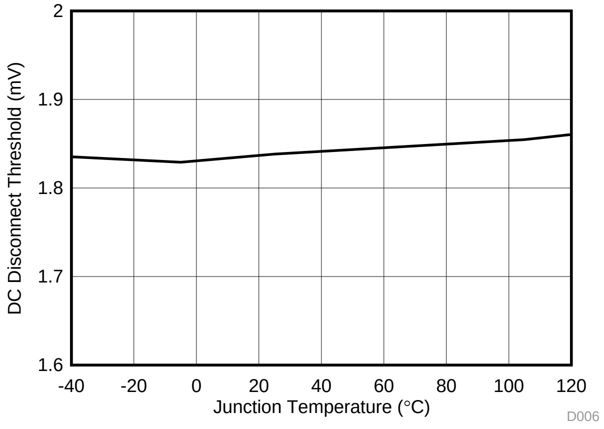

Figure 6. DC Disconnect Threshold (V_{IMIN}) vs Junction Temperature

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Typical Characteristics (continued)

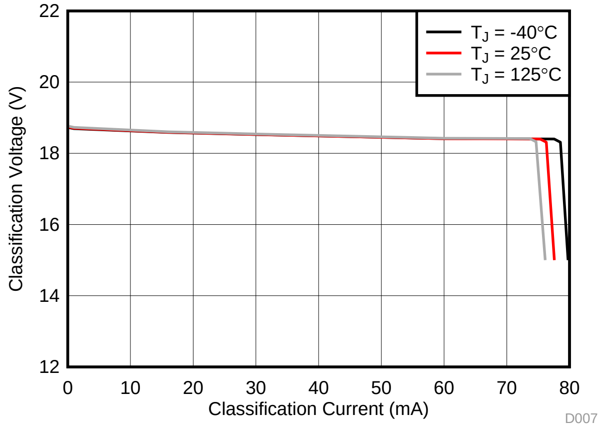

Figure 7. Classification Voltage (V_{CLASS}) vs Port Classification Current

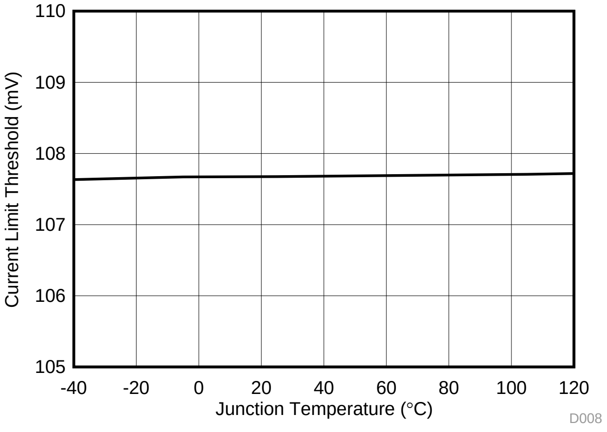

Figure 8. Current Limit 1x Threshold (V_{LIM}) vs Junction Temperature

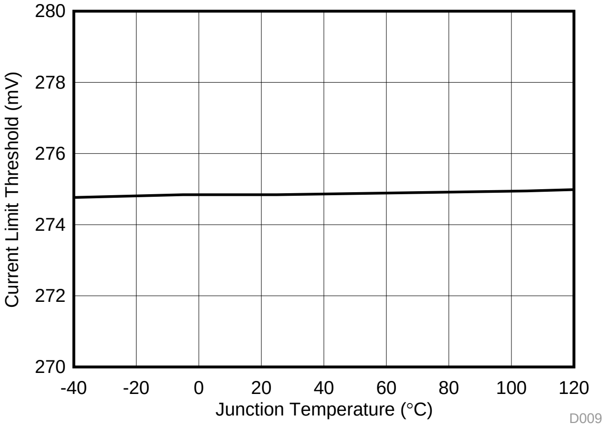

Figure 9. Current Limit 2x Threshold (V_{LIM2X}) vs Junction Temperature

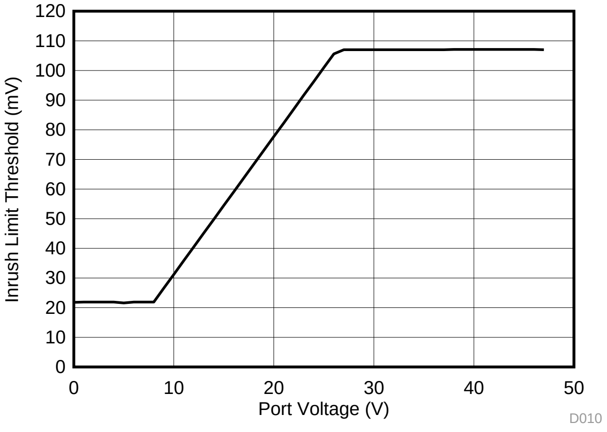

Figure 10. Inrush Current Limit Threshold (V_{Inrush}) vs Port Voltage

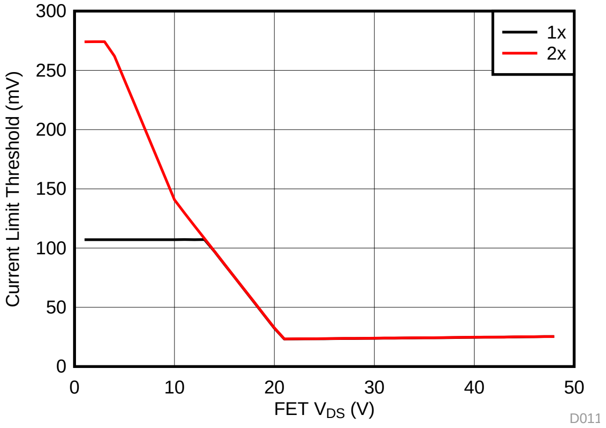

Figure 11. Foldback Current Limit Threshold (V_{LIM}, V_{LIM2X}) vs Port MOSFET Voltage

7 Parameter Measurement Information

7.1 Timing Diagrams

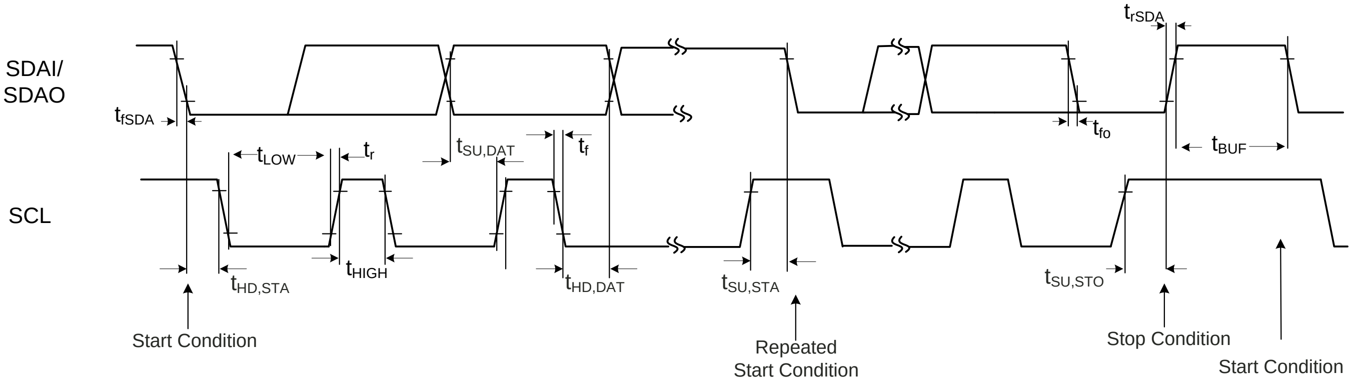

Figure 12. I²C Timings

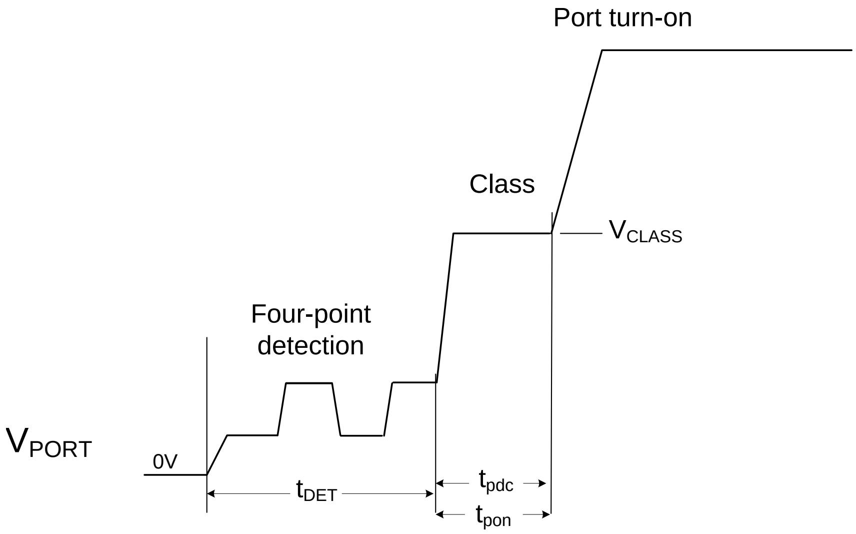

Figure 13. Detection, 1-Event Classification and Turn On

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Timing Diagrams (continued)

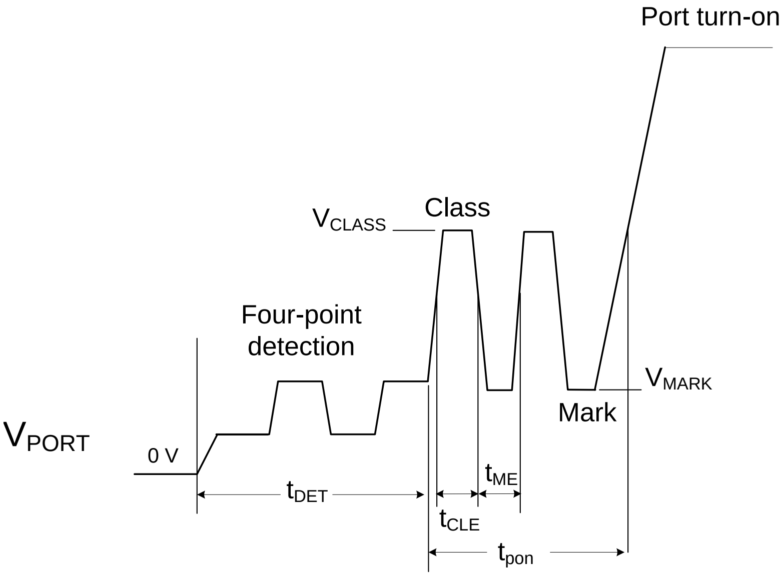

Figure 14. Detection, 2-Event Classification and Turn On

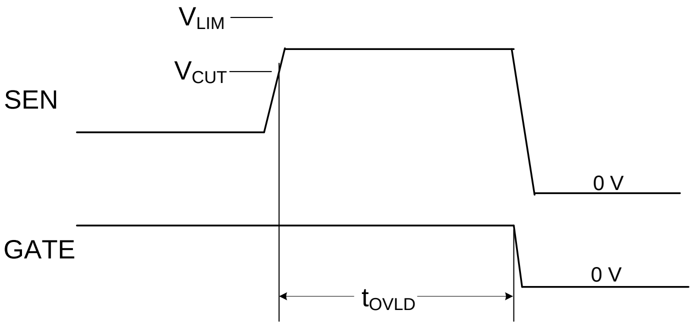

Figure 15. Overcurrent Fault Timing

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8 Detailed Description

8.1 Overview

The TPS2388 is an eight-port PSE for power over Ethernet applications. Each of the eight ports provides detection, classification, protection, and shut down in compliance with the IEEE 802.3at standard.

Basic PoE features include the following:
- Performs high-reliability 4-point load detection
- Performs classification including type-2 (two-finger) of up to Class 4 loads
- Enables power with protective foldback current limiting, and adjustable I_{CUT} threshold
- Shuts down in the event of fault loads and shorts
- Performs maintain power signature function to ensure removal of power if load is disconnected
- Undervoltage lockout occurs if VPWR falls below VPUV_F (typical 26.5 V).

Enhanced features include the following:
- Port re-mapping capability
- 8- and 16-bit access mode selectable
- 1- and 3-bit port shutdown priority
- Port turn ON command automatically supports IEEE TPON specification (0x23 register or 0x19 and 0x40 register)

Following a power-off command, disconnect, or shutdown due to a start, ICUT, or ILIM fault, the port powers down. Following port power off due to a power off command or disconnect, the TPS2388 restarts a detection cycle if commanded to do so. If the shutdown is due to a start, ICUT, or ILIM fault, the TPS2388 first enters into a cool-down period, at the end of this period the TPS2388 is able to restart the detection cycle.

Using the turn ON command supporting TPON, the TPS2388 will not automatically apply power to a port under the following circumstances:
- The detect status is not resistance valid.
- If the classification status is overcurrent, class mismatch, or unknown.

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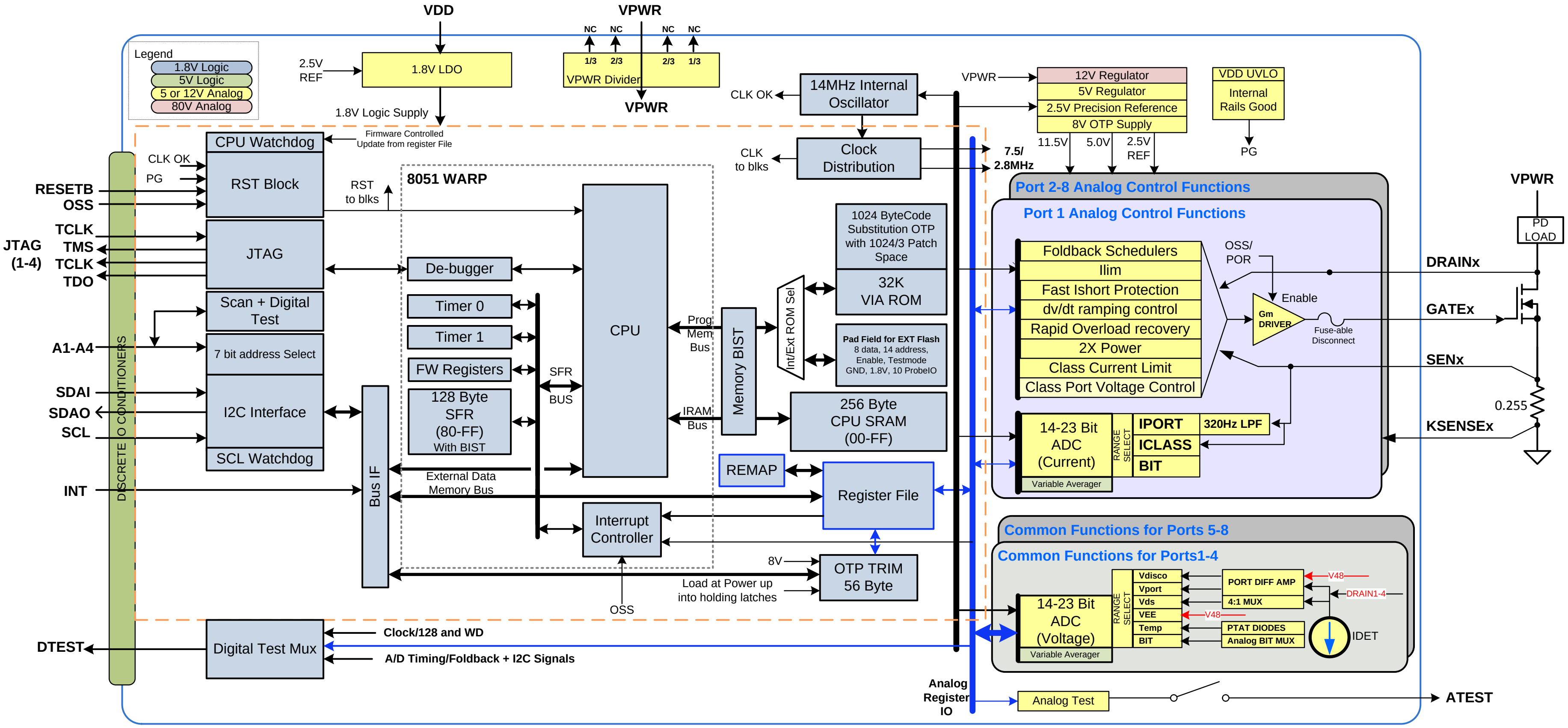
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Port Remapping

The TPS2388 provides port remapping capability, from the logical ports to the physical ports/pins.

The remapping is between any port of a 4-port group (1 to 4, 5 to 8).

The following example is applicable to 0x26 register = 00111001, 00111001b.

- Logical port 1 (5) ↔ Physical port 2 (6)
- Logical port 2 (6) ↔ Physical port 3 (7)
- Logical port 3 (7) ↔ Physical port 4 (8)
- Logical port 4 (8) ↔ Physical port 1 (5)

NOTE

The device ignores any remapping command unless all four ports are in off mode.

If the TPS2388 receives an incorrect configuration, it simply ignores the incorrect configuration and keeps the configuration unchanged. The ACK is also sent as usual at the end of communication. For example, if the same code is received for more than one port, then a read back of the Re-Mapping register (0x26) would be the last valid configuration.

Also note that if an IC reset command (1Ah register) is received, the port remapping configuration is kept unchanged. However, if there is a Power-on Reset or if the $\overline{\text{RESET}}$ pin is activated, the Re-Mapping register is reinitialized to a default value.

8.3.2 Port Power Priority

The TPS2388 supports 1- and 3-bit shutdown priority, selectable with the MbitPrty bit of General Mask register (0x17).

The 1-bit shutdown priority works with the Port Power Priority (0x15) register. An OSSn bit with a value of 1 indicates that the corresponding port will be treated as low priority, while a value of 0 corresponds to a high priority. As soon as the OSS input goes high, the low-priority ports are turned off.

The 3-bit shutdown priority works with the Multi Bit Power Priority (0x27/28) register, which holds the priority settings. A port with “000” code in this register has highest priority. Port priority reduces as the 3-bit value increases, with up to 8 priority levels. See Figure 16.

The port priority is defined as the following:

- OSS code ≤ Priority setting (0x27/28 register): OSS code turns off the port
- OSS code > Priority setting (0x27/28 register): OSS code has no impact on the port

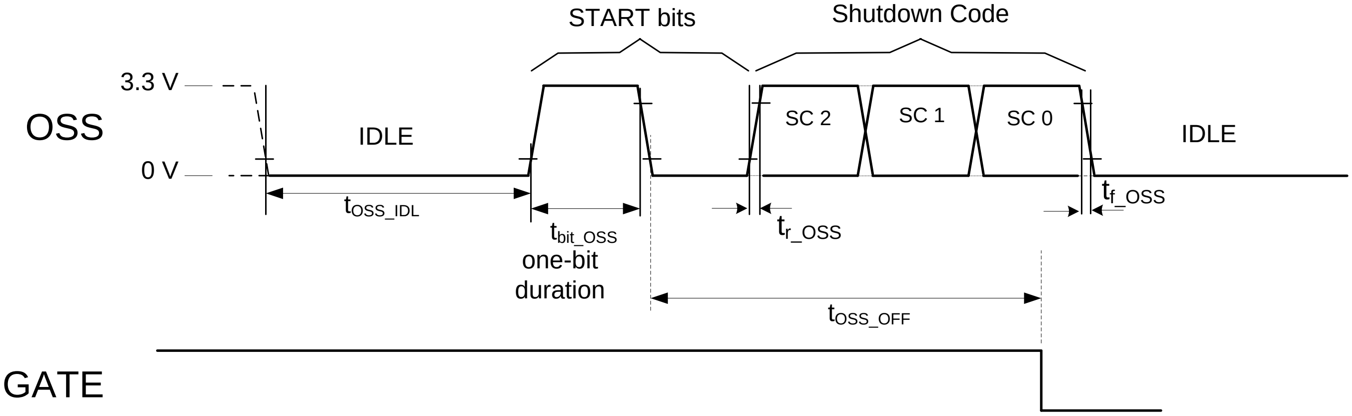


Figure 16. Multi-Bit Priority Port Shutdown if Lower-Priority Port

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Feature Description (continued)

NOTE

Prior to setting the MbitPrty bit from 0 to 1, make sure the OSS input is in the idle (low) state for a minimum of 200 µs, to avoid any port misbehavior related to loss of synchronization with the OSS bit stream.

NOTE

The OSS input has an internal 1-µs to 5-µs deglitch filter. From the idle state, a pulse with a longer duration is interpreted as a valid start bit. Ensure that the OSS signal is noise free.

8.3.3 A/D Converter

The TPS2388 features ten multi-slope integrating converters. Each of the first eight converters is dedicated to current measurement for one port and is operated independently to perform measurements in any of the following modes: classification and port powered. When the port is powered, the converter is used for current (100-ms averaged) monitoring, port policing, and DC disconnect. Each of the last two converters are shared within a group of four ports for discovery (16.6-ms averaged), port powered voltage monitoring, Power Good status, and FET short detection. It is also used for general-purpose measurements including input voltage (1 ms) and temperature.

The A/D converter type used in the TPS2388 differs from other similar types of converters in that it converts while the input signal is being sampled by the integrator, providing inherent filtering over the conversion period. The typical conversion time of the current converters is 800 µs, while it is 1 ms for the other converters. Powered-device detection is performed by averaging 16 consecutive samples providing significant rejection of noise at 50-Hz or 60-Hz line frequency. While a port is powered, digital averaging is used to provide a port current measurement integrated over a 100-ms time period. Note also that an anti-aliasing filter is present for port powered current monitoring.

NOTE

During port-powered mode, port current conversions are performed continuously. Also, in port-powered mode, the t_{START} timer must expire before any current or voltage A/D conversion can begin.

8.3.4 I^{2}C Watchdog

An I^{2}C Watchdog timer is available on the TPS2388 device. The timer monitors the I^{2}C, SCL line for clock edges. When enabled, a timeout of the watchdog resets the I^{2}C interface along with any active ports. This feature provides protection in the event of a hung software situation or I^{2}C bus hang-up by slave devices. In the latter case, if a slave is attempting to send a data bit of 0 when the master stops sending clocks, then the slave could get stuck driving the data line low indefinitely. Because the data line is being driven low, the master cannot send a STOP to clean up the bus. Activating the I^{2}C watchdog feature of the TPS2388 would clear this deadlocked condition. If the timer of 2 seconds expires, the ports latch off and the WD Status bit is set. Note that WD Status will be set even if the watchdog is not enabled. WD Status can only be cleared by a reset or writing a 0 to the WDS status bit location. The 4-bit watchdog disable field shuts down this feature when a code of 1011b is loaded. This field is preset to 1011b whenever the TPS2388 is initially powered. Also see *I2C WATCHDOG Register* for more details.

8.3.5 Foldback Protection

The TPS2388 features two types of foldback protection mechanisms for complete MOSFET protection. During inrush at port turn on, the foldback is based on the port voltage as shown in Figure 17. Note that the inrush current profile remains the same, whatever the state of the PoEPn bit in the PoE Plus register.

Feature Description (continued)

After the port has been turned on and the Power Good is valid, a dual-slope foldback is used, providing protection against partial and total short-circuit at port output, while still being able to maintain the PD powered during normal transients at the PSE input voltage. Note that setting the PoEPn bit selects the 2× curve and clearing it selects the 1× curve. See Figure 18.

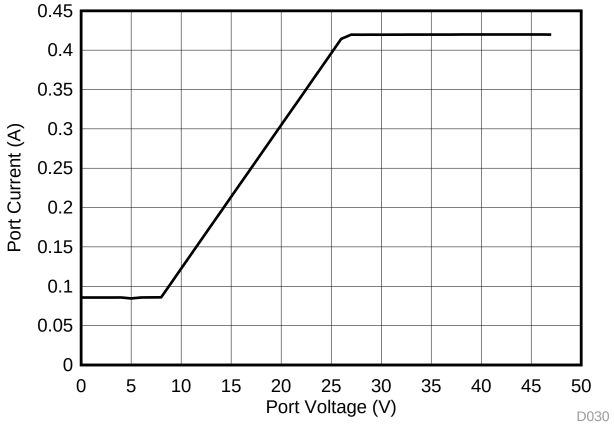

Figure 17. Foldback during Inrush (at Port Turn On): I_{LIM} vs V_{port}

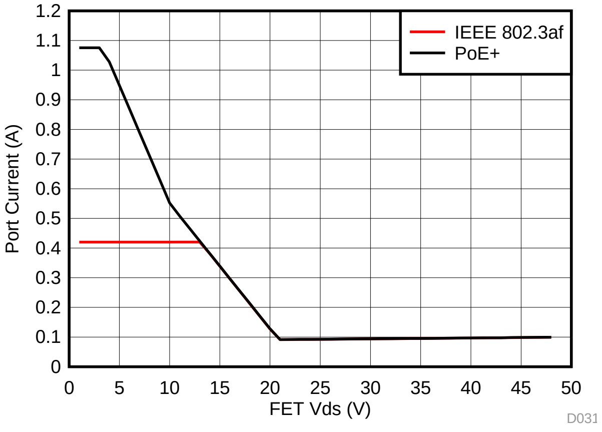

Figure 18. Foldback when the Port is Already ON: I_{LIM} vs V_{drain}

8.4 Device Functional Modes

8.4.1 Port Operating Modes

8.4.1.1 Semiauto

The port performs detection and classification (if valid detection occurs) continuously. Registers are updated each time a detection or classification occurs. The port power is not automatically turned on. Power Enable or IEEE Power Enable command is required to turn on the port.

8.4.1.2 Manual

The port performs the functions indicated by its registers one time when commanded. There is no automatic state change.

8.4.1.3 Power Off

The port is powered off and does not autonomously perform a detection, classification, or power-on. In this mode, Status and Enable bits for the associated port are reset.

8.4.2 Detection

To eliminate the possibility of false detection, the TPS2388 uses a TI proprietary 4-point detection method to determine the signature resistance of the PD device. False detection of a 25-kΩ signature can occur with 2-point detection type PSEs in noisy environments or if the load is highly capacitive.

Both detection 1 and detection 2 are merged into a single detection function which is repeated. Detection 1 applies I1 (160 µA) to a port, waits 60 ms, then measures the port voltage V1 with the integrating ADC. Detection 2 applies I2 (270 µA) to a port, waits 60 ms, then measures the port voltage V2. The process is repeated a second time. Multiple comparisons and calculations are performed on all four measurement point combinations to eliminate the effects of a non-linear or hysteretic PD signature. The resulting port signature is then sorted into the appropriate category.

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Device Functional Modes (continued)

NOTE

The detection resistance measurement result is also available in the Port Detect Resistance register.

8.4.3 Classification

Hardware classification (class) is performed by supplying a voltage and sampling the resulting current. To eliminate the high power of a classification event from occurring in the power controller chip, the TPS2388 makes use of the external power FET for classification.

During classification, the voltage on the gate node of the external MOSFET is part of a linear control loop. The control loop applies the appropriate MOSFET drive to maintain a differential voltage between VPWR and DRAIN of 17.5 V. During classification the voltage across the sense resistor in the source of the MOSFET is measured and converted to a class level within the TPS2388. If a load short occurs during classification, the MOSFET gate voltage is quickly reduced to a linearly controlled, short-circuit value for the duration of the class event.

Classification results may be read through the I^2C Detection Event and Port n Status Registers. The TPS2388 also supports two-event classification for type 2 PDs, using the IEEE Power Enable register.

8.4.4 DC Disconnect

Disconnect is the automated process of turning off power to the port. When the port is unloaded or at least falls below minimum load, it is necessary to turn off power to the port and restart detection. In DC disconnect, the voltage across the sense resistors is measured. When enabled, the DC disconnect function monitors the sense resistor voltage of a powered port to verify the port is drawing at least the minimum current to remain active. The TDIS timer counts up whenever the port current is below a 7.5-mA threshold. If a timeout occurs, the port is shut down and the corresponding disconnect bit in the Fault Event Register is set. The TDIS counter is reset each time the current goes continuously higher than the disconnect threshold for nominally 15 ms.

The TDIS duration is set by the TMPDO Bits of the Timing Configuration register (0x16).

8.5 Programming

8.5.1 I^2C Serial Interface

The TPS2388 features a 3-wire I^2C interface, using SDAI, SDAO, and SCL. Each transmission includes a Start condition sent by the master, followed by the device address (7-bit) with R/W bit, a register address byte, then one or two data bytes and a Stop condition. The recipient also sends an acknowledge bit following each byte transmitted. Also, SDAI/SDAO is stable while SCL is high except during a Start or Stop condition.

Figure 19 and Figure 20 illustrate read and write operations through I^2C interface, using configuration A or B (see *Table 19* for more details). The 'parametric' read operation is applicable to A/D conversion results. The TPS2388 also features quick access to the latest addressed register through I^2C bus. This means that when a Stop bit is received, the register pointer is not automatically reset.

It is also possible to perform a write operation to many TPS2388 devices at the same time. The slave address during this broadcast access is 0x7F, as shown in *Pin Status Register*. Depending on which configuration (A or B) is selected, a global write proceeds as following:

- Config A: Both 4-port devices (1 to 4 and 5 to 8) are addressed at same time.
- Config B: The whole device is addressed.

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Programming (continued)

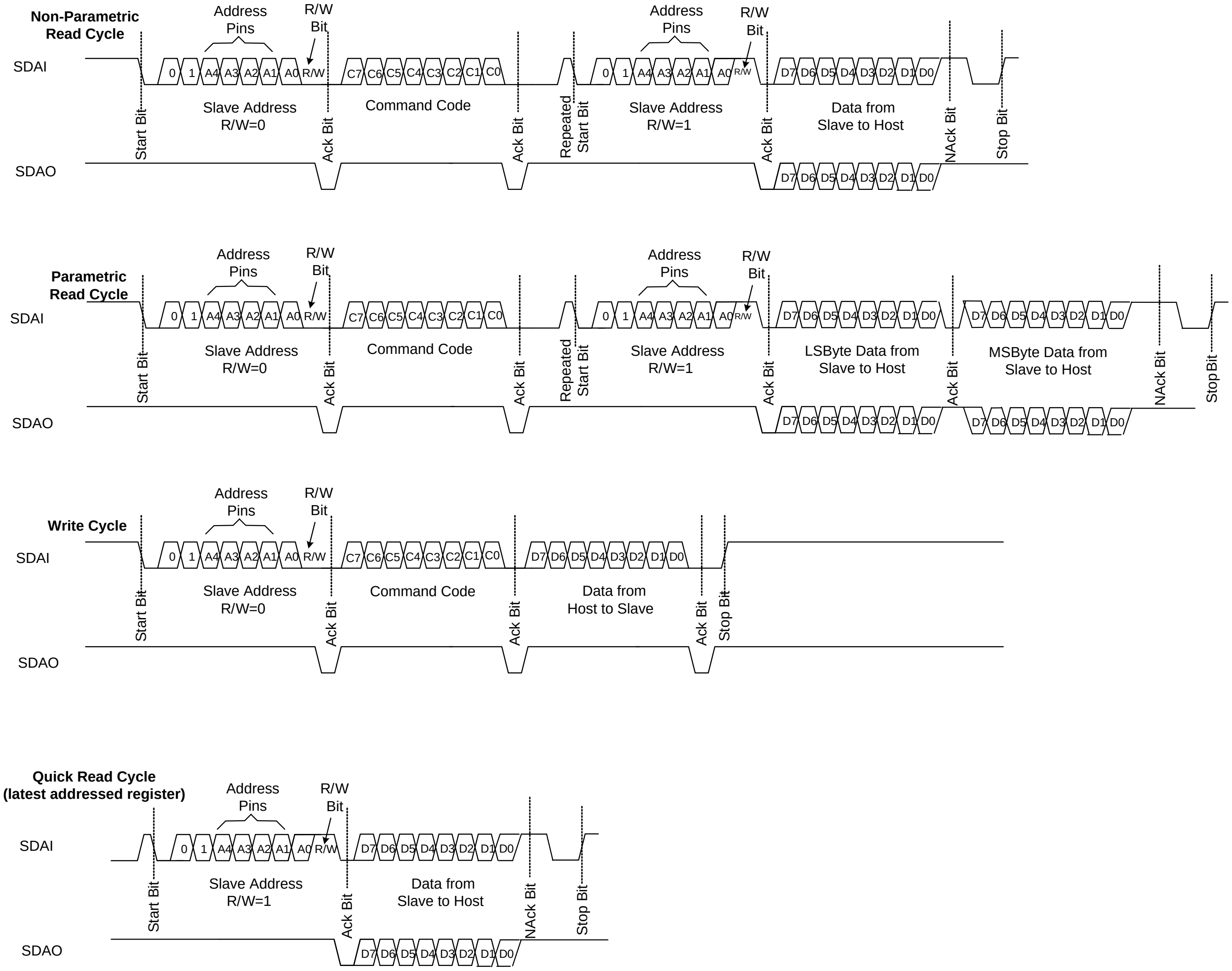

Figure 19. I^{2}C interface Read and Write Protocol – Configuration A

Programming (continued)

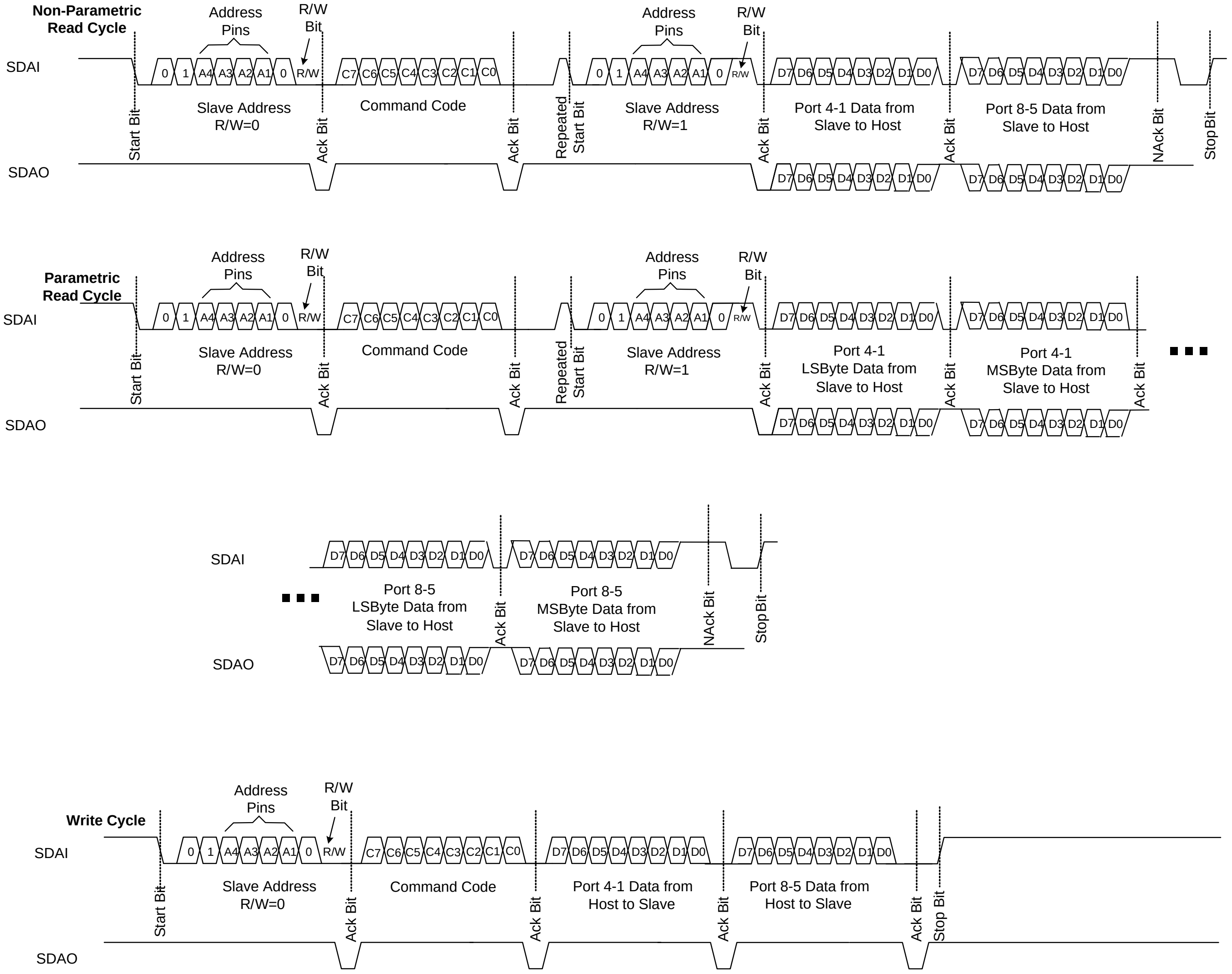

Figure 20. I^{2}C interface Read and Write Protocol – Configuration B

8.6 Register Maps

8.6.1 Complete Register Set

Table 1. Main Registers

Cmd Code	Register or Command Name	I^2C R/W	Data Byte	RST State	Bits Description							
INTERRUPTS												
00h	INTERRUPT	RO	1	1000,0000b(1)	SUPF	STRTF	IFAULT	CLASC	DETC	DISF	PGC	PEC
01h	INTERRUPT MASK	R/W	1	1000,0000b	SUMSK	STMSK	IFMSK	CLMSK	DEMSK	DIMSK	PGMSK	PEMSK
EVENT												
02h	POWER EVENT	RO	1	0000,0000b	Power Good status change				Power Enable status change			
03h		CoR	1		PGC4	PGC3	PGC2	PGC1	PEC4	PEC3	PEC2	PEC1
04h	DETECTION EVENT	RO	1	0000,0000b	Classification				Detection			
05h		CoR	1		CLSC4	CLSC3	CLSC2	CLSC1	DETC4	DETC3	DETC2	DETC1
06h	FAULT EVENT	RO	1	0000,0000b	Disconnect occurred				ICUT fault occurred			
07h		CoR	1		DISF4	DISF3	DISF2	DISF1	ICUT4	ICUT3	ICUT2	ICUT1
08h	START/ILIM EVENT	RO	1	0000,0000b	ILIM fault occurred				START fault occurred			
09h		CoR	1		ILIM4	ILIM3	ILIM2	ILIM1	STRT4	STRT3	STRT2	STRT1
0Ah	SUPPLY EVENT	RO	1	0111,0000b(2)	TSD	VDUV	VDWRN	VPUV	Rsvd	Rsvd	Rsvd	Rsvd
0Bh		CoR	1									
STATUS												
0Ch	PORT 1 STATUS	RO	1	0000,0000b	Rsvd	CLASS Port 1			DETECT Port 1			
0Dh	PORT 2 STATUS	RO	1	0000,0000b	Rsvd	CLASS Port 2			DETECT Port 2			
0Eh	PORT 3 STATUS	RO	1	0000,0000b	Rsvd	CLASS Port 3			DETECT Port 3			
0Fh	PORT 4 STATUS	RO	1	0000,0000b	Rsvd	CLASS Port 4			DETECT Port 4			
10h	POWER STATUS	RO	1	0000,0000b	PG4	PG3	PG2	PG1	PE4	PE3	PE2	PE1
11h	PIN STATUS	RO	1	0,A[4:0],0,0	Rsvd	SLA4	SLA3	SLA2	SLA1	SLA0	Rsvd	Rsvd
CONFIGURATION												
12h	OPERATING MODE	R/W	1	0000,0000b	Port 4 Mode		Port 3 Mode		Port 2 Mode		Port 1 Mode	
13h	DISCONNECT ENABLE	R/W	1	0000,0000b	Rsvd	Rsvd	Rsvd	Rsvd	DCDE4	DCDE3	DCDE2	DCDE1
14h	DETECT/CLASS ENABLE	R/W	1	0000,0000b	CLE4	CLE3	CLE2	CLE1	DETE4	DETE3	DETE2	DETE1
15h	PWRPR/ICUT DISABLE	R/W	1	0000,0000b	OSS4	OSS3	OSS2	OSS1	DCUT4	DCUT3	DCUT2	DCUT1
16h	TIMING CONFIG	R/W	1	0000,0000b	TLIM		TSTART		TOVLD		TMPDO	
17h	GENERAL MASK	R/W	1	1000,0000b	INTEN	Rsvd	nbitACC	MbitPrty	CLCHE	DECHE	Rsvd	

(1) SUPF bit reset state shown is at Power up only
(2) VDUV, VPUV and VDWRN bits reset state shown is at Power up only

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Register Maps (continued)

Table 1. Main Registers (continued)

Cmd Code	Register or Command Name	I^2C R/W	Data Byte	RST State	Bits Description							
PUSH BUTTONS												
18h	DETECT/CLASS Restart	WO	1	0000,0000b	RCL4	RCL3	RCL2	RCL1	RDET4	RDET3	RDET2	RDET1
19h	POWER ENABLE	WO	1	0000,0000b	POFF4	POFF3	POFF2	POFF1	PWON4	PWON3	PWON2	PWON1
1Ah	RESET	WO	1	0000,0000b	CLRAIN	CLINP	Rsvd	RESAL	RESP4	RESP3	RESP2	RESP1
GENERAL/SPECIALIZED												
1Bh	ID	RO	1	Mf[4:0],IC[2:0]	MFR ID					IC Version		
1Ch	Reserved	CoR	1	0000,0000b	Reserved					Reserved		
1Eh	POLICE 21 CONFIG	R/W	1	1111,1111b	POLICE Port 2				POLICE Port 1			
1Fh	POLICE 43 CONFIG	R/W	1	1111,1111b	POLICE Port 4				POLICE Port 3			
23h	IEEE Power Enable	WO	1	0000,0000b	T2PON4	T2PON3	T2PON2	T2PON1	T1PON4	T1PON3	T1PON2	T1PON1
24h	Power-on FAULT	RO	1	0000,0000b	PF Port 4		PF Port 3		PF Port 2		PF Port 1	
25h		CoR	1									
26h	RE-MAPPING	R/W	1	1110,0100b	Physical re-map Logical Port 4		Physical re-map Logical Port 3		Physical re-map Logical Port 2		Physical re-map Logical Port 1	
27h	Multi-bit Power Priority 21	R/W	1	0000,0000b	Rsvd	Port 2			Rsvd	Port 1		
28h	Multi-bit Power Priority 43	R/W	1	0000,0000b	Rsvd	Port 4			Rsvd	Port 3		
29h-2Bh	Reserved	R/W	1	0000,0000b	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2Ch	TEMPERATURE	RO	1	0000,0000b	Temperature (bits 7 to 0)							
2Eh	INPUT VOLTAGE	RO	2	0000,0000b	Input Voltage: LSByte							
2Fh		RO		0000,0000b	Rsvd	Rsvd	Input Voltage: MSByte (bits 13 to 8)					
EXTENDED REGISTER SET – PORT PARAMETRIC MEASUREMENT												
30h	PORT 1 CURRENT	RO	2	0000,0000b	Port 1 Current: LSByte							
31h		RO		0000,0000b	Rsvd	Rsvd	Port 1 Current: MSByte (bits 13 to 8)					
32h	PORT 1 VOLTAGE	RO	2	0000,0000b	Port 1 Voltage: LSByte							
33h		RO		0000,0000b	Rsvd	Rsvd	Port 1 Voltage: MSByte (bits 13 to 8)					

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Table 2. Main Registers

Cmd Code	Register or Command Name	I^2C R/W	Data Byte	RST State	Bits Description							
34h	PORT 2 CURRENT	RO	2	0000,0000b	Port 2 Current: LSByte							
35h		RO		0000,0000b	Rsvd	Rsvd	Port 2 Current: MSByte (bits 13 to 8)					
36h	PORT 2 VOLTAGE	RO	2	0000,0000b	Port 2 Voltage: LSByte							
37h		RO		0000,0000b	Rsvd	Rsvd	Port 2 Voltage: MSByte (bits 13 to 8)					
38h	PORT 3 CURRENT	RO	2	0000,0000b	Port 3 current: LSByte							
39h		RO		0000,0000b	Rsvd	Rsvd	Port 3 Current: MSByte (bits 13 to 8)					
3Ah	PORT 3 VOLTAGE	RO	2	0000,0000b	Port 3 Voltage: LSByte							
3Bh		RO		0000,0000b	Rsvd	Rsvd	Port 3 Voltage: MSByte (bits 13 to 8)					
3Ch	PORT 4 CURRENT	RO	2	0000,0000b	Port 4 current: LSByte							
3Dh		RO		0000,0000b	Rsvd	Rsvd	Port 4 Current: MSByte (bits 13 to 8)					
3Eh	PORT 4 VOLTAGE	RO	2	0000,0000b	Port 4 Voltage: LSByte							
3Fh		RO		0000,0000b	Rsvd	Rsvd	Port 4 Voltage: MSByte (bits 13 to 8)					
CONFIGURATION/OTHERS												
40h	PoE PLUS	R/W	1	0000,0000b	PoEP4	PoEP3	PoEP2	PoEP1	Rsvd	Rsvd	Rsvd	TPON
41h	FIRMWARE REVISION	RO	1	RRRR,RRRRb	Firmware Revision							
42h	I2C WATCHDOG	R/W	1	0001,0110b	Rsvd	Rsvd	Rsvd	Watchdog Disable				WDS
43h	DEVICE ID	RO	1	110,sr[4:0]	Device ID number			Silicon Revision number				
PORT SIGNATURE MEASUREMENTS												
44h	P1 DETECT RESISTANCE	RO	1	0000,0000b	Port 1 Resistance							
45h	P2 DETECT RESISTANCE	RO	1	0000,0000b	Port 2 Resistance							
46h	P3 DETECT RESISTANCE	RO	1	0000,0000b	Port 3 Resistance							
47h	P4 DETECT RESISTANCE	RO	1	0000,0000b	Port 4 Resistance							
48h-6Fh	Reserved	R/W	1	0000,0000b	Reserved							

Table 3. Registers Configuration A vs B

Cmd Code	Register or Command Name	Bits Description	Configuration A	Configuration B
00h	INTERRUPT	INT bits P1-4, P5-8	Separate mask and interrupt result per group of 4 ports. The Supply event bit is repeated twice.	
01h	INTERRUPT MASK	MSK bits P1-4, P5-8		
02h	POWER EVENT	PGC_PEC P4-1, P8-5	Separate event byte per group of 4 ports.	
03h				
04h	DETECTION EVENT	CLS_DET P4-1, P8-5		
05h				
06h	FAULT EVENT	DIS_ICUT P4-1, P8-5		
07h				
08h	START/ILIM EVENT	ILIM_STR P4-1, P8-5		
09h				
0Ah	SUPPLY EVENT	TSD, VDUV, VDUW, VPUV	Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** result. Clearing at least one VPUV/VDUV also clears the other one.	
0Bh				
0Ch	PORT 1 STATUS	CLS&DET1_CLS&DET5	Separate Status byte per port	
0Dh	PORT 2 STATUS	CLS&DET2_CLS&DET6		
0Eh	PORT 3 STATUS	CLS&DET3_CLS&DET7		
0Fh	PORT 4 STATUS	CLS&DET4_CLS&DET8		
10h	POWER STATUS	PG_PE P4-1, P8-5	Separate status byte per group of 4 ports	
11h	PIN STATUS	A4-A1,A0	Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** result, except that A0 = 0 (port 1 to 4) or 1 (port 5 to 8).	Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** result, including A0 = 0.
12h	OPERATING MODE	MODE P4-1, P8-5	Separate Mode byte per group of 4 ports.	
13h	DISCONNECT ENABLE	DCDE P4-1, P8-5	Separate DC disconnect enable byte per group of 4 ports.	
14h	DETECT/CLASS ENABLE	CLE_DETE P4-1, P8-5	Separate Detect/Class Enable byte per group of 4 ports.	
15h	PWRPR/ICUT DISABLE	OSS_DCUT P4-1, P8-5	Separate OSS/DCUT byte per group of 4 ports.	
16h	TIMING CONFIG	TLIM_TSTRT_TOVLD_TMPDO P4-1, P8-5	Separate Timing byte per group of 4 ports.	
17h	GENERAL MASK	P4-1, P8-5 including n-bit access	Separate byte per group of 4 ports. n-bit access: Setting this in at least one of the virtual quad register space is enough to enter Config B mode. To go back to config A, clear both. MbitPrty: Setting this in at least one of the virtual quad register space is enough to enter 3-bit shutdown priority. To go back to 1-bit shutdown, clear both MbitPrty bits.	
18h	DETECT/CLASS Restart	RCL_RDET P4-1, P8-5	Separate DET/CL RST byte per group of 4 ports	
19h	POWER ENABLE	POF_PWON P4-1, P8-5	Separate POF/PWON byte per group of 4 ports	
1Ah	RESET	P4-1, P8-5	Separate byte per group of 4 ports, Clear Int pin and Clear All int. However, If at least one of the IC reset bits is set – the whole chip has a POR.	Separate byte per group of 4 ports. However, if any of the following bit is set for one 4-port group, the corresponding action is applied to both 4-port groups: Reset IC, Clear Int pin, and Clear All Int.
1Bh	ID		Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** result unless modified through I^2C.	

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Table 3. Registers Configuration A vs B (continued)

Cmd Code	Register or Command Name	Bits Description	Configuration A	Configuration B
1Eh	POLICE 21 CONFIG	POL2&1, POL6&5	Separate Policing byte per group of 2 ports.	
1Fh	POLICE 43 CONFIG	POL4&3, POL8&7		
23h	IEEE Power Enable	T2P_T1P P4-1, P8-5	Separate IEEE Power Enable byte per group of 2 ports	
24h	Power-on FAULT	PF P4-1, P8-5	Separate Power-on FAULT byte per group of 4 ports	
25h				
26h	PORT REMAPPING	Logical P4-1, P8-5	Separate Remapping byte per group of 4 ports. Reinitialized only if POR or RESET pin. Kept unchanged if 0x1A IC reset or CPU watchdog reset.	
2Ch	TEMPERATURE	TEMP P1-4, P5-8	Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** result.	
2Eh	INPUT VOLTAGE	VPWR P1-4, P5-8	Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** result.	
2Fh				
30h	PORT 1 CURRENT	I1, I5	Separate 2-byte per group of 4 ports	Separate 2-byte per group of 4 ports. 2-byte Read at 0x30 gives I1 4-byte Read at 0x30 gives I1, I5.
31h			N/A	2-byte Read at 0x31 gives I5.
32h	PORT 1 VOLTAGE	V1, V5	Separate 2-byte per group of 4 ports	2-byte Read at 0x32 gives V1 4-byte Read at 0x32 gives V1, V5.
33h			N/A	2-byte Read at 0x33 gives V5.
34h	PORT 2 CURRENT	I2, I6	Separate 2-byte per group of 4 ports	2-byte Read at 0x34 gives I2 4-byte Read at 0x34 gives I2, I6.
35h			N/A	2-byte Read at 0x35 gives I6.
36h	PORT 2 VOLTAGE	V2, V6	Separate 2-byte per group of 4 ports	2-byte Read at 0x36 gives V2 4-byte Read at 0x36 gives V2, V6.
37h			N/A	2-byte Read at 0x37 gives V6.
38h	PORT 3 CURRENT	I3, I7	Separate 2-byte per group of 4 ports	2-byte Read at 0x38 gives I3 4-byte Read at 0x38 gives I3, I7.
39h			N/A	2-byte Read at 0x39 gives I7.
3Ah	PORT 3 VOLTAGE	V3, V7	Separate 2-byte per group of 4 ports	2-byte Read at 0x3A gives V3 4-byte Read at 0x3A gives V3, V7.
3Bh			N/A	2-byte Read at 0x3B gives V7.
3Ch	PORT 4 CURRENT	I4, I8	Separate 2-byte per group of 4 ports	2-byte Read at 0x3C gives I4 4-byte Read at 0x3C gives I4, I8.
3Dh			N/A	2-byte Read at 0x3D gives I8.
3Eh	PORT 4 VOLTAGE	V4, V8	Separate 2-byte per group of 4 ports	2-byte Read at 0x3E gives V4 4-byte Read at 0x3E gives V4, V8.
3Fh			N/A	2-byte Read at 0x3F gives V8.
40h	PoE PLUS	PoEP_TPON, P4-1, P8-5	TPON setting: separate setting per group of 4 ports. Separate PoEP config byte per group of 4 ports.	
41h	FIRMWARE REVISION	FRV P1-4, P5-8	Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** result.	

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Table 3. Registers Configuration A vs B (continued)

Cmd Code	Register or Command Name	Bits Description	Configuration A	Configuration B
42h	I2C WATCHDOG	P1-4, P5-8	IWD3-0: if at least one of the two 4-port settings is different than 1011b, the watchdog is enabled for all 8 ports. WDS: Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** WDS result. Each WDS bit needs to be cleared individually through I^{2}C.	
43h	DEVICE ID	DID_SR P1-4, P5-8	Both 8-bit registers (port 1 to 4 and port 5 to 8) must show the **same** result unless modified through I^{2}C.	
44h	PORT 1 RESISTANCE	RDET1, RDET5	Separate byte per port. Detection resistance always updated, detection good or bad.	
45h	PORT 2 RESISTANCE	RDET2, RDET6		
46h	PORT 3 RESISTANCE	RDET3, RDET7		
47h	PORT 4 RESISTANCE	RDET4, RDET8		

8.6.2 INTERRUPT Register

COMMAND = 00h with 1 Data Byte, Read only

Active high, each bit corresponds to a particular event that occurred. Each bit can be individually reset by doing a read at the corresponding event register address, or by setting bit 7 of Reset register.

Any active bit of Interrupt register activates the $\overline{\text{INT}}$ output if its corresponding Mask bit in INTERRUPT Mask register (01h) is set, as well as the INTEN bit in the General Mask register.

Figure 21. INTERRUPT Register Format

7	6	5	4	3	2	1	0
SUPF	STRTF	IFAULT	CLASC	DETC	DISF	PGC	PEC
R-1	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. INTERRUPT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SUPF	R	1	Indicates that a Supply Event Fault occurred SUPF = TSD || VDUV || VPUV 1 = At least one Supply Event Fault occurred 0 = No such event occurred
6	STRTF	R	0	Indicates that a t_{START} Fault occurred on at least one port. STRTF = STRT1 || STRT2 || STRT3 || STRT4 1 = t_{START} Fault occurred for at least one port 0 = No t_{START} Fault occurred
5	IFAULT	R	0	Indicates that a t_{OVLD} or t_{LIM} Fault occurred on at least one port. IFAULT = ICUT1 || ICUT2 || ICUT3 || ICUT4 || ILIM1 || ILIM2 || ILIM3 || ILIM4 1 = t_{OVLD} and/or t_{LIM} Fault occurred for at least one port 0 = No t_{OVLD} nor t_{LIM} Fault occurred
4	CLASC	R	0	Indicates that at least one classification cycle occurred on at least one port CLASC = CLSC1 || CLSC2 || CLSC3 || CLSC4 1 = At least one classification cycle occurred for at least one port 0 = No classification cycle occurred
3	DETC	R	0	Indicates that at least one detection cycle occurred on at least one port DETC = DETC1 || DETC2 || DETC3 || DETC4 1 = At least one detection cycle occurred for at least one port 0 = No detection cycle occurred
2	DISF	R	0	Indicates that a disconnect event occurred on at least one port. DISF = DISF1 || DISF2 || DISF3 || DISF4 1 = Disconnect event occurred for at least one port 0 = No disconnect event occurred
1	PGC	R	0	Indicates that a power good status change occurred on at least one port. PGC = PGC1 || PGC2 || PGC3 || PGC4 1 = Power good status change occurred on at least one port 0 = No power good status change occurred
0	PEC	R	0	Indicates that a power enable status change occurred on at least one port PEC = PEC1 || PEC2 || PEC3 || PEC4 1 = Power enable status change occurred on at least one port 0 = No power enable status change occurred

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8.6.3 INTERRUPT MASK Register

COMMAND = 01h with 1 Data Byte, Read/Write

Each bit corresponds to a particular event or fault as defined in the Interrupt register.

Writing a 0 into a bit will mask the corresponding event/fault from activating the $\overline{\text{INT}}$ output.

Note that the bits of the Interrupt register always change state according to events or faults, regardless of the state of the state of the Interrupt Mask register.

Note that the INTEN bit of the General Mask register must also be set in order to allow an event to activate the $\overline{\text{INT}}$ output.

Figure 22. INTERRUPT MASK Register Format

7	6	5	4	3	2	1	0
SUMSK	STMSK	IFMSK	CLMSK	DEMSK	DIMSK	PGMSK	PEMSK
R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. INTERRUPT MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SUMSK	R/W	1	Supply Event Fault mask bit. 1 = Supply Event Fault will activate the $\overline{\text{INT}}$ output. 0 = Supply Event Fault will have no impact on $\overline{\text{INT}}$ output.
6	STMSK	R/W	0	t_{START} Fault mask bit. 1 = t_{START} Fault will activate the $\overline{\text{INT}}$ output. 0 = t_{START} Fault will have no impact on $\overline{\text{INT}}$ output.
5	IFMSK	R/W	0	tOVLD or LIM Fault mask bit. 1 = t_{OVLD} and/or t_{LIM} Fault occurrence will activate the $\overline{\text{INT}}$ output 0 = t_{OVLD} and/or t_{LIM} Fault occurrence will have no impact on $\overline{\text{INT}}$ output
4	CLMSK	R/W	0	Classification cycle mask bit. 1 = Classification cycle occurrence will activate the $\overline{\text{INT}}$ output. 0 = Classification cycle occurrence will have no impact on $\overline{\text{INT}}$ output.
3	DEMSK	R/W	0	Detection cycle mask bit. 1 = Detection cycle occurrence will activate the $\overline{\text{INT}}$ output. 0 = Detection cycle occurrence will have no impact on $\overline{\text{INT}}$ output.
2	DIMSK	R/W	0	Disconnect event mask bit. 1 = Disconnect event occurrence will activate th $\overline{\text{INT}}$ output. 0 = Disconnect event occurrence will have no impact on $\overline{\text{INT}}$ output.
1	PGMSK	R/W	0	Power good status change mask bit. 1 = Power good status change will activate the $\overline{\text{INT}}$ output. 0 = Power good status change will have no impact on $\overline{\text{INT}}$ output.
0	PEMSK	R/W	0	Power enable status change mask bit. 1 = Power enable status change will activate the $\overline{\text{INT}}$ output. 0 = Power enable status change will have no impact on $\overline{\text{INT}}$ output.

NOTE

If SUMSK = 0, a VPWR undervoltage Event Fault (VPUV) will also **not** shut off ports, as long as VPWR is above the VPWR UVLO threshold.

8.6.4 POWER EVENT Register

COMMAND = 02h with 1 Data Byte, Read only

COMMAND = 03h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual port.

A read at each location (02h or 03h) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 23. POWER EVENT Register Format

7	6	5	4	3	2	1	0
PGC4	PGC3	PGC2	PGC1	PEC4	PEC3	PEC2	PEC1
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 6. POWER EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	PGC4–PGC1	R or CR	0	Indicates that a power good status change occurred. 1 = Power good status change occurred 0 = No power good status change occurred
3–0	PEC4–PEC1	R or CR	0	Indicates that a power enable status change occurred. 1 = Power enable status change occurred 0 = No power enable status change occurred

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8.6.5 DETECTION EVENT Register

COMMAND = 04h with 1 Data Byte, Read only

COMMAND = 05h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual port.

A read at each location (04h or 05h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when port n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 24. DETECTION EVENT Register Format

7	6	5	4	3	2	1	0
CLSC4	CLSC3	CLSC2	CLSC1	DETC4	DETC3	DETC2	DETC1
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 7. DETECTION EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	CLSC4–CLSC1	R or CR	0	Indicates that at least one classification cycle occurred if the CLCHE bit in General Mask register is low. Conversely, it indicates when a change of class occurred if the CLCHE bit is set. 1 = At least one classification cycle occurred (if CLCHE = 0) or a change of class occurred (CLCHE = 1) 0 = No classification cycle occurred (if CLCHE = 0) or no change of class occurred (CLCHE = 1)
3–0	DETC4–DETC1	R or CR	0	Indicates that at least one detection cycle occurred if the DECHE bit in General Mask register is low. Conversely, it indicates when a change in detection occurred if the DECHE bit is set. 1 = At least one detection cycle occurred (if DECHE = 0) or a change in detection occurred (DECHE = 1) 0 = No detection cycle occurred (if DECHE = 0) or no change in detection occurred (DECHE = 1)

8.6.6 FAULT EVENT Register

COMMAND = 06h with 1 Data Byte, Read only

COMMAND = 07h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual port.

A read at each location (06h or 07h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when port n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 25. FAULT EVENT Register Format

7	6	5	4	3	2	1	0
DISF4	DISF3	DISF2	DISF1	ICUT4	ICUT3	ICUT2	ICUT1
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 8. FAULT EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	DISF4–DISF1	R or CR	0	Indicates that a disconnect event occurred. 1 = Disconnect event occurred 0 = No disconnect event occurred
3–0	ICUT4–ICUT1	R or CR	0	Indicates that a t_{OVLD} Fault occurred. 1 = t_{OVLD} Fault occurred 0 = No t_{OVLD} Fault occurred

Note that if ICUT is disabled for a port, this port will not be automatically turned off during an ICUT fault condition. However, the ICUT fault flag will still be operational, with a fault timeout equal to t_{LIM} / 2.

Also, if a Clear on Read is done at the Fault Event register, not only the ICUTn bit is reset, but the associated port ICUT counter is also reset.

Note that this has no impact on TLIM counter at all.

In any other case, ICUT fault is related to TOVLD fault timer as usual and there is no counter reset during clear on read operation.

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8.6.7 START/ILIM EVENT Register

COMMAND = 08h with 1 Data Byte, Read only

COMMAND = 09h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual port.

A read at each location (08h or 09h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when port n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Note: When a Start Fault is reported after the IEEE Power Enable command is used, if the PECn bit in Power Event register is set, then there is an Inrush fault. If PECn bit is not set, then the Power-On Fault register indicates the cause of the fault.

Figure 26. START/ILIM EVENT Register Format

7	6	5	4	3	2	1	0
ILIM4	ILIM3	ILIM2	ILIM1	STRT4	STRT3	STRT2	STRT1
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 9. START/ILIM EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	ILIM4–ILIM1	R or CR	0	Indicates that a t_{LIM} fault occurred, which means the port has limited its output current to I_{LIM} or the folded back I_{LIM} for more than t_{LIM}. 1 = t_{LIM} fault occurred 0 = No t_{LIM} fault occurred
3–0	STRT4–STRT1	R or CR	0	Indicates that a t_{START} fault occurred at port turn on. Also indicates if a class or detection error occurred during a port turn on using the IEEE Power Enable command. 1 = t_{START} fault or class/detect error occurred 0 = No t_{START} fault or class/detect error occurred

8.6.8 SUPPLY EVENT Register

COMMAND = 0Ah with 1 Data Byte, Read only

COMMAND = 0Bh with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit D3, D2, D1, and D0 are reserved for future use.

A read at each location (0Ah or 0Bh) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 27. SUPPLY EVENT Register Format

7	6	5	4	3	2	1	0
TSD	VDUV	VDWRN	VPUV	–	–	–	–
R	R	R	R	R	R	R	R
CR	CR	CR	CR	CR	CR	CR	CR

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 10. SUPPLY EVENT Register Field Descriptions

Bit	Field	Type	POR	Description
7	TSD	R or CR	0	Indicates that a thermal shutdown occurred. When there is thermal shutdown, all ports are turned off and are put in OFF mode. The TPS2388 internal circuitry continues to operate however, including the A/D converters. Note that at as soon as the internal temperature has decreased below the low threshold, the ports can be turned back ON regardless of the status of the TSD bit. 1 = Thermal shutdown occurred 0 = No thermal shutdown occurred
6	VDUV	R or CR	1	Indicates that a VDD UVLO occurred. 1 = VDD UVLO occurred 0 = No VDD UVLO occurred
5	VDWRN	R or CR	1	Indicates that the VDD has fallen under the UVLO warning threshold. 1 = VDD UV Warning occurred 0 = No VDD UV warning occurred
4	VPUV	R or CR	1	Indicates Indicates that a VPWR undervoltage occurred. 1 = VPWR undervoltage occurred 0 = No VPWR undervoltage occurred

Note: Pulling $\overline{\text{RESET}}$ input low will not clear VDUV or VPUV.

When VPWR undervoltage occurs, all ports are shut off if SUMSK = 1. If VPWR UVLO or VDD UVLO occurs, there is power-on reset. Note also that turning OFF a port when VPWR undervoltage occurs also clears the corresponding bits in Fault Event register (DISFn, ICUTn), Start Event register (STRTn), Port n Status register (CLASS Pn, DETECT Pn), DETECT/CLASS ENABLE register (CLEn, DETEn) and Power-on Fault register (PFn). The corresponding PGCn and PECn bits of Power Event register will also be set if there is a change. The corresponding PEn and PGn bits of Power Status Register are also updated accordingly.

NOTE

A clear on Read will not effectively clear VDUV bit as long as the VPWR undervoltage condition is maintained.

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NOTE

If SUMSK = 0, a VPWR undervoltage Event Fault (VPUV) will not shut off ports, as long as VPWR is above the VPWR UVLO threshold.

NOTE

During VPWR undervoltage, the Detection Event register (CLSCn, DETCn) is not cleared, unless VPWR also falls below the VPWR UVLO falling threshold.

NOTE

If VPWR UVLO or VDD UVLO occurs, the I^2C interface stops operating, and SDAO is forced low.

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8.6.9 PORT 1 STATUS Register

COMMAND = 0Ch with 1 Data Byte, Read Only

Figure 28. PORT 1 STATUS Register Format

7	6	5	4	3	2	1	0
–	CLASS P1			DETECT P1			
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.10 PORT 2 STATUS Register

COMMAND = 0Dh with 1 Data Byte, Read Only

Figure 29. PORT 2 STATUS Register Format

7	6	5	4	3	2	1	0
–	CLASS P2			DETECT P2			
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.11 PORT 3 STATUS Register

COMMAND = 0Eh with 1 Data Byte, Read Only

Figure 30. PORT 3 STATUS Register Format

7	6	5	4	3	2	1	0
–	CLASS P3			DETECT P3			
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.12 PORT 4 STATUS Register

COMMAND = 0Fh with 1 Data Byte, Read Only

Figure 31. PORT 4 STATUS Register Format

7	6	5	4	3	2	1	0
–	CLASS P4			DETECT P4			
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit Descriptions: These bits represent the most recent classification and detection results for port n. These bits are cleared when port n is turned off.

Table 11. PORT STATUS Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7</td><td>–</td><td>R</td><td>0</td><td>Reserved</td></tr>
<tr><td>6–4</td><td>CLASS Pn</td><td>R</td><td>0</td><td>Most recent classification result on port n.
The selection is as following:
<table>
<tr><th colspan="3">CLASS Pn</th><th>Class Status</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Unknown</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Class 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Class 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Class 3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Class 4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved – read as Class 0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Class 0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Overcurrent</td></tr>
</table></td></tr>
<tr><td>3–0</td><td>DETECT Pn</td><td>R</td><td>0</td><td>Most recent detection result on port n.
The selection is as following:
<table>
<tr><th colspan="4">DETECT Pn</th><th>Class Status</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Unknown</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Short-circuit</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Too Low</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Valid</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Too High</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Open Circuit</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>MOSFET fault</td></tr>
</table></td></tr>
</table>

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8.6.13 POWER STATUS Register

COMMAND = 10h with 1 Data Byte, Read only

Each bit represents the actual power status of a port.

Each bit xx1-4 represents an individual port..

These bits are cleared when port n is turned off, including if the turn off is caused by a fault condition.

Figure 32. POWER STATUS Register Format

7	6	5	4	3	2	1	0
PG4	PG3	PG2	PG1	PE4	PE3	PE2	PE1
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. POWER STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	PG4–PG1	R	0	Each bit, when at 1, indicates that the port is on and that the voltage at DRAINn pin has gone below the power good threshold during the port turn on. These bits are latched high once the turn on is complete and can only be cleared when the port is turned off or at RESET/POR. 1 = Power is good 0 = Power is not good
3–0	PE4–PE1	R	0	Each bit indicates the ON/OFF state of the corresponding port. 1 = Port is on 0 = Port is off

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8.6.14 Pin Status Register

COMMAND = 11h with 1 Data Byte, Read Only

Figure 33. Pin Status Register Format

7	6	5	4	3	2	1	0
0	SLA4	SLA3	SLA2	SLA1	SLA0	0	0
0	A4 pin	A3 pin	A2 pin	A1 pin	0/1 (1)	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) If Configuration A, it can be 0 or 1. If configuration B, it is 0.

Table 13. Pin Status Register Field Descriptions

Bit	Field	Type	Reset	Description
6-2	SLA4-SLA0	R	See above	I^{2}C device address, as defined while using pins A4-A1. SLA0 is internally defined as 0 or 1.

DESCRIPTION	BINARY DEVICE ADDRESS							ADDRESS PINS			
	6	5	4	3	2	1	0	A4	A3	A2	A1
Broadcast access	1	1	1	1	1	1	1	X	X	X	X
Slave 0	0	1	0	0	0	0	0/1	GND	GND	GND	GND
	0	1	0	0	0	1	0/1	GND	GND	GND	HIGH
	0	1	0	0	1	0	0/1	GND	GND	HIGH	GND
	0	1	0	0	1	1	0/1	GND	GND	HIGH	HIGH
	0	1	0	1	0	0	0/1	GND	HIGH	GND	GND
	0	1	0	1	0	1	0/1	GND	HIGH	GND	HIGH
	0	1	0	1	1	0	0/1	GND	HIGH	HIGH	GND
	0	1	0	1	1	1	0/1	GND	HIGH	HIGH	HIGH
	0	1	1	0	0	0	0/1	HIGH	GND	GND	GND
	0	1	1	0	0	1	0/1	HIGH	GND	GND	HIGH
	0	1	1	0	1	0	0/1	HIGH	GND	HIGH	GND
	0	1	1	0	1	1	0/1	HIGH	GND	HIGH	HIGH
	0	1	1	1	0	0	0/1	HIGH	HIGH	GND	GND
	0	1	1	1	0	1	0/1	HIGH	HIGH	GND	HIGH
	0	1	1	1	1	0	0/1	HIGH	HIGH	HIGH	GND
Slave 15	0	1	1	1	1	1	0/1	HIGH	HIGH	HIGH	HIGH

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8.6.15 OPERATING MODE Register

COMMAND = 12h with 1 Data Byte, Read/Write

Figure 34. OPERATING MODE Register Format

7	6	5	4	3	2	1	0
P4M1	P4M0	P3M1	P3M0	P2M1	P2M0	P1M1	P1M0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. OPERATING MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
-	P4M1–P4M0 P3M1–P3M0 P2M1–P2M0 P1M1–P1M0	R/W	0	Each pair of bits configures the operating mode per port. The selection is as following: M1 / M0 / Operating Mode: 0 0 OFF; 0 1 Manual; 1 0 Semiauto; 1 1 Semiauto In OFF mode, the port is OFF and there is no detection nor classification. In Manual mode, there is no automatic state change. In semiauto mode, detection and class are automated but not the port power on. Note that while in OFF mode, the corresponding bits are cleared: Detection Event register (CLSCn, DETCn), Fault Event register (DISFn, ICUTn), Start Event register (STRTn), Port n Status register (CLASS Pn, DETECT Pn), Detect/Class Enable register (CLEn, DETEn) and Power-on Fault register (PFn). The corresponding PEn and PGn bits of Power Status Register are also updated accordingly. The corresponding PGCn and PECn bits of Power Event register will also be set if there is a change. Also, a change of mode from semiauto to manual mode or OFF mode will cancel any ongoing cooldown time period.

M1	M0	Operating Mode
0	0	OFF
0	1	Manual
1	0	Semiauto
1	1	Semiauto

8.6.16 DISCONNECT ENABLE Register

COMMAND = 13h with 1 Data Byte, Read/Write

Bit Descriptions: Defines the disconnect detection mechanism for each port.

Figure 35. DISCONNECT ENABLE Register Format

7	6	5	4	3	2	1	0
–	–	–	–	DCDE4	DCDE3	DCDE2	DCDE1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. DISCONNECT ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	—	R/W	0	
3–0	DCDE4–DCDE1	R/W	0	DC disconnect enable. DC disconnect consists in measuring the port DC current at SENn, starting a timer (TDIS) if this current is below a threshold and turning the port off if a time-out occurs. Also, the corresponding disconnect bit (DISFn) in the FAULT EVENT register is set accordingly. The TDIS counter is reset each time the current goes continuously higher than the disconnect threshold for nominally 15 msec. The counter does not decrement below zero. Look at the TIMING CONFIGURATION register for more details on how to define the TDIS time period.

8.6.17 DETECT/CLASS ENABLE Register

COMMAND = 14h with 1 Data Byte, Read/Write

Bit Descriptions:

Detection and classification enable for each port.

When in Manual mode, setting a bit means that only one cycle (detection or classification) is performed for the corresponding port. The bit is automatically cleared by the time the cycle has been completed.

Note that similar result can be obtained by writing to the Detect/Class Restart register.

It is also cleared if a port turn off (Power Enable register) is issued.

When in semiauto mode, as long as the port is kept off, detection and classification are performed continuously, as long as the class and detect enable bits are kept set, but the class will be done only if the detection was valid. A Detect/Class Restart PB command can also be used to set the CLEn and DETEn bits, if in semiauto mode.

During t_{OVLD}, t_{LIM} or t_{START} cool down cycle, any Detect/Class Enable command for that port will be delayed until end of cool-down period. Note that at the end of cool down cycle, one or more detection/class cycles are automatically restarted as described previously, if the class and/or detect enable bits are set.

Figure 36. DETECT/CLASS ENABLE Register Format

7	6	5	4	3	2	1	0
CLE4	CLE3	CLE2	CLE1	DETE4	DETE3	DETE2	DETE1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. DETECT/CLASS ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	CLE4-CLE1	R/W	0	Classification enable bits.
3–0	DETE4-DETE1	R/W	0	Detection enable bits.

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8.6.18 Port Power Priority/ICUT Disable Register Name

COMMAND = 15h with 1 Data Byte, R/W

Figure 37. Port Power Priority/ICUT Disable Register Format

7	6	5	4	3	2	1	0
OSS4	OSS3	OSS2	OSS1	DCUT4	DCUT3	DCUT2	DCUT1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Port Power Priority/ICUT Disable Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	OSS4-OSS1	R/W	0	Port power priority bits, one bit per port, if 1-bit shutdown priority has been selected. It is used to determine which port is shut down in response to an external assertion of the OSS fast shutdown signal. The turn off procedure (including register bits clearing) is similar to a port reset using Reset command (1Ah register), except that it does not cancel any ongoing fault cool down time count. 1 = When the OSS signal is asserted, the corresponding port is powered off. 0 = OSS signal has no impact on the port.
3–0	DCUT4-DCUT1	R/W	0	ICUT disable for each port. Used to prevent removal of the associated port's power due to an ICUT fault, regardless of the programming status of the Timing Configuration register. Note that there is still monitoring of ILIM faults. 1: Port's ICUT is disabled. This means that an ICUT fault alone will not turn off this port. 0: Port's ICUT is enabled. This enables port turn off if there is ICUT fault. Note that if ICUT is disabled for a port, this port will not be automatically turned off during an ICUT fault condition. However, the ICUT fault flag will still be operational, with a fault timeout equal to $t_{LIM}/2$.

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8.6.19 TIMING CONFIGURATION Register

COMMAND = 16h with 1 Data Byte, Read/Write

Bit Descriptions: These bits define the timing configuration for all four ports.

Note: the PGn and PEn bits (Power Status register) are cleared when there is a TLIM, TOVLD, TMPDO, or TSTART fault condition.

Figure 38. TIMING CONFIGURATION Register Format

7	6	5	4	3	2	1	0
TLIM		TSTART		TOVLD		TMPDO	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. TIMING CONFIGURATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7 –6	TLIM	R/W	0	ILIM fault timing, which is the output current limit time duration before port turn off. This timer is active and increments to the settings defined below after expiration of the TSTART time window and when the port is limiting its output current to I_{LIM}. If the ILIM counter is allowed to reach the programmed time-out duration specified below, the port will be powered off. The 1-second cool down timer is then started, and the port can not be turned-on until the counter has reached completion. In other circumstances (ILIM time-out has not been reached), while the port current is below I_{LIM}, the same counter decrements at a rate 1/16th of the increment rate. The counter does not decrement below zero. The ILIM counter is also cleared in the event of a port turn off due to a Power Enable or Port Reset command, a DC disconnect event or the OSS input. Note that in the event the TLIM setting is changed while this timer is already active for a port, this timer is automatically reset then restarted with the new programmed time-out duration. Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the detect enable bit is set. Also note that the cool down time count is immediately canceled with a port reset command, or if the OFF or Manual mode is selected. When a PoEPn bit in PoE Plus register is deasserted, the t_{LIM} used for the associated port is always the nominal value (about 60 ms). If PoEPn bit is asserted, then t_{LIM} for associated port is programmable with the following selection:
				TLIM / Nominal t_{LIM} (ms): 0 0 60 0 1 15 1 0 12 1 1 10
5-4	TSTART (or TINRUSH)	R/W	0	START fault timing, which is the maximum allowed overcurrent time during inrush. If at the end of TSTART period the current is still limited to I_{Inrush}, the port is powered off. This is followed by a 1-second cool down period, during which the port can not be turned-on Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the class and detect enable bits are set. Note that in the event the TSTART setting is changed while this timer is already active for a port, this new setting is ignored and will be applied only next time the port is turned ON. The selection is as following:
				TSTART / Nominal t_{START} (ms): 0 0 60 0 1 30 1 0 120 1 1 Reserved

TLIM sub-table:

TLIM		Nominal t_{LIM} (ms)
0	0	60
0	1	15
1	0	12
1	1	10

TSTART sub-table:

TSTART		Nominal t_{START} (ms)
0	0	60
0	1	30
1	0	120
1	1	Reserved

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Table 18. TIMING CONFIGURATION Register Field Descriptions (continued)

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>3–2</td><td>TOVLD</td><td>R/W</td><td>0</td><td>
<p>ICUT fault timing, which is the overcurrent time duration before port turn off. This timer is active and increments to the settings defined below after expiration of the TSTART time window and when the port current meets or exceeds I_{CUT}, or when it is limited by the current foldback. If the ICUT counter is allowed to reach the programmed time-out duration specified below, the port will be powered off. The 1-second cool down timer is then started, and the port can not be turned-on until the counter has reached completion.</p>
<p>In other circumstances (ICUT time-out has not been reached), while the port current is below I_{CUT}, the same counter decrements at a rate 1/16th of the increment rate. The counter does not decrement below zero. The ICUT counter is also cleared in the event of a port turn off due to a Power Enable or Port Reset command, a DC disconnect event or the OSS input</p>
<p>Note that in the event the TOVLD setting is changed while this timer is already active for a port, this timer is automatically reset then restarted with the new programmed time-out duration.</p>
<p>Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the detect enable bit is set. Also note that the cool down time count is immediately canceled with a port reset command, or if the OFF or Manual mode is selected.</p>
<p>Note that if a DCUTn bit is high in the Port Power Priority/ICUT Disable register, the ICUT fault timing for the associated port is disabled. This means that this port will not be turned off if there is only ICUT fault.</p>
<p>The selection is as following:</p>
<table>
<tr><th colspan="2">TOVLD</th><th>Nominal t_{OVLD} (ms)</th></tr>
<tr><td>0</td><td>0</td><td>60</td></tr>
<tr><td>0</td><td>1</td><td>30</td></tr>
<tr><td>1</td><td>0</td><td>120</td></tr>
<tr><td>1</td><td>1</td><td>240</td></tr>
</table>
</td></tr>
<tr><td>1–0</td><td>TMPDO</td><td>R/W</td><td>0</td><td>
<p>Disconnect delay, which is the time to turn off a port once there is a disconnect condition, and if the dc disconnect detect method has been enabled.</p>
<p>The TDIS counter is reset each time the current goes continuously higher than the disconnect threshold for nominally 15 ms.</p>
<p>The counter does not decrement below zero.</p>
<p>The selection is as following:</p>
<table>
<tr><th colspan="2">TMPDO</th><th>Nominal t_{MPDO} (ms)</th></tr>
<tr><td>0</td><td>0</td><td>360</td></tr>
<tr><td>0</td><td>1</td><td>90</td></tr>
<tr><td>1</td><td>0</td><td>180</td></tr>
<tr><td>1</td><td>1</td><td>720</td></tr>
</table>
</td></tr>
</table>

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8.6.20 GENERAL MASK Register

COMMAND = 17h with 1 Data Byte, Read/Write

Figure 39. GENERAL MASK Register Format

7	6	5	4	3	2	1	0
INTEN	–	nbitACC	MbitPrty	CLCHE	DECHE	–	–
R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. GENERAL MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INTEN	R/W	1	$\overline{\text{INT}}$ pin mask bit. Writing a 0 will mask any bit of Interrupt register from activating the $\overline{\text{INT}}$ output, whatever the state of the Interrupt Mask register. Note that activating INTEN has no impact on the event registers. 1 = Any unmasked bit of Interrupt register can activate the $\overline{\text{INT}}$ output 0 = $\overline{\text{INT}}$ output cannot be activated
6	–	R/W	0	
5	nbitACC	R/W	0	Register Access Configuration bit. Used to select configuration A or B. 1 = Configuration B. This means 16-bit access with a single device address. 0 = Configuration A. This means 8-bit access, while the 8-port device is treated as 2 separate 4-port devices with 2 consecutive slave addresses.
4	MbitPrty	R/W	0	Multi Bit Priority bit. Used to select between 1-bit shutdown priority and 3-bit shutdown priority. 1 = 3-bit shutdown priority. Register 0x27 and 0x28 need to be followed for port priority and OSS action. 0 = 1-bit shutdown priority. Register 0x15 needs to be followed for port priority and OSS action Note: If the MbitPrty bit needs to be changed from 0 to 1, make sure the OSS input is in the idle (low) state for a minimum of 200 µsec prior to setting the MbitPrty bit, to avoid any port misbehavior related to loss of synchronization with the OSS bit stream.
3	CLCHE	R/W	0	Class change Enable bit. When set, the CLSCn bits in Detection Event register only indicates when the result of the most current classification operation differs from the result of the previous one. 1 = CLSCn bit is set only when a change of class occurred for the associated port. 0 = CLSCn bit is set each time a classification cycle occurred for the associated port.
2	DECHE	R/W	0	Detect Change Enable bit. When set, the DETCn bits in Detection Event register only indicates when the result of the most current detection operation differs from the result of the previous one. 1 = DETCn bit is set only when a change in detection occurred for the associated port. 0 = DETCn bit is set each time a detection cycle occurred for the associated port.
1	–	R/W	0	
0	–	R/W	0	

8.6.21 DETECT/CLASS RESTART Register

COMMAND = 18h with 1 Data Byte, Write Only

Push button register.

Each bit corresponds to a particular cycle (detect or class restart) per port. Each cycle can be individually triggered by writing a 1 at that bit location, while writing a 0 does not change anything for that event.

In Manual mode, a single cycle (detect or class restart) will be triggered while in Semiauto mode, it sets the corresponding bit in the Detect/Class Enable register.

A Read operation will return 00h.

During t_{OVLD}, t_{LIM} or t_{START} cool down cycle, any Detect/Class Restart command for that port will be accepted but the corresponding action will be delayed until end of cool-down period.

Figure 40. DETECT/CLASS RESTART Register Format

7	6	5	4	3	2	1	0
RCL4	RCL3	RCL2	RCL1	RDET4	RDET3	RDET2	RDET1
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 20. DETECT/CLASS RESTART Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	RCL4–RCL1	W	0	Restart classification bit
3–0	RDET4–RDET1	W	0	Restart detection bits

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8.6.22 POWER ENABLE Register

COMMAND = 19h with 1 Data Byte, Write Only

Push button register.

Used to force a port(s) turn on or turn off in any mode except OFF mode. If TPON bit in the PoE Plus register is low, or if the PSE controller is configured in Manual mode, writing a 1 at that PWONn bit location will immediately turn on the associated port, regardless of the classification and detection status and regardless of the IEEE802.3 TPON timing specification. This is also the case if TPON is set and DETn bit is 0, in semiauto mode.

If TPON bit in the PoE Plus register is set, and DETn bit (DETECT/CLASS ENABLE register) is set and while in semiauto mode, writing a 1 at a PWONn bit will turn on the associated port but only if the IEEE802.3 TPON timing specification can be met and if the detection is valid (and class is valid if enabled). TPON specification is the time from the completion of a valid detection cycle to port turn ON.

If TPON specification cannot be met, a new detection cycle is restarted, followed by a classification cycle if enabled, at the end of which the port is turned on, but only if a valid detection is returned and the IEEE802.3 TPON specification can be met. For this case, there is no additional attempt to turn on the port until this push button is reasserted. If the last detection result is not valid, the port is not turned on.

Note that in semiauto, as long as the port is kept off, detection and classification are performed continuously, if the corresponding class and detect enable bits are set.

Writing a 1 at POFFn location turns off the associated port.

Note that writing a 1 at POFFn and PWONn of same port during the same write operation turns the port off.

Also note that t_{OVLD}, t_{LIM}, t_{START}, and disconnect events have priority over the power on command. During t_{OVLD}, t_{LIM}, or t_{START} cool down cycle, any port turn on using Power Enable command will be ignored and the port will be kept off.

Turning OFF a port with this command also clears the corresponding bits in Detection Event register (CLSCn, DETCn), Fault Event register (DISFn, ICUTn), Start Event register (STRTn, ILIMn), Port n Status register (CLASS Pn, DETECT Pn), DETECT/CLASS ENABLE register (CLEn, DETEn) and Power-on Fault register (PFn). The corresponding PGCn and PECn bits of Power Event register will also be set if there is a change. The corresponding PEn and PGn bits of Power Status Register are also updated accordingly.

Figure 41. POWER ENABLE Register Format

7	6	5	4	3	2	1	0
POFF4	POFF3	POFF2	POFF1	PWON4	PWON3	PWON2	PWON1
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 21. POWER ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	POFF4–POFF1	W	0	Port power off bits
3–0	PWON4–PWON1	W	0	Port power on bits

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8.6.23 RESET Register

COMMAND = 1Ah with 1 Data Byte, Write Only

Push button register.

Writing a 1 at a bit location triggers an event while a 0 has no impact. Self-clearing bits.

Figure 42. RESET Register Format

7	6	5	4	3	2	1	0
CLRAIN	CLINP	–	RESAL	RESP4	RESP3	RESP2	RESP1
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 22. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLRAIN	W	0	Clear all interrupts bit. Writing a 1 to CLRAIN clears all event registers and all bits in the Interrupt register. It also releases the $\overline{\text{INT}}$ pin
6	CLINP	W	0	When set, it releases the $\overline{\text{INT}}$ pin without any impact on the Event registers nor on the Interrupt register.
5	–	W	0	
4	RESAL	W	0	Reset all bits when RESAL is set. Results in a state equivalent to a power-up reset. Note that the VDUV and VPUV bits (Supply Event register) follow the state of VDD and VPWR supply rails.
3–0	RESP4–RESP1	W	0	Reset port bits. Used to force an immediate port(s) turn off in any mode, by writing a 1 at the corresponding RESPn bit location(s). Turning OFF a port with this command also clears the corresponding bits in Detection Event register (CLSCn, DETCn), Fault Event register (DISFn, ICUTn), Start Event register (STRTn, ILIMn), Port n Status register (CLASS Pn, DETECT Pn), DETECT/CLASS ENABLE register (CLEn, DETEn) and Power-on Fault register (PFn). Note that the port can be turned back on immediately after a port reset; this means that any ongoing cool down cycle becomes immediately terminated once a port reset is received. The corresponding PGCn and PECn bits of Power Event register will also be set if there is a change. The corresponding PEn and PGn bits of Power Status Register are also updated accordingly.

8.6.24 ID Register

COMMAND = 1Bh with 1 Data Byte, Read/Write

Figure 43. ID Register Format

7	6	5	4	3	2	1	0
MFR ID					ICV		
R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7–3	MFR ID	R/W	01010b	Manufacture Identification number (0101,0)
2–0	ICV	R/W	011b	IC version number (011)

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8.6.25 Police 21 Configuration Register

COMMAND = 1Eh with 1 Data Byte, Read/Write

Replaces the ICUT mechanism. The threshold is defined with the Police bits and the PoE Plus register.

Figure 44. Police 21 Register Format

7	6	5	4	3	2	1	0
POL2_3	POL2_2	POL2_1	POL2_0	POL1_3	POL1_2	POL1_1	POL1_0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.26 Police 43 Configuration Register

COMMAND = 1Fh with 1 Data Byte, Read/Write

Replaces the ICUT mechanism. The threshold is defined with the Police bits and the PoE Plus register.

Figure 45. Police 43 Register Format

7	6	5	4	3	2	1	0
POL4_3	POL4_2	POL4_1	POL4_0	POL3_3	POL3_2	POL3_1	POL3_0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Police 43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	POLn_3-POLn_0	R/W	1	4-bit nibble defining I_{CUT} threshold. The result varies depending on the PoE Plus port bit. The equation defining the I_{CUT} threshold is: $I_{CUT} = (N \times IC_{STEP}) + IC_{OFFS}$ Where, when assuming 0.255-Ω Rsense resistor is used: IC_{STEP} = 20 mA (1 W resolution if at 50 V) when the associated port's PoE Plus bit is 0 IC_{STEP} = 40 mA (2 W resolution if at 50 V)when the associated port's PoE Plus bit is 1 and: IC_{OFFS} = 20 mA when the associated port's PoE Plus bit is 0 IC_{OFFS} = 320 mA (16 W if at 50 V) when the associated port's PoE Plus bit is 1 Note: When a PoEPn bit is set in PoE Plus register, the corresponding POLn bits are initially changed to 0x0. When a PoEPn bit is reset in PoE Plus register, the corresponding POLn bits are initially changed to 0xF. In both cases, the port police current threshold is the same value.

8.6.27 IEEE Power Enable Register

COMMAND = 23h with 1 Data Byte, Write Only

Used to do a port(s) turn on during semiauto mode. This command is ignored if in manual mode. Note that if at completion of this command the addressed port is not turned on, the corresponding bits in the Detect/Class Enable register (register 14h) are being set, which means that detection and classification are performed continuously, as long as the class and detect enable bits are kept set.

Writing a 1 at a TmPONn bit will turn on the associated port but only if the IEEE802.3 TPON timing specification can be met. TPON specification is the time from the completion of a valid detection cycle to port turn ON.

If TPON specification cannot be met, a new detection cycle is restarted, followed by a classification cycle, at the end of which the port is turned on, but only if a valid detection and classification is returned. For this case, there is no additional attempt to turn on the port until this push button is reasserted.

Note that a port turn on will be performed only after both its current detection and classification cycle are completed

Note that writing a 1 at T1PONn and T2PONn of same port during the same write operation is interpreted as a T1PONn.

The corresponding PGCn and PECn bits of Power Event register will also be set depending on the result, while the CLSCn and DETCn bits of Detection Event register will be set based on the result and the CLCHE and DECHE bits in the General Mask register.

Also note that t_{OVLD}, t_{LIM}, t_{START}, and disconnect events are prioritary over the power on command. During t_{OVLD}, t_{LIM}, or t_{START} cool down cycle, any port turn on using IEEE Power Enable command will be ignored and the port will be kept off.

Figure 46. IEEE Power Enable Register Format

7	6	5	4	3	2	1	0
Type 2 IEEE Power Enable Pushbutton				Type 1 IEEE Power Enable Pushbutton			
T2PON4	T2PON3	T2PON2	T2PON1	T1PON4	T1PON3	T1PON2	T1PON1
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 25. IEEE Power Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	T2PON4–T2PON1	W	0	If class 4 is detected during the first event classification, a second event classification is performed. If the last detection result is not valid or last classification result yields “over current” or is different from the first classification event result, the port is not turned on, and the STRTn bit in Start/Ilim Event register is set, while the corresponding fault code in the Power-on Fault register is written. When power-on is complete and if class 4 has been detected, the corresponding PoEPn bit in PoE Plus register is set and the value of the corresponding Police Configuration register is set to 640 mA (08h code). This is done within 5 ms of completion of inrush.
3–0	T1PON4–T1PON1	W	0	Indicates only a single-event classification is performed, even if a class 4 PD is detected. If the last detection result is not valid or last classification result yields “over current”, the port is not turned on, and the STRTn bit in Start/Ilim Event register is set, while the corresponding fault code in the Power-on Fault register is written.

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8.6.28 Power-on Fault Register

COMMAND = 24h with 1 Data Byte, Read Only

COMMAND = 25h with 1 Data Byte, Clear on Read

Figure 47. Power-on Fault Register Format

7	6	5	4	3	2	1	0
PF4		PF3		PF2		PF1	
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0	CR-0

LEGEND: R/W = Read/Write; R = Read only; W = Write only; CR = Clear on Read; -n = value after reset

Table 26. Power-on Fault Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7–0</td><td>PF4–PF1</td><td>R or CR</td><td>0</td><td>Represents the fault status of the classification and detection for port n, following an IEEE Power Enable command. These bits are cleared when port n is turned off.
PFn: the selection is as follows:
<table>
<tr><th colspan="2">Fault Code</th><th>Power-on Fault Description</th></tr>
<tr><td>0</td><td>0</td><td>No fault</td></tr>
<tr><td>0</td><td>1</td><td>Invalid detection</td></tr>
<tr><td>1</td><td>0</td><td>Classification overcurrent</td></tr>
<tr><td>1</td><td>1</td><td>Classification mismatch</td></tr>
</table></td></tr>
</table>

8.6.29 PORT RE-MAPPING Register

COMMAND = 26h with 1 Data Byte, Read/Write

Figure 48. PORT RE-MAPPING Register Format

7	6	5	4	3	2	1	0
Physical Port # of Logical Port 4		Physical Port # of Logical Port 3		Physical Port # of Logical Port 2		Physical Port # of Logical Port 1	
R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; W = Write only; CR = Clear on Read; -n = value after reset

Table 27. PORT RE-MAPPING Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7–0</td><td>Physical Port # of Logical Port n</td><td>R/W</td><td>1/0</td><td>
<p>Used to re-map ports logically due to physical board constraints. Re-mapping is between any port of a 4-port group (1-4, 5-8). All ports of a group of four must be in OFF mode prior to receiving the port re-mapping command, otherwise the command will be ignored. By default there is no re-mapping.</p>
<p>Each pair of bits corresponds to the logical port assigned.</p>
<p>The selection per port is as follows:</p>
<table>
<tr><th colspan="2">Re-Map Code</th><th>Physical Port</th><th>Package Pins</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Drain1,Gat1,Sen1</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>Drain2,Gat2,Sen2</td></tr>
<tr><td>1</td><td>0</td><td>3</td><td>Drain3,Gat3,Sen3</td></tr>
<tr><td>1</td><td>1</td><td>4</td><td>Drain4,Gat4,Sen4</td></tr>
</table>
<p>When there is no re-mapping the default value of this register is 1110,0100. The 2 MSbits with a value 11 indicate that logical port 4 is mapped onto physical port 4, the next 2 bits, 10, suggest logical port 3 is mapped onto physical port 3 and so on.</p>
<p>Note: Code duplication is not allowed – that is, Same code cannot be written into the remapping bits of more than one port – if such a value is received, it will be ignored and the chip will stay with existing configuration.</p>
<p>Note: Port remapping configuration is kept unchanged if 0x1A IC reset command is received.</p>
<p>NOTE
After port remapping, TI recommends to do at least one detection-classification cycle before next port turn on.</p>
</td></tr>
</table>

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8.6.30 Port 21 Multi Bit Priority Register

COMMAND = 27h with 1 Data Byte, Read/Write .

Figure 49. Port 21 Register Format

7	6	5	4	3	2	1	0
–	MBP2_2	MBP2_1	MBP2_0	–	MBP1_2	MBP1_1	MBP1_0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W–0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.31 Port 43 Multi Bit Priority Register

COMMAND = 28h with 1 Data Byte, Read/Write

Figure 50. Port 43 Register Format

7	6	5	4	3	2	1	0
–	MBP4_2	MBP4_1	MBP4_0	–	MBP3_2	MBP3_1	MBP3_0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W–0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Port 43 Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7–0</td><td>MBPn_2-0</td><td>R/W</td><td>0</td><td>
<p>MBPn_2-0: Multi Bit Port power priority bits, three bits per port, if 3-bit shutdown priority has been selected (MbitPrty in General Mask register is high). It is used to determine which port(s) is (are) shut down in response to a serial shutdown code received at the OSS shutdown input. A port with 000 code has highest priority. Port priority reduces as the 3-bit value increases.</p>
<p>The turn off procedure (including register bits clearing) is similar to a port reset using Reset command (1Ah register), except that it does not cancel any ongoing fault cool down time count.</p>
<p>The port priority is defined as followings:</p>
<p>OSS code ≤ MBPn_2-0 : when the OSS code is received, the corresponding port is powered off.</p>
<p>OSS code > MBPn_2-0 : OSS code has no impact on the port</p>
<table>
<tr><th colspan="3">MBPn_2-0 0x27/28 Register</th><th>Multi Bit Priority</th><th>Condition for Port Off</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Highest</td><td>OSS = ‘000’</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td><td>OSS = ‘000’ or ‘001’</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3</td><td>OSS ≤ ‘010’</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4</td><td>OSS ≤ ‘011’</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>5</td><td>OSS ≤ ‘100’</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6</td><td>OSS = any code except ‘111’</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Lowest</td><td>OSS = any code</td></tr>
</table>
</td></tr>
</table>

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8.6.32 TEMPERATURE Register

COMMAND = 2Ch with 1 Data Byte, Read Only

Figure 51. TEMPERATURE Register Format

7	6	5	4	3	2	1	0
TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. TEMPERATURE Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	TEMP7–TEMP0	R	0	Bit Descriptions: Data conversion result. The I^2C data transmission is a 1-byte transfer. 8-bit Data conversion result of temperature, from –20°C to 125°C. The update rate is around once per second. The equation defining the temperature measured is: $T = -20 + N \times T_{STEP}$ Where T_{STEP} is defined below as well as the full scale value:

Mode	Full Scale Value	T_{STEP}
Any	146.2°C	0.652°C

8.6.33 INPUT VOLTAGE Register

COMMAND = 2Eh with 2 Data Byte (LSByte first, MSByte second), Read only

Figure 52. INPUT VOLTAGE Register Format

7	6	5	4	3	2	1	0
LSB:							
VPWR7	VPWR6	VPWR5	VPWR4	VPWR3	VPWR2	VPWR1	VPWR0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	VPWR13	VPWR12	VPWR11	VPWR10	VPWR9	VPWR8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. INPUT VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
13–0	VPWR13- VPWR0	R	0	Bit Descriptions: Data conversion result. The I^2C data transmission is a 2-byte transfer. 14-bit Data conversion result of input voltage. The equation defining the voltage measured is: $V = N \times V_{STEP}$ Where V_{STEP} is defined below as well as the full scale value:

Mode	Full Scale Value	V_{STEP}
Any	60 V	3.662 mV

Note that the measurement is made between VPWR and AGND.

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8.6.34 PORT 1 CURRENT Register

COMMAND = 30h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 53. PORT 1 CURRENT Register Format

7	6	5	4	3	2	1	0
LSB:							
I1_7	I1_6	I1_5	I1_4	I1_3	I1_2	I1_1	I1_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	I1_13	I1_12	I1_11	I1_10	I1_9	I1_8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.35 PORT 2 CURRENT Register

COMMAND = 34h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 54. PORT 2 CURRENT Register Format

7	6	5	4	3	2	1	0
LSB:							
I2_7	I2_6	I2_5	I2_4	I2_3	I2_2	I2_1	I2_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	I2_13	I2_12	I2_11	I2_10	I2_9	I2_8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.36 PORT 3 CURRENT Register

COMMAND = 38h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 55. PORT 3 CURRENT Register Format

7	6	5	4	3	2	1	0
LSB:							
I3_7	I3_6	I3_5	I3_4	I3_3	I3_2	I3_1	I3_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	I3_13	I3_12	I3_11	I3_10	I3_9	I3_8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.37 PORT 4 CURRENT Register

COMMAND = 3Ch with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 56. PORT 4 CURRENT Register Format

7	6	5	4	3	2	1	0
LSB:							
I4_7	I4_6	I4_5	I4_4	I4_3	I4_2	I4_1	I4_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	I4_13	I4_12	I4_11	I4_10	I4_9	I4_8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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Table 31. PORT 4 CURRENT Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>13-0</td><td>In_13- In_0</td><td>R</td><td>0</td><td>Bit Descriptions: Data conversion result. The I^{2}C data transmission is a 2-byte transfer.
Note that the conversion is done using a TI proprietary multi-slope integrating converter.
14-bit Data conversion result of current for port n. The update rate is around once per 100 ms in port powered state.
The equation defining the current measured is:
$I = N \times I_{STEP}$
Where I_{STEP} is defined below as well as the full scale value, according to the operating mode:
<table><tr><th>Mode</th><th>Full Scale Value</th><th>I_{STEP}</th></tr><tr><td>Port Powered and Classification</td><td>1 A (with 0.255 Ω Rsense)</td><td>61.035 µA</td></tr></table>Note: in any of the following cases, the result through I^{2}C interface is automatically 0000
port is in OFF mode
port is OFF while in semiauto mode and detect/class is not enabled
port is OFF while in semiauto mode and detection result is incorrect
In manual mode, if detect/class has been enabled at least once, the register retains the result of the last measurement</td></tr>
</table>

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8.6.38 PORT 1 VOLTAGE Register

COMMAND = 32h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 57. PORT 1 VOLTAGE Register Format

7	6	5	4	3	2	1	0
LSB:							
V1_7	V1_6	V1_5	V1_4	V1_3	V1_2	V1_1	V1_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	V1_13	V1_12	V1_11	V1_10	V1_9	V1_8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.39 PORT 2 VOLTAGE Register

COMMAND = 36h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 58. PORT 2 VOLTAGE Register Format

7	6	5	4	3	2	1	0
LSB:							
V2_7	V2_6	V2_5	V2_4	V2_3	V2_2	V2_1	V2_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	V2_13	V2_12	V2_11	V2_10	V2_9	V2_8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.40 PORT 3 VOLTAGE Register

COMMAND = 3Ah with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 59. PORT 3 VOLTAGE Register Format

7	6	5	4	3	2	1	0
LSB:							
V3_7	V3_6	V3_5	V3_4	V3_3	V3_2	V3_1	V3_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	V3_13	V3_12	V3_11	V3_10	V3_9	V3_8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.41 PORT 4 VOLTAGE Register

COMMAND = 3Eh with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 60. PORT 4 VOLTAGE Register Format

7	6	5	4	3	2	1	0
LSB:							
V4_7	V4_6	V4_5	V4_4	V4_3	V4_2	V4_1	V4_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MSB:							
–	–	V4_13	V4_12	V4_11	V4_10	V4_9	V4_8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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Table 32. PORT 4 VOLTAGE Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>13-0</td><td>Vn_13- Vn_0</td><td>R</td><td>0</td><td>Bit Descriptions: Data conversion result. The I^{2}C data transmission is a 2-byte transfer.
The equation defining the voltage measured is:
$V = N \times V_{STEP}$
Where V_{STEP} is defined below as well as the full scale value:
<table>
<tr><th>Mode</th><th>Full Scale Value</th><th>V_{STEP}</th></tr>
<tr><td>Port Powered</td><td>60 V</td><td>3.662 mV</td></tr>
</table>
Note that a powered port voltage measurement is made between VPWR and DRAINn.
Note: if a port is OFF, the result through I^{2}C interface is automatically 0000.</td></tr>
</table>

8.6.42 PoE Plus Register

COMMAND = 40h with1 Data Byte Read/Write

Figure 61. PoE Plus Register Format

7	6	5	4	3	2	1	0
PoEP4	PoEP3	PoEP2	PoEP1	–	–	–	TPON
R/W-0	R/W-0	R/W-0	R/W-0	–	–	–	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. PoE Plus Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	PoEP4- PoEP1	R/W	0	When set, this activates the PoE Plus mode for a port which increases its I_{LIM} and I_{SHORT} levels to around 2 ½ times their normal settings, as shown in Figure 18. Also the PoE Plus bit is used with the Police Configuration register to define I_{CUT} threshold. See Police Configuration register for more details on the subject. Note that the fault timer starts when the I_{LIM} or I_{CUT} (if ICUT is enabled) threshold is exceeded. Also see the Port Power Priority/ICUT Disable register. Notes: 1) At port turn on, the inrush current profile remains the same, whatever the state of the PoEPn bit, as shown in Figure 17. 2) When a PoEPn bit is set, the corresponding POLn bits in Police Configuration register are initially changed to 0x0. When a PoEPn bit is reset, the corresponding POLn bits in Police Configuration register are initially changed to 0xF. In both cases, the port police current threshold is the same value. 3) When a PoEPn bit is deasserted, the t_{LIM} used for the associated port is always the nominal value (~60 ms). If PoEPn bit is asserted, then t_{LIM} for associated port is programmable as defined in the Timing Configuration register. 4) If a port is turned on by use of the Type 2 IEEE Power Enable Pushbutton, the PSE does the following. When power-on is complete and if class 4 has been detected, the corresponding PoEPn bit is set and the value of the corresponding Police Configuration register is set to 640 mA (08h code). This is done within 5 ms of completion of inrush.
0	TPON	R/W	0	When set, if DETn bit (DETECT/CLASS ENABLE register) is set and while in semiauto mode, writing a 1 at a PWONn bit in the Power Enable register will turn on a port after the current detection (and class is valid if enabled) cycle is completed but only if the IEEE802.3 TPON timing specification can be met. TPON specification is the time from the completion of a valid detection cycle to port turn ON. If TPON specification cannot be met, a new detection cycle is restarted, followed by a classification cycle, at the end of which the port is turned on, but only if a valid detection is returned. For this case, there is no additional attempt to turn on the port until this push button is reasserted. If TPON bit is low, writing a 1 at a PWONn bit in the Power Enable register will turn on the associated port immediately, regardless of IEEE802.3 TPON timing specification and regardless of the detection result.

8.6.43 FIRMWARE REVISION

COMMAND = 41h with 1 Data Byte, Read Only

Figure 62. FIRMWARE REVISION Register Format

7	6	5	4	3	2	1	0
FRV							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. FIRMWARE REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	FRV	R		Firmware Revision number

8.6.44 I2C WATCHDOG Register

COMMAND = 42h with 1 Data Byte, Read/Write

The I^2C watchdog timer monitors the I^2C clock line in order to prevent hung software situations that could leave ports in a hazardous state. The timer can be reset by either edge on SCL input. If the watchdog timer expires, all ports will be turned off and WDS bit will be set. The nominal watchdog time-out period is 2 seconds.

Figure 63. I2C WATCHDOG Register Format

7	6	5	4	3	2	1	0
–	–	–	IWDD3	IWDD2	IWDD1	IWDD0	WDS
–	–	–	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. I2C WATCHDOG Register Field Descriptions

Bit	Field	Type	Reset	Description
4–1	IWDD3–IWDD0	R/W	1011b	I^2C Watchdog disable. When equal to 1011b, the watchdog is masked. Otherwise, it is umasked and the watchdog is operational.
0	WDS	R/W	0	I^2C Watchdog timer status, valid even if the watchdog is masked. When set, it means that the watchdog timer has expired without any activity on I^2C clock line. Writing 0 at WDS location clears it. Note that when the watchdog timer expires and if the watchdog is unmasked, all ports are also turned off.

When the ports are turned OFF due to I^2C watchdog, the corresponding bits in Detection Event register (CLSCn, DETCn), Fault Event register (DISFn, ICUTn), Start Event register (STRTn, ILIMn), Port n Status register (CLASS Pn, DETECT Pn), DETECT/CLASS ENABLE register (CLEn, DETEn) and Power-on Fault register (PFn) are also cleared.

The corresponding PGCn and PECn bits of Power Event register will also be set if there is a change. The corresponding PEn and PGn bits of Power Status Register are also updated accordingly.

NOTE

If the I^2C watchdog timer has expired, the Temperature and Input voltage registers will stop being updated until the WDS bit is cleared. The WDS bit must then be cleared to allow these registers to work normally.

8.6.45 DEVICE ID Register

COMMAND = 43h with 1 Data Byte, Read Only

Figure 64. DEVICE ID Register Format

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="3">DID</td><td colspan="5">SR</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. DEVICE ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7–5	DID	R	110b	Device ID number (110)
4–0	SR	R		Silicon Revision number

8.6.46 PORT 1 DETECT RESISTANCE Register

COMMAND = 44h with 1 Data Byte, Read Only

Figure 65. PORT 1 DETECT RESISTANCE Register Format

7	6	5	4	3	2	1	0
R1_7	R1_6	R1_5	R1_4	R1_3	R1_2	R1_1	R1_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.47 PORT 2 DETECT RESISTANCE Register

COMMAND = 45h with 1 Data Byte, Read Only

Figure 66. PORT 2 DETECT RESISTANCE Register Format

7	6	5	4	3	2	1	0
R2_7	R2_6	R2_5	R2_4	R2_3	R2_2	R2_1	R2_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.48 PORT 3 DETECT RESISTANCE Register

COMMAND = 46h with 1 Data Byte, Read Only

Figure 67. PORT 3 DETECT RESISTANCE Register Format

7	6	5	4	3	2	1	0
R3_7	R3_6	R3_5	R3_4	R3_3	R3_2	R3_1	R3_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.49 PORT 4 DETECT RESISTANCE Register

COMMAND = 47h with 1 Data Byte, Read Only

Figure 68. PORT 4 DETECT RESISTANCE Register Format

7	6	5	4	3	2	1	0
R4_7	R4_6	R4_5	R4_4	R4_3	R4_2	R4_1	R4_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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Table 37. PORT 4 DETECT RESISTANCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Rn_7- Rn_0	R	0	8-bit data conversion result of detection resistance for port n. Most recent 2-point Detection Resistance measurement result. The I^2C data transmission is a 1-byte transfer. Note that the register content is not cleared at port turn off. The equation defining the resistance measured is: $R = N \times R_{STEP}$ Where R_{STEP} is defined below as well as the full scale value: **Useable Resistance Range** / R_{STEP}: 2 kΩ to 50 kΩ / 195.3125 Ω

Useable Resistance Range	R_{STEP}
2 kΩ to 50 kΩ	195.3125 Ω

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Introduction to PoE

Power-over-Ethernet (PoE) is a means of distributing power to Ethernet devices over the Ethernet cable using either data or spare pairs. PoE eliminates the need for power supplies at the Ethernet device. Common applications of PoE are security cameras, IP Phones and PDA chargers. The host or mid-span equipment that supplies power is the power source equipment (PSE). The load at the Ethernet connector is the powered device (PD). PoE protocol between PSE and PD controlling power to the load is specified by IEEE Std 802.3at-2009. Transformers are used at Ethernet host ports, mid-spans and hubs, to interface data to the cable. A DC voltage can be applied to the center tap of the transformer with no effect on the data signals. As in any power transmission line, a relatively high 48 V is used to keep current low, minimize the effect of IR drops in the line and preserve power to the load. Standard POE delivers approximately 13 W to a type 1 PD, and 25.5 W to a type 2 PD.

9.1.2 TPS2388 Application

The TPS2388 is an 8-port, IEEE 802.3at PoE PSE controller and can be used in high port count semiauto or fully micro-controller managed applications (The MSP430G2553 micro-controller is recommended for most applications). Subsequent sections describe detailed design procedures for applications with different requirements including host control.

The schematic of Figure 71 depicts semiauto mode operation of the TPS2388, providing functionality to power PoE loads. In Figure 71 the TPS2388 can do the following:

1. Performs load detection.
2. Performs classification including type-2 (two-finger) of up to Class 4 loads.
3. Enables power with protective foldback current limiting, and POLICE (I_{CUT}) value.
4. Shuts down in the event of fault loads and shorts.
5. Performs Maintain Power Signature function to insure removal of power if load is disconnected.
6. Undervoltage lock out occurs if VPWR falls below VPUV_F (typical 26.5 V).

Following a power-off command, disconnect or shutdown due to a start, ICUT or ILIM fault, the port powers down. Following port power off due to a power off command or disconnect, the TPS2388 will restart a detection cycle if commanded to do so through I^2C bus. If the shutdown is due to a start, ICUT or ILIM fault, the TPS2388 enters into a cool-down period during which any Detect/Class Enable Command for that port will be delayed. At the end of cool down cycle, one or more detection/class cycles are automatically restarted if the class and/or detect enable bits are set.

9.1.3 Kelvin Current Sensing Resistor

Load current in each PSE port is sensed as the voltage across a low-end current-sense resistor with a value of 255 mΩ. For more accurate current sensing, kelvin sensing of the low end of the current-sense resistor is provided through pins KSENSA for ports 1 and 2, KSENSB for ports 3 and 4, KSENSC for ports 5 and 6 and KSENSD for ports 7 and 8.

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Application Information (continued)

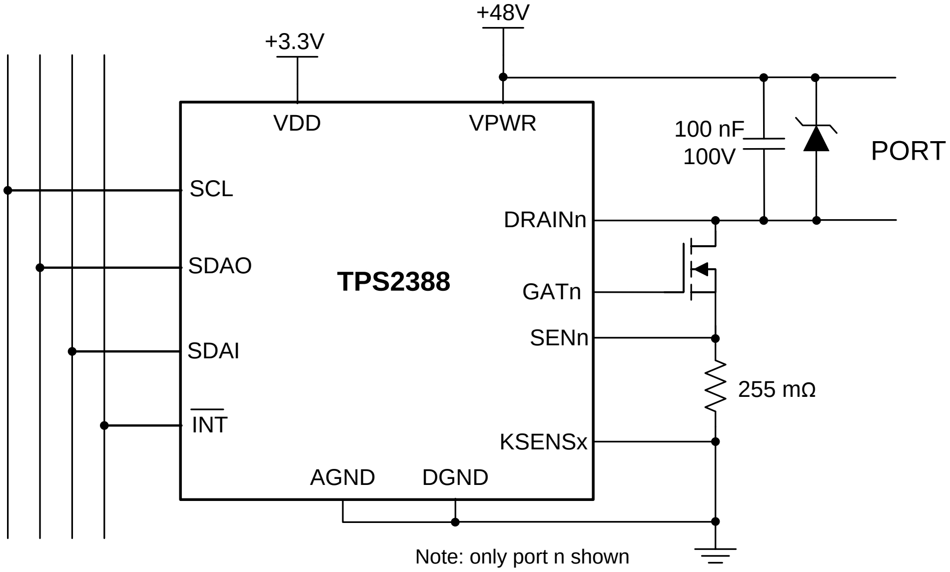

Figure 69. Kelvin Current-Sense Connection

9.1.4 Connections on Unused Ports

On unused ports, it is recommended to ground the SENx pin and leave the GATx pin open. DRAINx pins can be grounded or left open (leaving open may slightly reduce power consumption). Figure 70 shows an example of an unused PORT4.

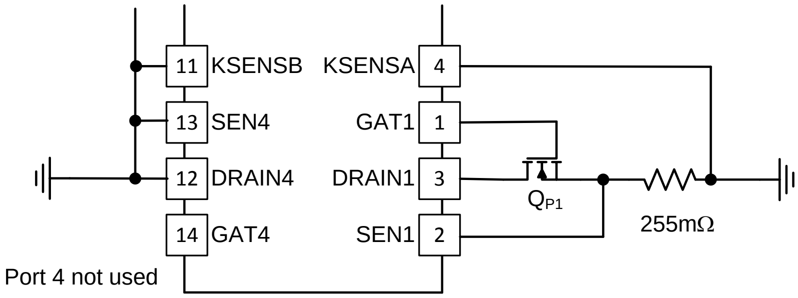

Figure 70. Unused PORT4 Connections

9.2 Typical Application

This typical application shows an eight port, semiauto mode application using MSP430 microcontroller. Operation in any mode requires I^{2}C host support. The TPS2388 provides useful telemetry in multi-port applications to aid in implementing port power management.

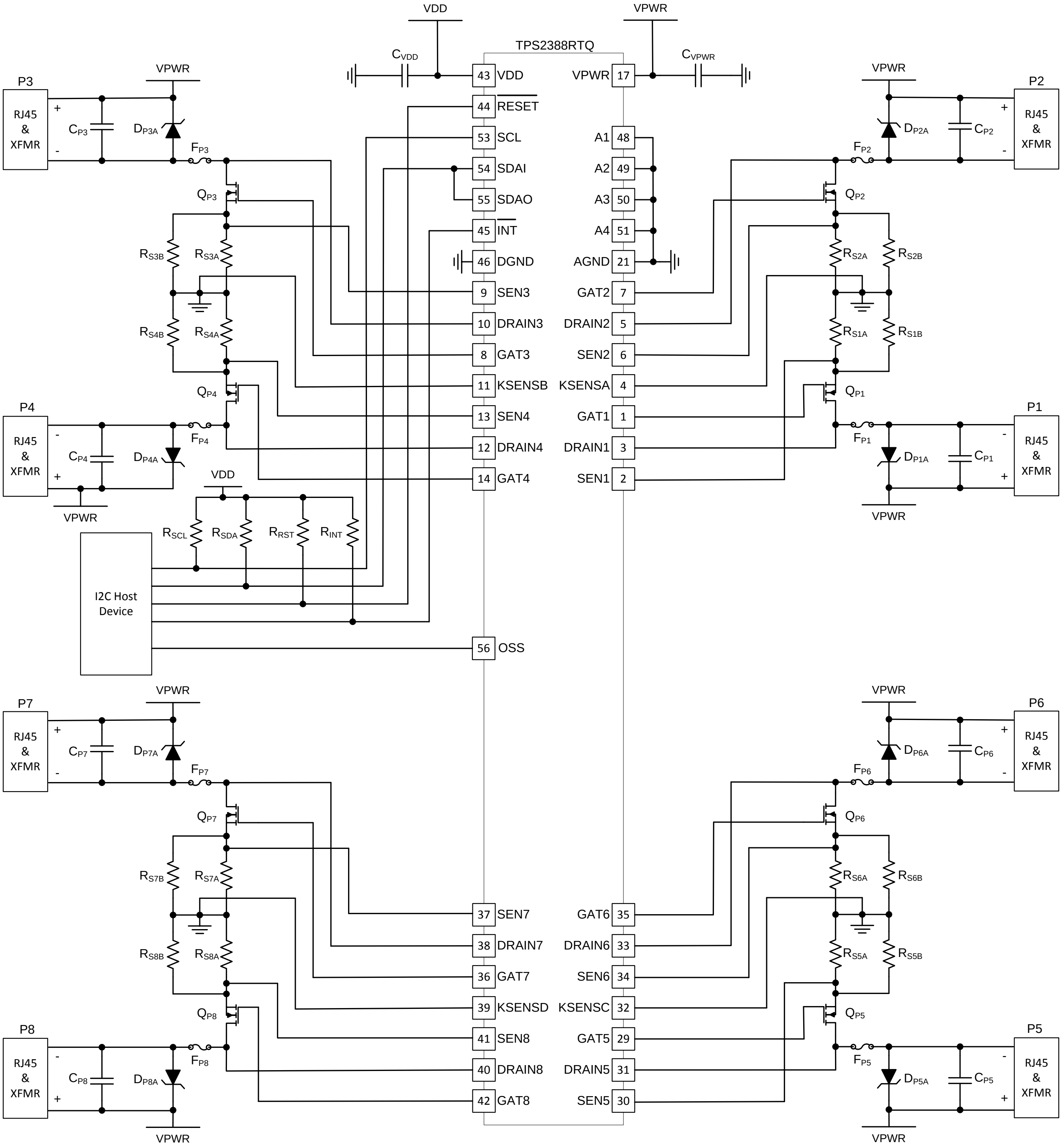

Figure 71. Eight Port Semiauto Mode Application

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Typical Application (continued)

9.2.1 Design Requirements

The $\overline{\text{RESET}}$ pin may be connected to the micro-controller if an external RESET is required or connected directly to VDD. TPS2388 devices are used in the eight port configuration and are managed by the I^2C host device. The I^2C address for TPS2388 is programmed using the A4..A1 pins.

9.2.2 Detailed Design Procedure

9.2.2.1 Power Pin Bypass Capacitors

- **C_{VPWR}:** 0.1 μF, 100 V, X7R ceramic at pin 17 (VPWR)
- **C_{VDD}:** 0.1 μF, 50 V, X7R ceramic at pin 43 (VDD)

9.2.2.2 Per Port Components

- **C_{Pn}**: 0.1-μF, 100-V, X7R ceramic between VPWR and Pn-
- **R_{SnA} / R_{SnB}**: The port current sense resistors are a combination of two 0.51-Ω, 1% resistors in parallel (0.255 Ω). Dual 0.51-Ω, 1%, 0.25-W resistors in an 0805 SMT package are recommended. If a nominal 640 mA Policing (I_{CUT}) threshold is selected, the maximum power dissipation for the resistor pair becomes approximately 115 mW (~57 mW each).
- **Q_{Pn}**: The port MOSFET can be a small, inexpensive device with average performance characteristics. BV_{DSS} should be 100 V minimum. Target a MOSFET $R_{DS(on)}$ at V_{GS} = 10 V of between 50 mΩ and 150 mΩ. The MOSFET GATE charge (Q_G) and input capacitance (C_{ISS}) should be less than 50 nC and 2000 pF respectively. The maximum power dissipation for Q_{Pn} with RDS(on) = 100 mΩ at 640 mA nominal policing (I_{CUT}) threshold is approximately 45 mW.
- **F_{Pn}**: The port fuse should be a slow blow type rated for at least 60 VDC and above ~2 x I_{CUT}(max). The cold resistance should be below 200 mΩ to reduce the DC losses. The power dissipation for FPn with a cold resistance of 180 mΩ at maximum I_{CUT} is approximately 81 mW.
- **D_{PnA}**: The port TVS should be rated for the expected port surge environment. D_{PnA} should have a minimum reverse standoff voltage of 58 V, peak pulse power rating of 600 W, and a maximum clamping voltage of less than 95 V at the expected peak surge current

9.2.2.3 System Level Components (not shown in the schematic diagrams)

The system TVS and bulk VPWR capacitance work together to protect the PSE system from surge events which could cause VPWR to surge above 70 V. The TVS and bulk capacitors should be placed on the PCB such that all TPS2388 ports are adequately protected.

- **TVS:** The system TVS should have a minimum reverse standoff voltage of 58 V and a peak pulse power rating of 600 W or 1500 W depending on the total number of system ports and amount of bulk VPWR capacitance used. Together with the VPWR bulk capacitance, the TVS must prevent the VPWR rail from exceeding 70 V.
- **Bulk Capacitor:** The system bulk capacitor(s) should be rated for 100 V and can be of aluminum electrolytic type. Two 47-μF capacitors can be used for each TPS2388 on board.
- **Distributed Capacitance:**In higher port count systems, it may be necessary to distribute 1-uF, 100-V, X7R ceramic capacitors across the 48-V power bus. One capacitor per each TPS2388 pair is recommended.
- **Digital I/O Pullup Resistors:** $\overline{\text{RESET}}$ and A1-A4 are internally pulled up to VDD, while OSS is internally pulled down, each with a 50-kΩ (typical) resistor. A stronger pull-up/down resistor can be added externally such as a 10 kΩ, 1%, 0.063 W type in a SMT package. SCL, SDAI, SDAO, and INT require external pull-up resistors within a range of 1 kΩ to 10 kΩ depending on the total number of devices on the bus .
- **Ethernet Data Transformer (per port):** The Ethernet data transformer must be rated to operate within the IEEE802.3at standard in the presence of the DC port current conditions. The transformer is also chosen to be compatible with the Ethernet PHY. The transformer may also be integrated into the RJ45 connector and cable terminations.
- **RJ45 Connector (per port):** The majority of the RJ45 connector requirements are mechanical in nature and include tab orientation, housing type (shielded or unshielded), or highly integrated. An integrated RJ45 consists of the Ethernet data transformer and cable terminations at a minimum. The integrated type may also contain the port TVS and common mode EMI filtering.

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Typical Application (continued)

- **Cable Terminations (per port):** The cable terminations typically consist of series resistor (usually 75 Ω) and capacitor (usually 10 nF) circuits from each data transformer center tap to a common node which is then bypassed to a chassis ground (or system earth ground) with a high-voltage capacitor (usually 1000 pF to 4700 pF at 2 kV).

9.2.3 Application Curves

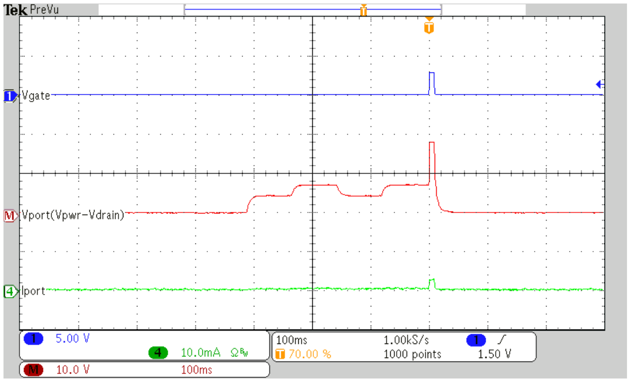

Figure 72. Startup With Valid PD (25 kΩ and 0.1 µF), Class 0

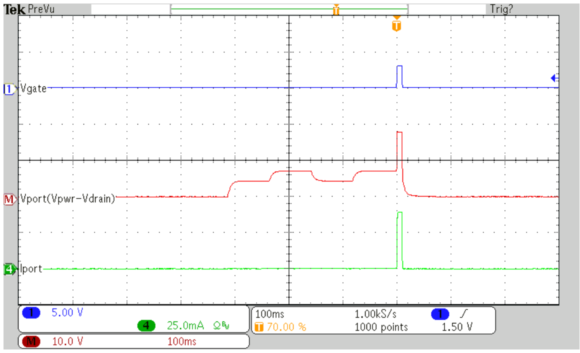

Figure 73. Startup With Valid PD (25 kΩ and 0.1 µF), Class 3

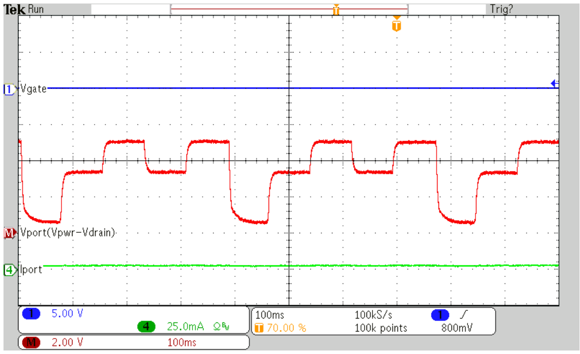

Figure 74. Detection With Invalid PD (15 kΩ and 0.1 µF)

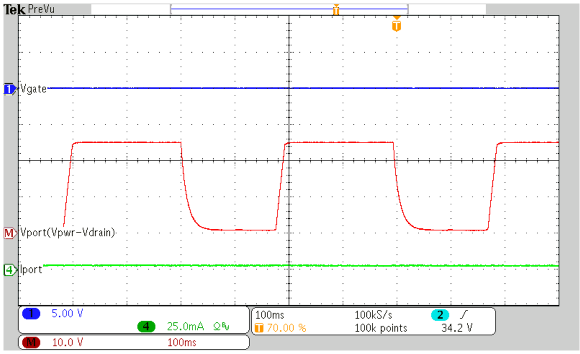

Figure 75. Detection With Invalid PD (Open Circuit)

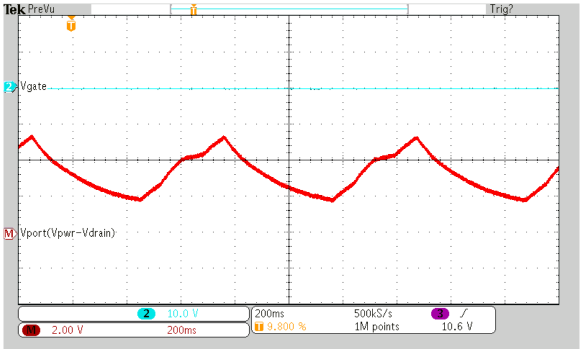

Figure 76. Detection With Invalid PD (25 kΩ and 10 µF)

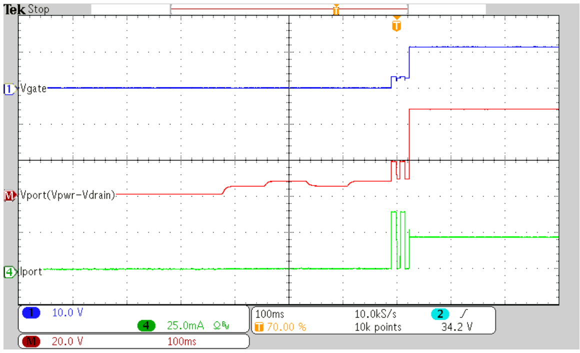

Figure 77. 2-Event Class and Startup With Valid PD

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Typical Application (continued)

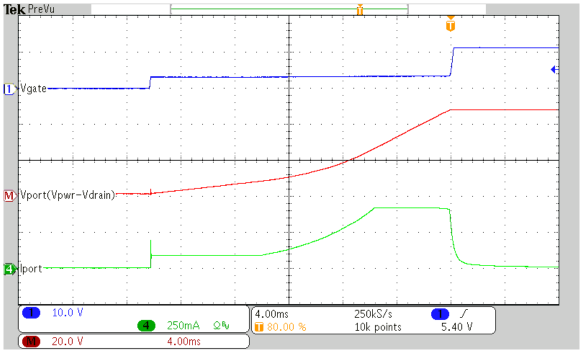

Figure 78. Powering Up into a 100-µF Load

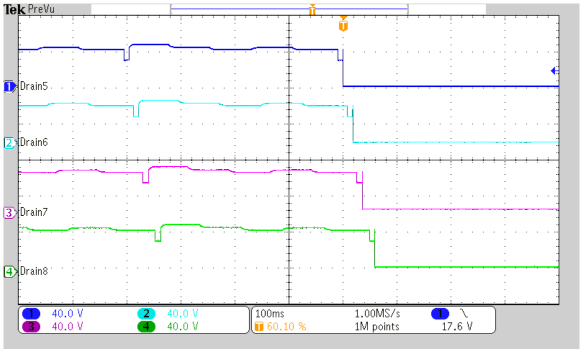

Figure 79. All Ports Power-On With TPON Bit Set

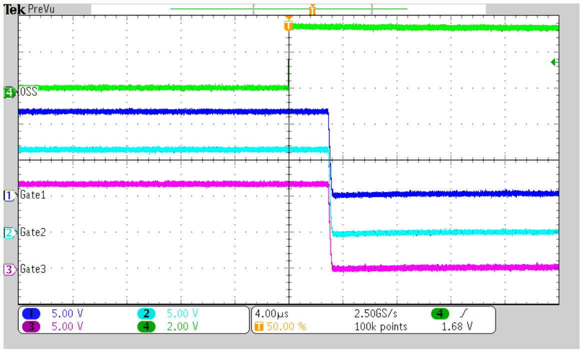

Figure 80. All Ports Fast Shutdown from OSS Input

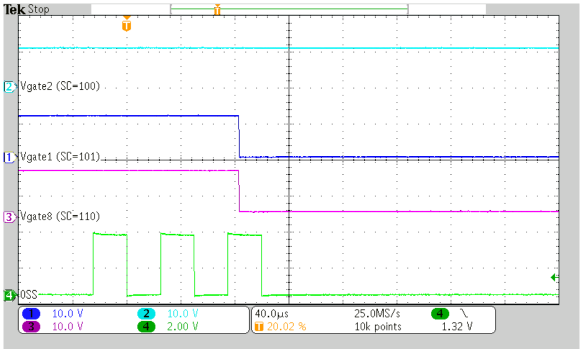

Figure 81. Ports Fast Shutdown from 3-Bit OSS Input

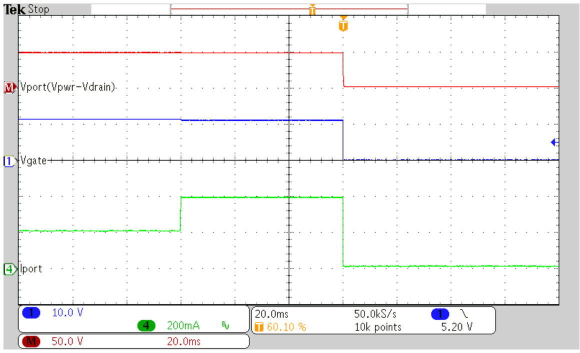

Figure 82. Overcurrent (ICUT) Timeout

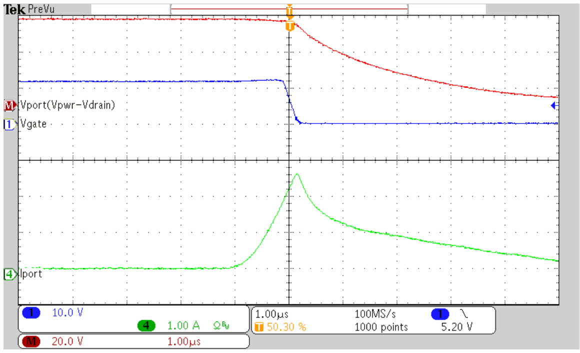

Figure 83. Rapid Response to a 1-Ω Short - 802.3af Mode

Typical Application (continued)

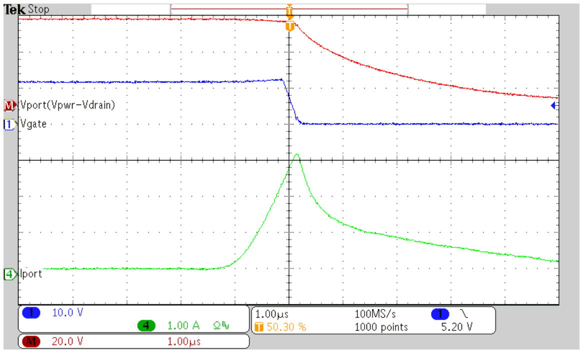

Figure 84. Rapid Response to a 1-Ω Short - PoE+ Mode

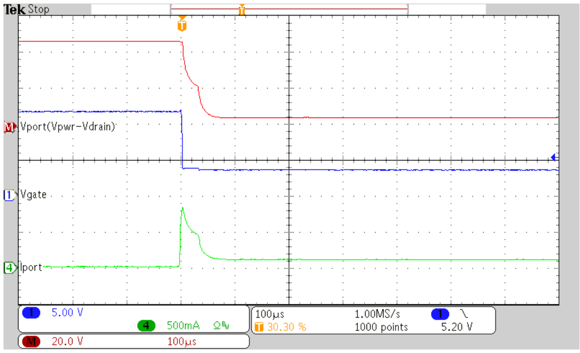

Figure 85. Response to a 50-Ω Load - 802.3af Mode

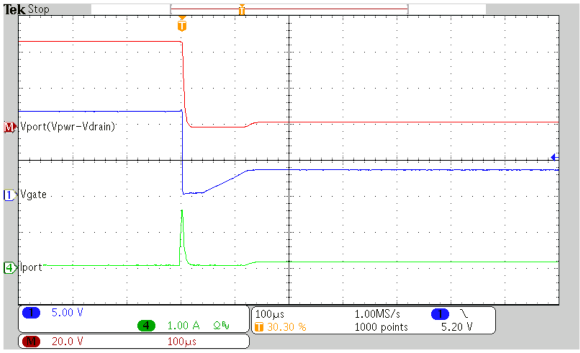

Figure 86. Response to a 25-Ω Load - PoE+ Mode

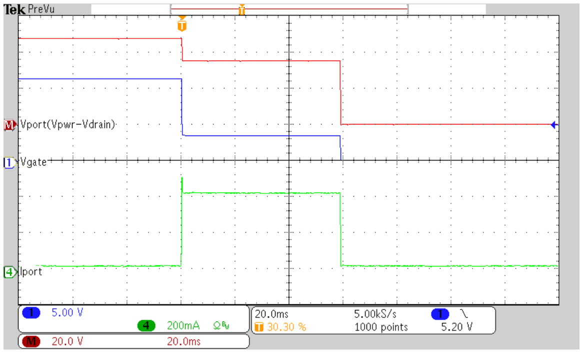

Figure 87. Current Limit Timeout - 802.3af Mode, 85-Ω Load

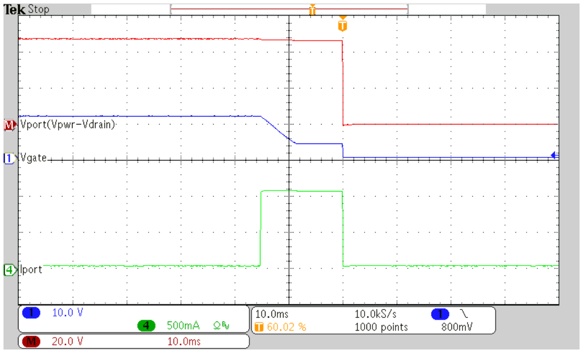

Figure 88. Current Limit 15-ms Timeout - PoE+ Mode, 45-Ω Load

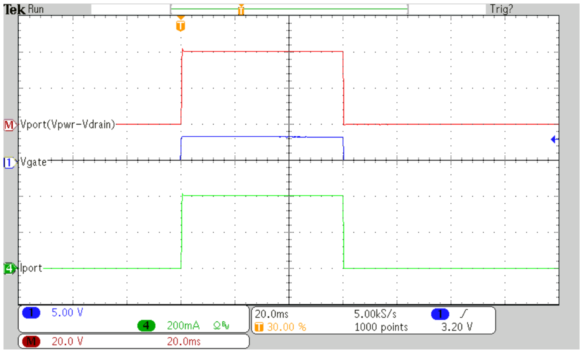

Figure 89. Inrush Fault Timeout - 100-Ω Load

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Typical Application (continued)

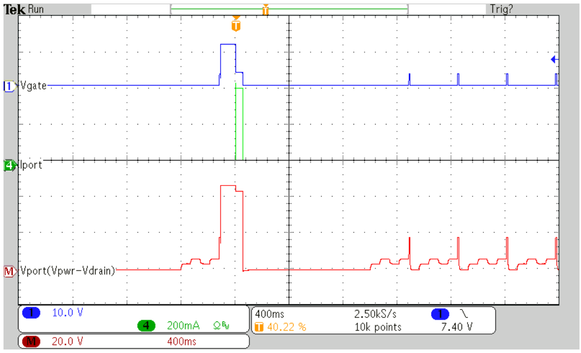

Figure 90. Current Limit Timeout Restart Delay

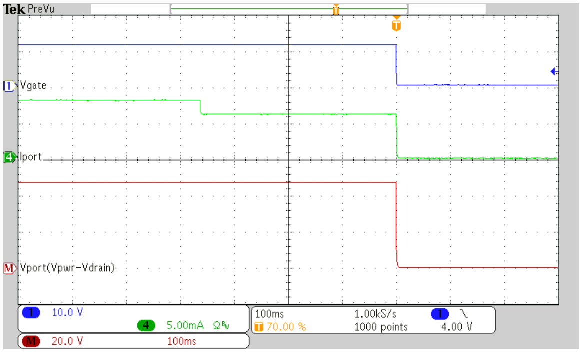

Figure 91. Response to 8-mA to 6-mA Load, DC Disconnect Enabled

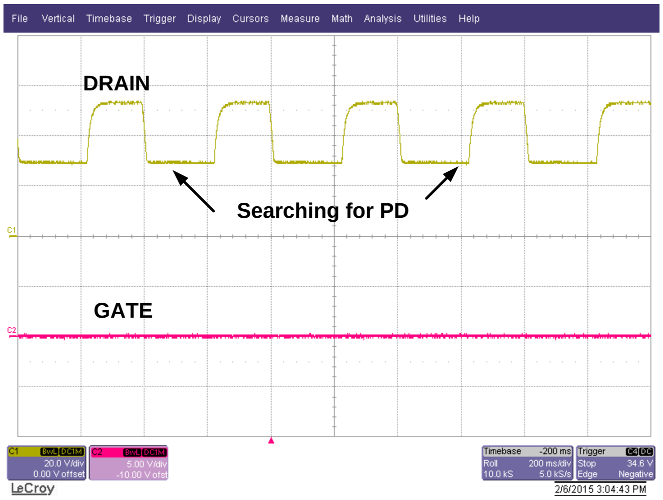

Figure 92. Detection With Open Circuit

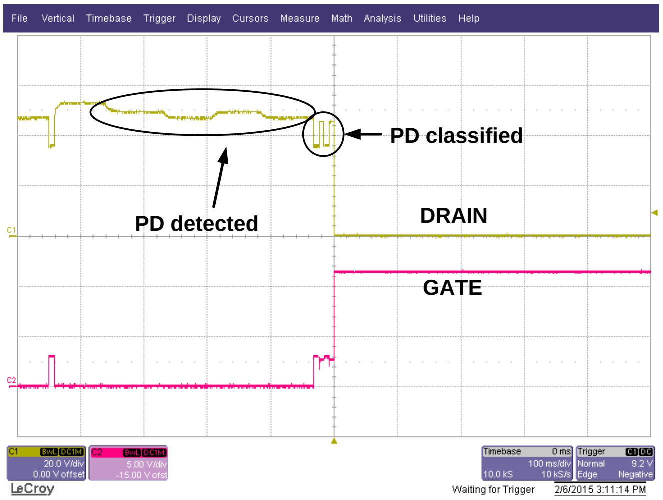

Figure 93. Detection, 2-Event Class and Port Turn On

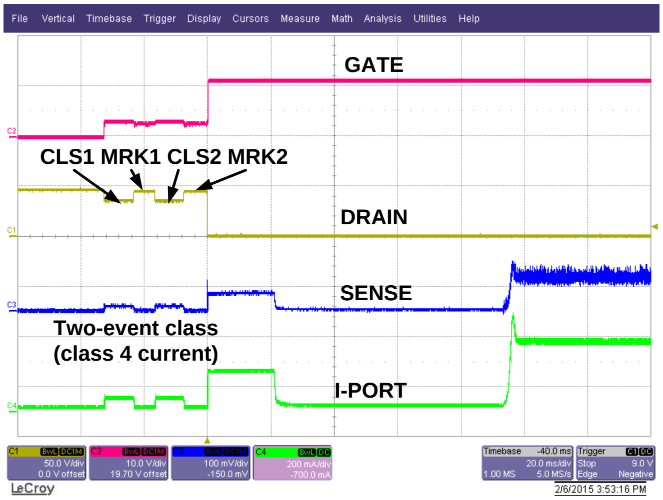

Figure 94. 2-Event Class and Port Turn On

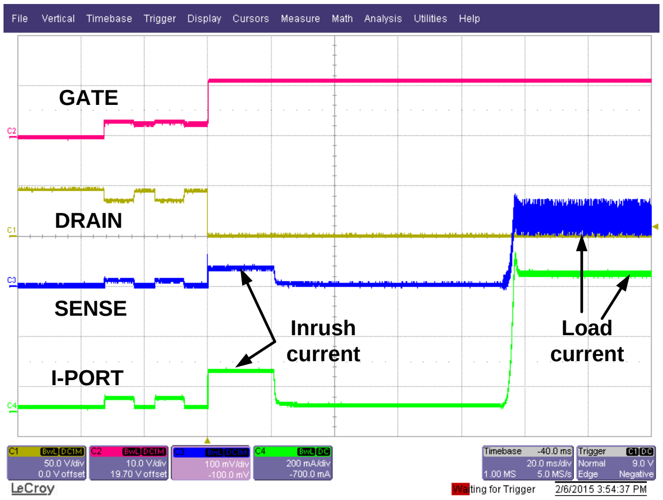

Figure 95. 2-Event Class and Port Turn On

10 Power Supply Recommendations

10.1 VDD

The recommended VDD supply voltage requirement is 3.3 V, ±0.3 V. TPS2388 requires approximately 6 mA typical and 12 mA maximum from the VDD supply. The VDD supply can be generated from VPWR with a buck-type regulator (LM5007 or LM5019 based) for a higher port count PSE using multiple TPS2388 devices operating in semiauto mode. The power supply design must ensure the VDD rail rises monotonically through the VDD UVLO thresholds without any droop under the UVLO_fall threshold as the loads are turned on. This is accomplished with proper bulk capacitance across the VDD rail for the expected load current steps over worst case design corners. Furthermore, the combination of decoupling capacitance and bulk storage capacitance must hold the VDD rail above the UVLO_fall threshold during any expected transient outages once power is applied.

10.2 VPWR

The recommended VPWR supply voltage requirement is 44 V to 57 V. A power supply with a nominal 48-V or 54-V output can support both type 1 and type 2 PD requirements. The output current required from the VPWR supply depends on the number and type of ports required in the system. The TPS2388 can be configured for type 1 and type 2 ports and the current limit is set proportionally. I_{CUT} is programmable, for example for a type 1 port it can be 380 mA , ±5%, while for a type 2 port it can be 640 mA, ±5%. Size the VPWR supply accordingly for the number and type of ports to be supported. As an example, the VPWR power supply rating should be greater than 3.2 A for eight type 1 ports or greater than 5.5 A for eight type 2 ports, assuming maximum port and standby currents.

11 Layout

11.1 Layout Guidelines

11.1.1 Port Current Kelvin Sensing

KSENSA is shared between SEN1 and SEN2, KSENSB is shared between SEN3 and SEN4, KSENSC is shared between SEN5 and SEN6, and KSENSD is shared between SEN7 and SEN8. To optimize the accuracy of the measurement, the PCB layout must be done carefully to minimize impact of PCB trace resistance. Refer to as an example.

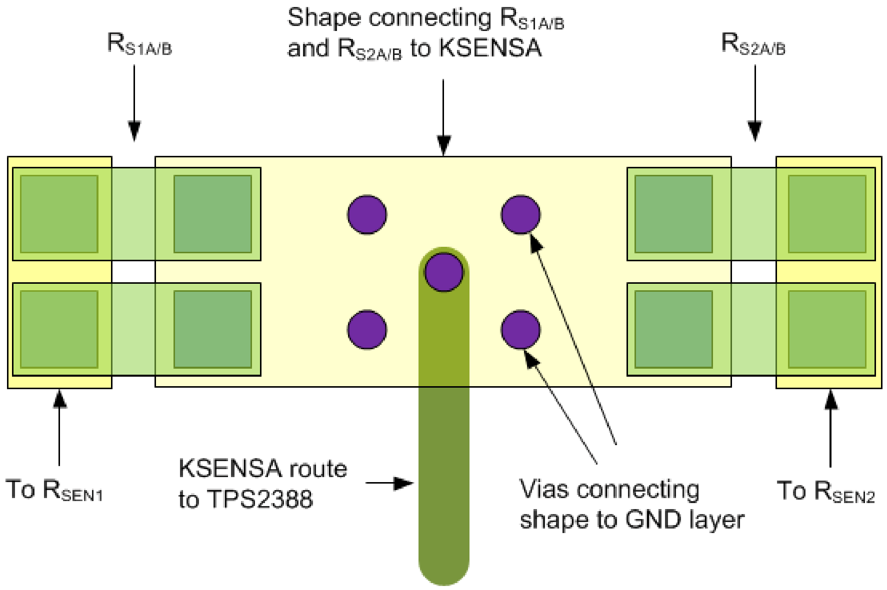

Figure 96. Kelvin Sense Layout Example

11.2 Layout Example

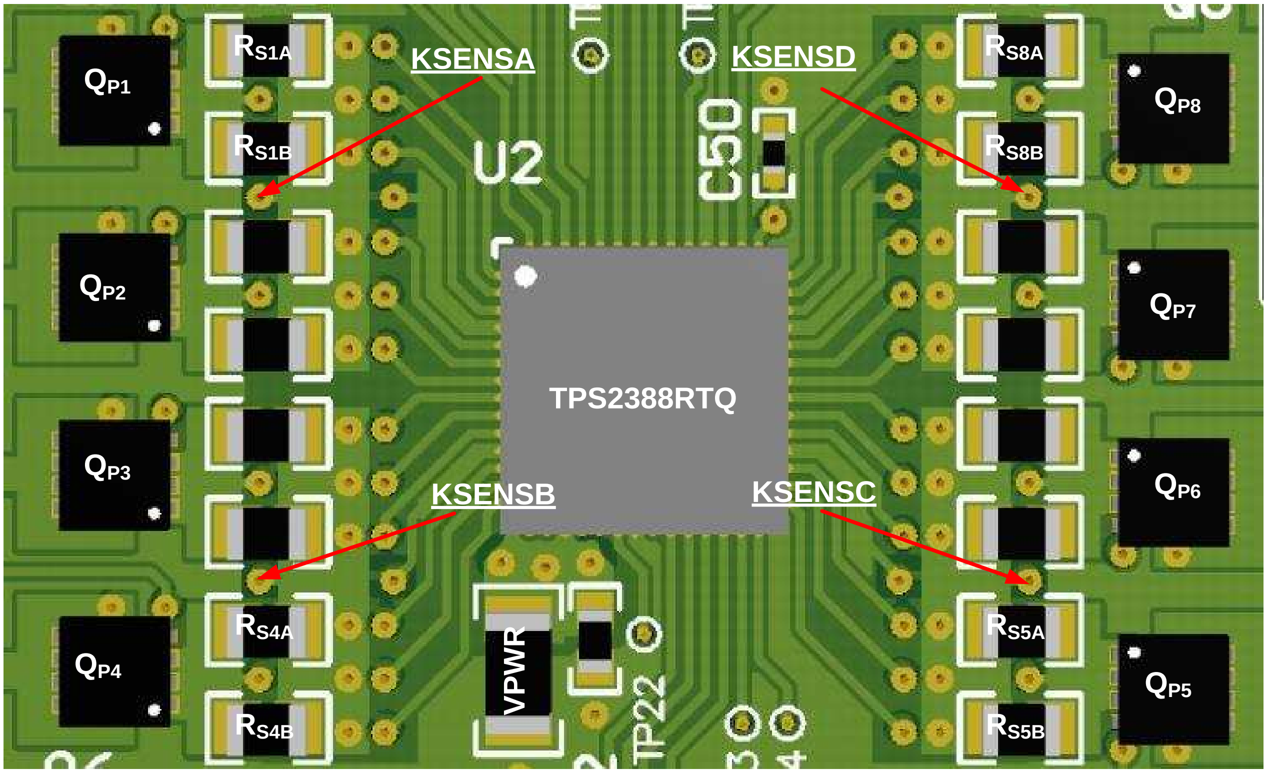

Figure 97. Eight Port Layout Example (Top Side)

11.2.1 Component Placement and Routing Guidelines

11.2.1.1 Power Pin Bypass Capacitors

- **C_{VPWR}:** Place close to pin 17 (VPWR) and connect with low inductance traces and vias according to Figure 97.
- **C_{VDD}:** Place close to pin 43 (VDD) and connect with low inductance traces and vias according to Figure 97

11.2.1.2 Per-Port Components

- **R_{SnA} / R_{SnB}:** Place according to in a manner that facilitates a clean Kelvin connection with KSENSEA/B/C/D.
- **Q_{Pn}:** Place Q_{Pn} around the TPS2388 as illustrated in Figure 97. Provide sufficient copper from Q_{Pn} drain to F_{Pn}.
- **F_{Pn}, C_{Pn}, D_{PnA}, D_{PnB}:** Place this circuit group near the RJ45 port connector (or port power interface if a daughter board type of interface is used as illustrated in Figure 97). Connect this circuit group to Q_{Pn} drain or GND (TPS2388- AGND) using low inductance traces.

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

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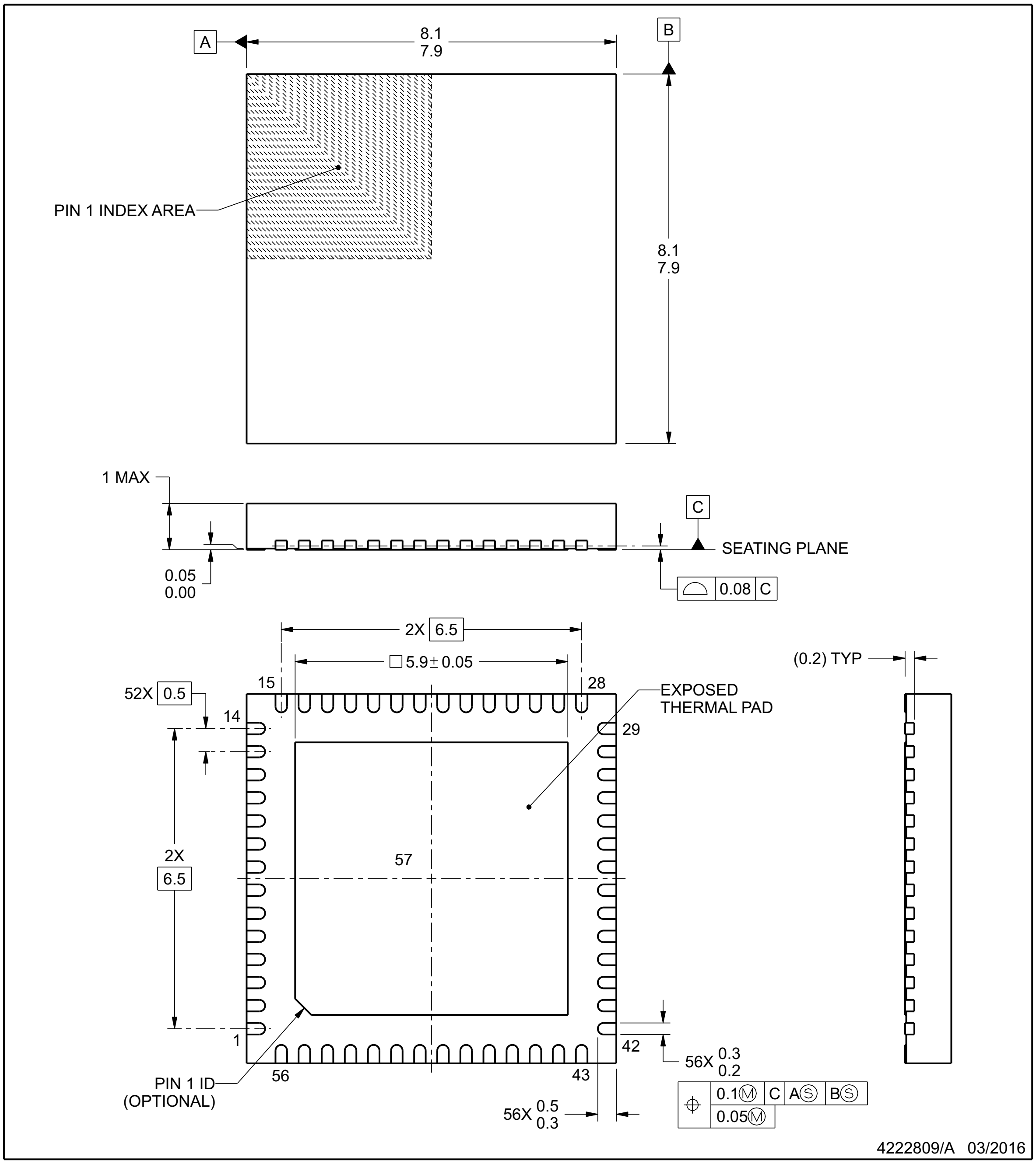
PACKAGE OUTLINE

RTQ0056H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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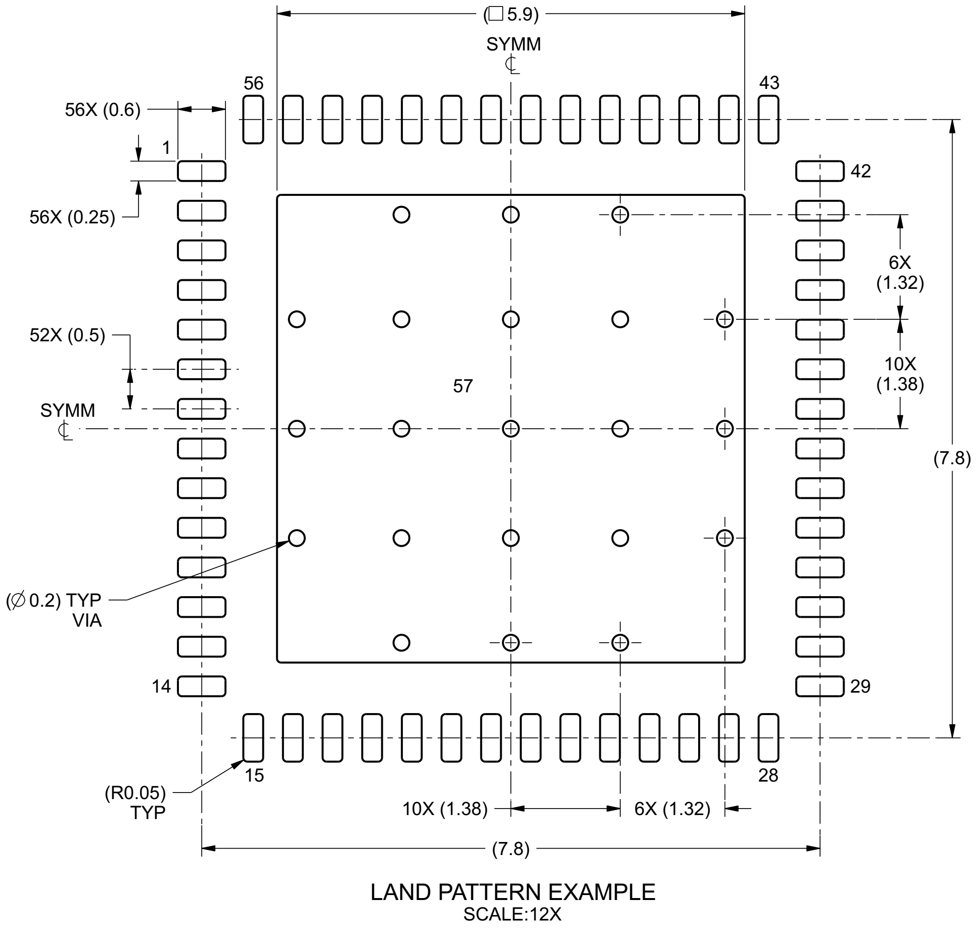
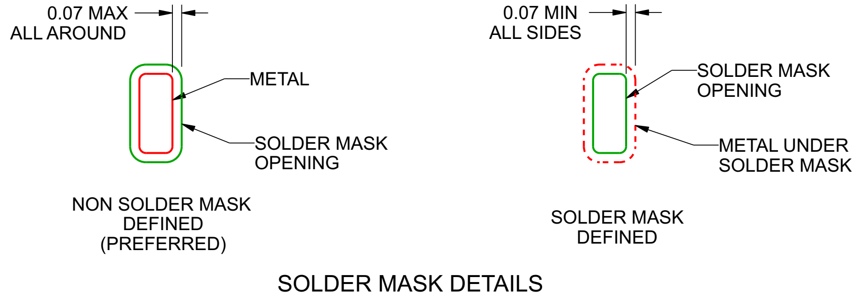
EXAMPLE BOARD LAYOUT

RTQ0056H **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

4222809/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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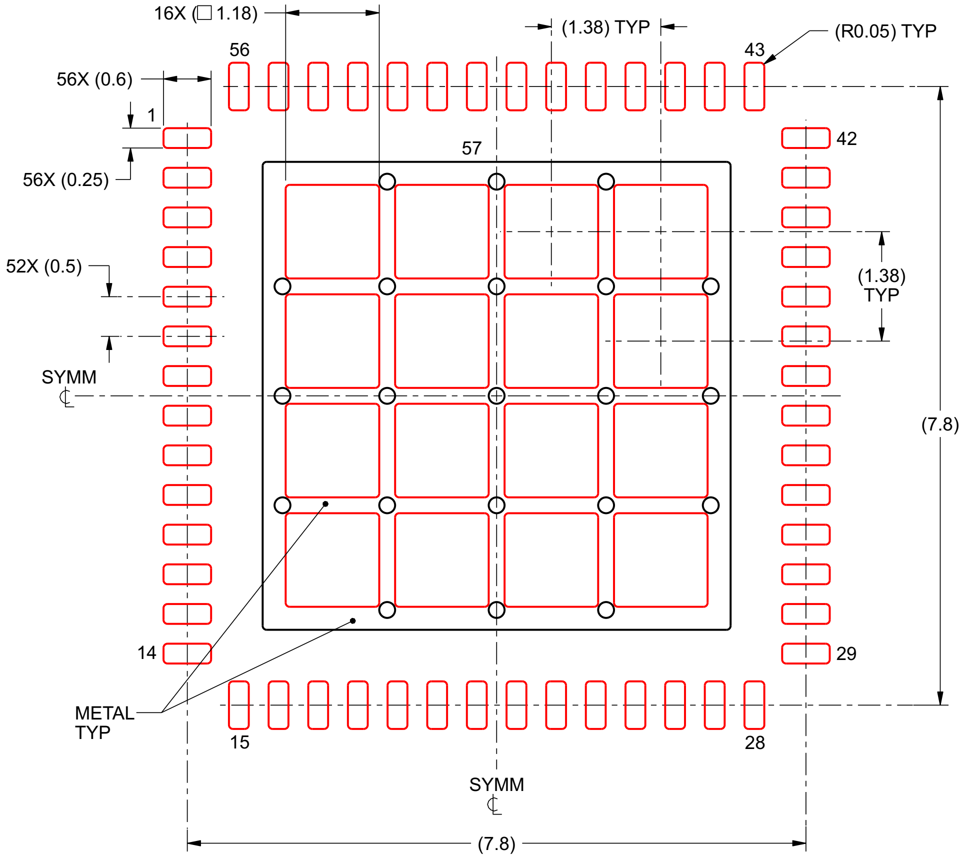
EXAMPLE STENCIL DESIGN

RTQ0056H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
64% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

4222809/A 03/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2388RTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS2388RTQ	Samples
TPS2388RTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2388RTQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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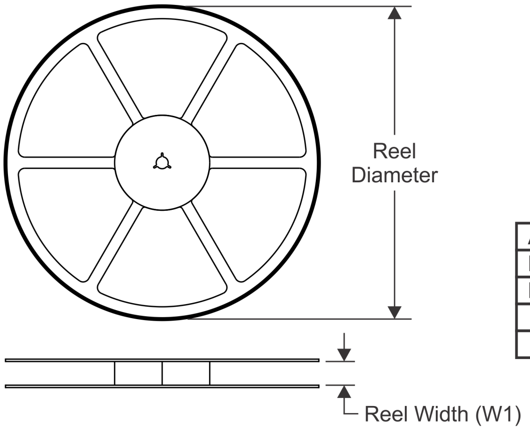
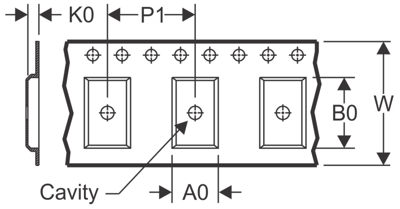
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

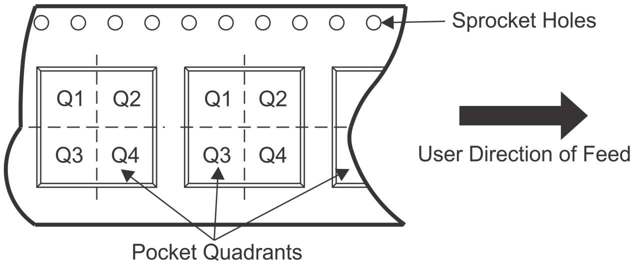


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

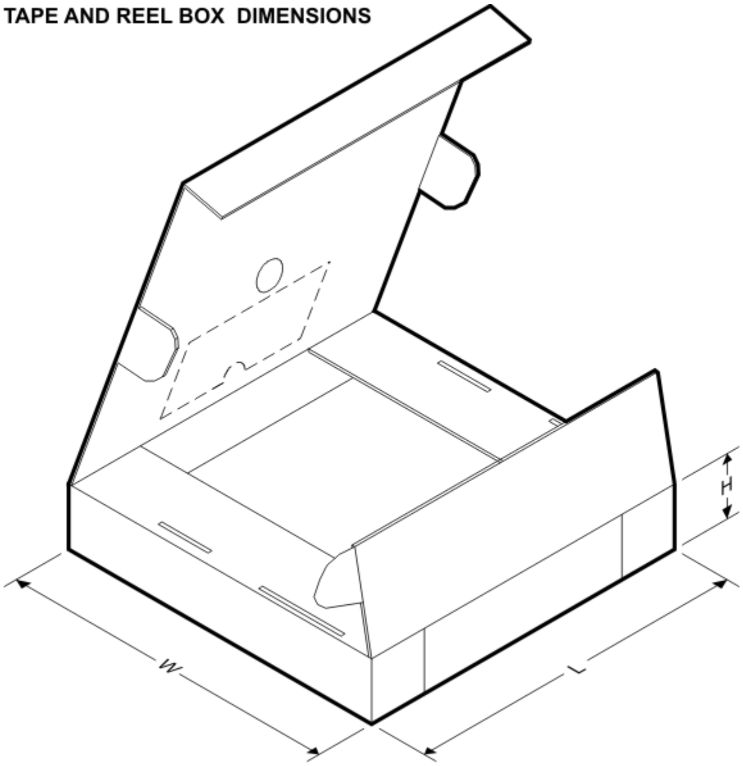
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2388RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS2388RTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2388RTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
TPS2388RTQT	QFN	RTQ	56	250	210.0	185.0	35.0

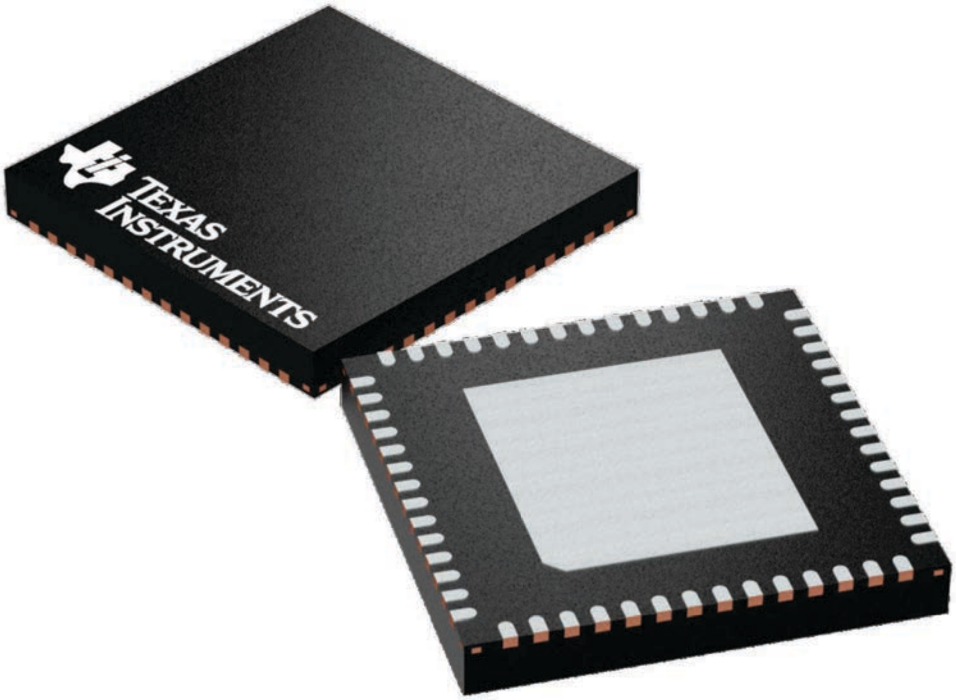
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

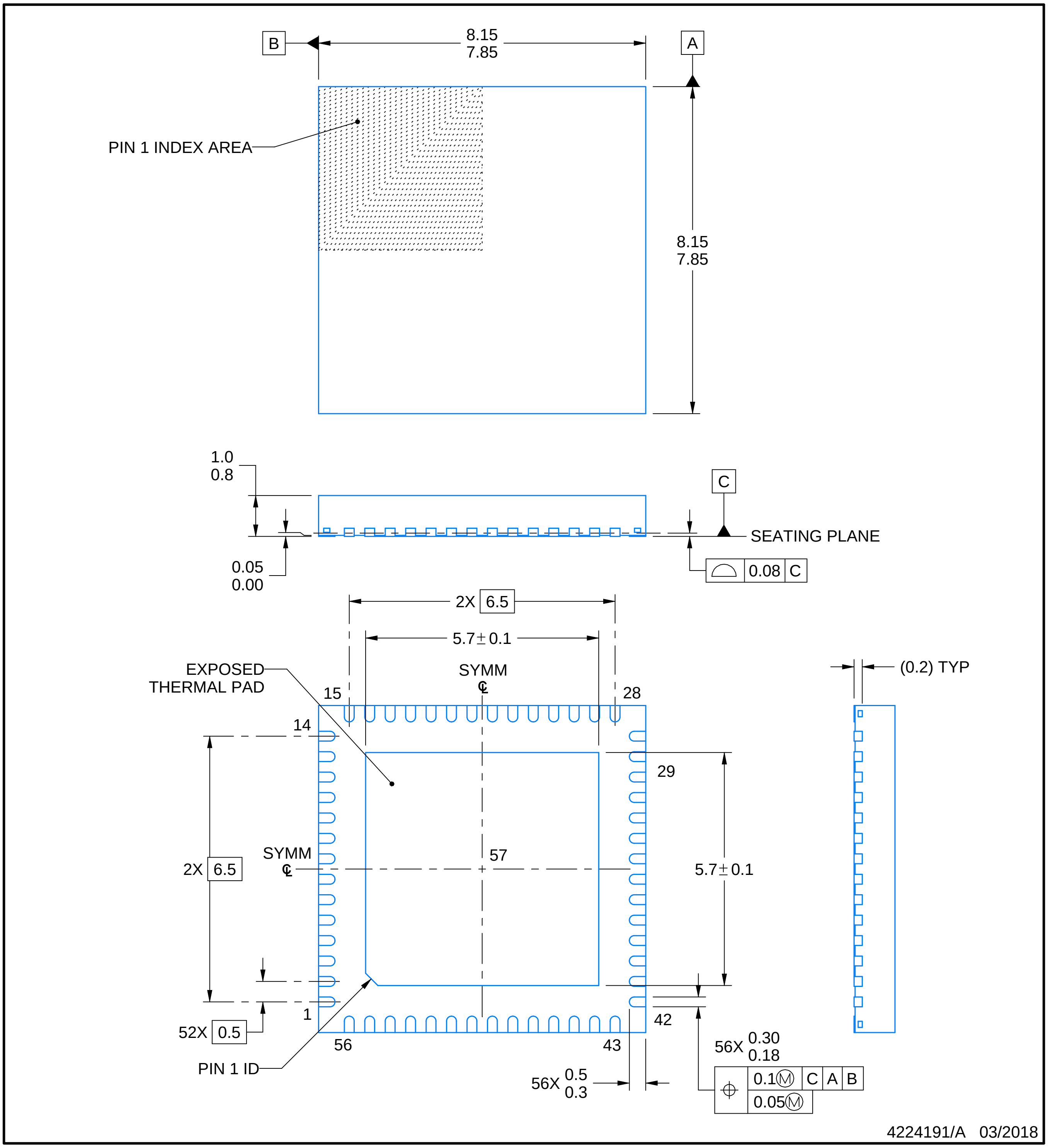
8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



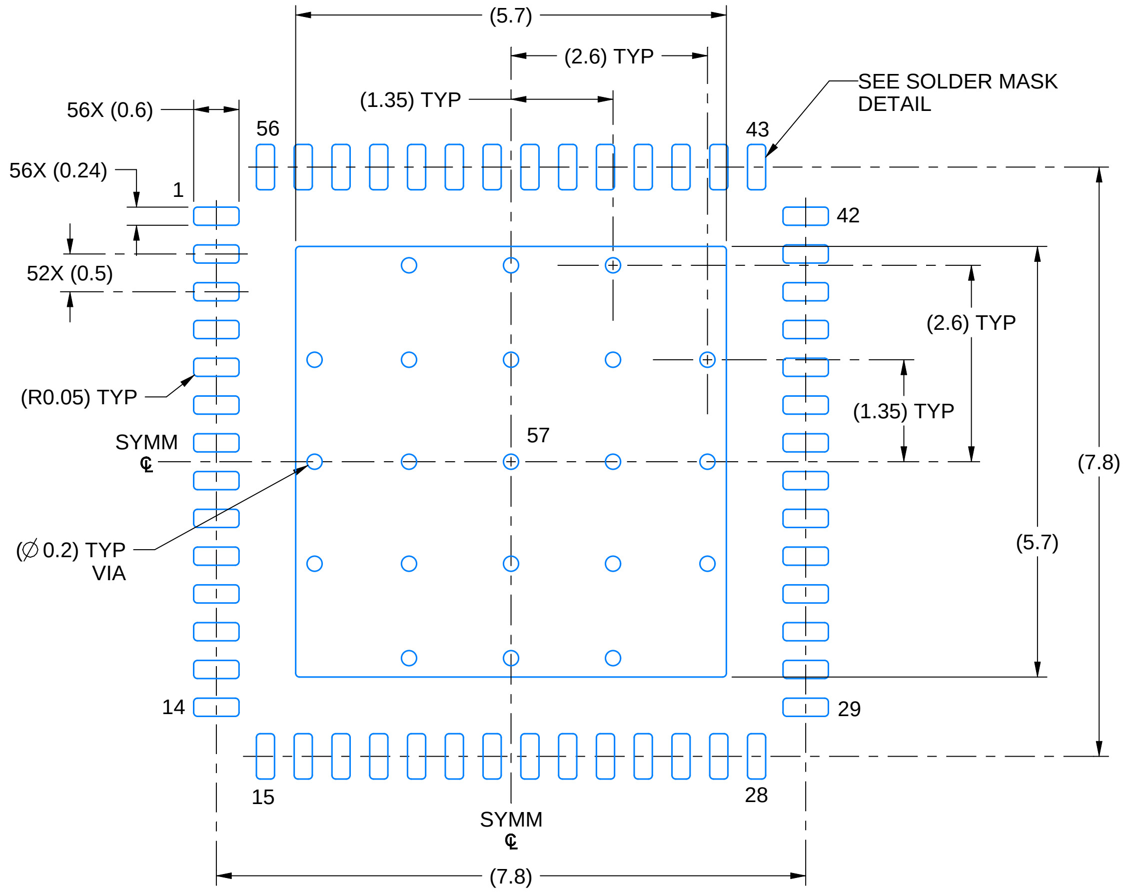
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224653/A

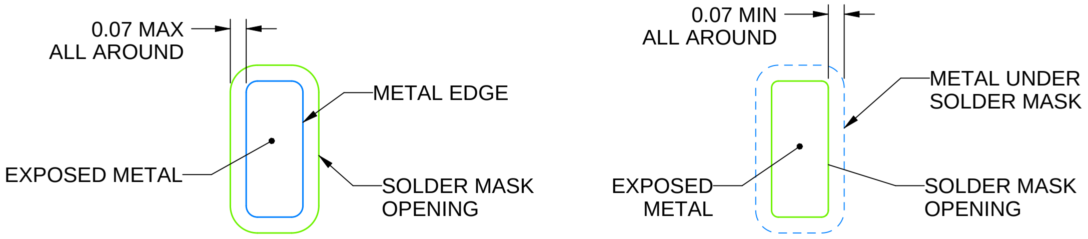


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK
DEFINED
(PREFERRED)

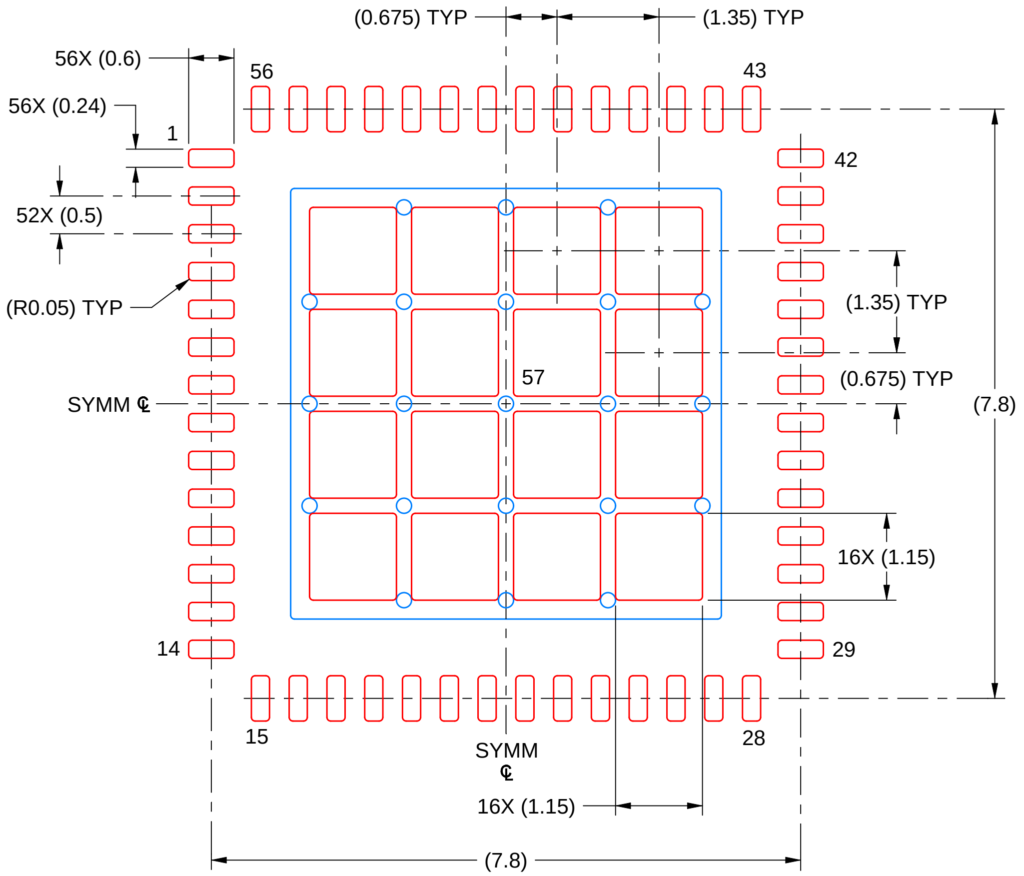
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224191/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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