TPS62684 1600mA，高效降压转换器 已针对最小解决方案尺寸进行优化

1 特性

- 从 3.25V 至 5.5V 的 VIN 范围
- 总体解决方案尺寸 < 12mm^2
- 需要三个表面贴装外部组件（一个 0805 片式多层陶瓷电容器 (MLCC) 电感器、两个小型陶瓷电容器）
- 完整的 1mm 以下组件外形解决方案
- 展频，脉宽调制 (PWM) 频率抖动
- *同类产品最佳的* 负载与线路瞬态
- 直流电压总精度为 ±2%
- 高达 1600mA 负载电流
- 5.5MHz 稳频运行
- 采用 6 引脚 NanoFree™ 晶圆级芯片封装 (WCSP)

2 应用范围

- 平板电脑
- 手机、智能电话
- 数字电视，无线网局域网 (WLAN)，全球定位系统 (GPS) 和 Bluetooth® 应用范围

3 说明

TPS62684 是一款已针对电池供电类便携式应用而进行优化的高频同步降压直流到直流转换器，在此类应用中，在极小的解决方案尺寸和高度内要求有高负载电流。 TPS62684 针对高效和低输出电压纹波进行优化，支持高达 1600mA 的负载电流，并且可使用低成本芯片电感器和电容器。 借助于 3.25V 至 5.5V 的输入电压范围，此器件支持由锂离子电池以及 5V 电源轨供电的应用。

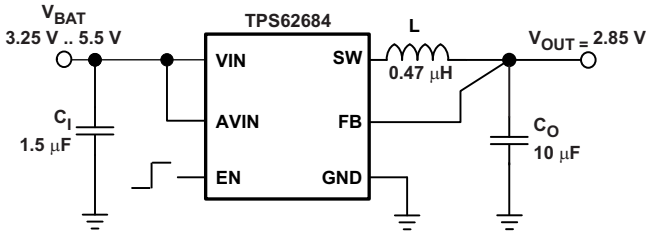
TPS62684 借助 PWM 展频功能以 5.5MHz 的频率运行。 对于噪声敏感应用，这一特性提供了一个低噪声经稳压输出，并且降低了输入上的噪声。 此器件支持 2.85V 固定输出电压，从而无需外部反馈网络。

这些特性与高电源抑制比 (PSRR) 和交流负载稳压性能组合在一起，使得该器件适合用来替代线性稳压器以获得更好的功率转换效率

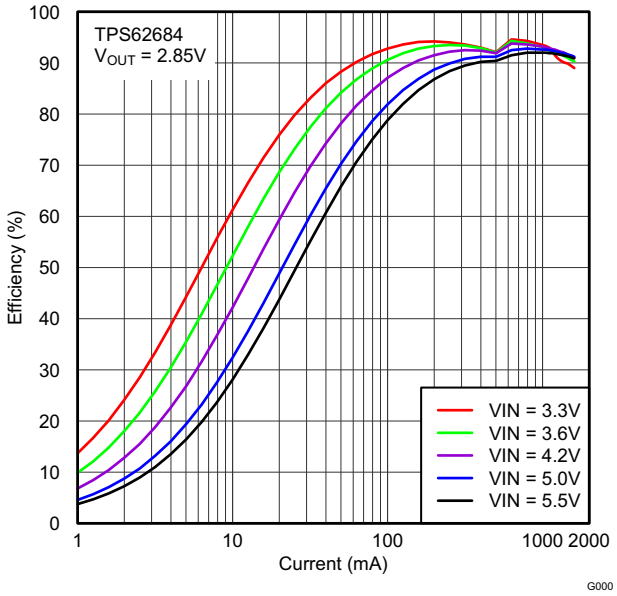
器件信息

订货编号	封装	封装尺寸
TPS62684YFF	芯片级球状引脚栅格阵列 (DSBGA) (6)	1.431mm x 1.135mm

最小解决方案尺寸应用



效率与负载电流间的关系



目录

4 修订历史记录

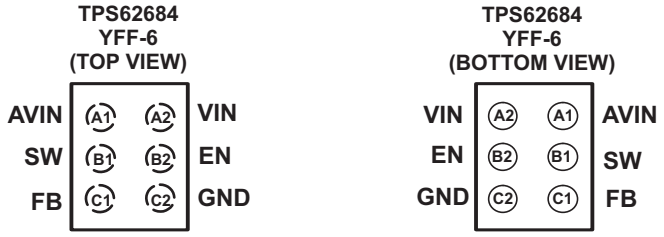
日期	修订版本	注释
2014 年 4 月	*	最初发布。

Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	DEVICE SPECIFIC FEATURE	PACKAGE MARKING CHIP CODE
TPS62684	2.85V	PWM Spread Spectrum Modulation Forced PWM Active Output Discharge	D1

5 Terminal Configuration and Functions

6-Terminal YFF



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
FB	C1	I	Output feedback sense input. Connect FB to the converter's output.
VIN	A2	I	Power supply input. Make sure the decoupling capacitor is connected as close as possible between terminal VIN (A2) and GND (C2).
AVIN	A1	I	Bias supply input voltage pin. This pin must be connected to VIN (A2).
SW	B1	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
EN	B2	I	This is the enable pin of the device. Connecting this pin low forces the device into shutdown mode. Pulling this pin high enables the device. This pin must not be left floating and must be terminated. When EN is pulled low, the output capacitor is actively discharged by internal circuitry.
GND	C2	-	Ground pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Voltage at VIN(2)	–0.3	6	V
	Voltage at FB(2)	–0.3	3.6	
	Voltage at SW, EN, AVIN (2)	–0.3	VIN + 0.3	
	Continuous average output current(3)		890	mA
	Peak output current(3)		1600	mA
T_J	Operating junction temperature(4)	-40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Limit the junction temperature to 105°C.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve full lifetime, it is recommended to operate the device with a maximum junction temperature of 105°C.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C
ESD rating (1)	Human body model		2	kV
	Charge device model		1	
	Machine model		100	V

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
VIN	Input voltage range		3.25		5.5	V
I_O	Peak output current (1)	VIN < $V_{OUT,nom}$ + 1V	0		960	mA
		$V_{OUT,nom}$ + 1V ≤ VIN ≤ 5.5V	0		1600	
C_I	Effective Input Capacitance (2) (3)		0.5			µF
L	Effective Inductance		0.3		1.2	µH
C_O	Effective Output Capacitance (2)		3.0	5.0	30	µF
T_A	Ambient temperature (4)		–40		+85	°C
T_J	Operating junction temperature (5)		–40		+125	°C

(1) Operating beyond the continuous average output current of 890mA may decrease the lifetime. See the Thermal, Lifetime Information and Maximum Output Current section.
(2) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. The capacitance is specified to allow the selection of the appropriate capacitor taking into account its dc bias effect.
(3) Larger values may be required if the source impedance can not support the transient requirements of the load.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$. To achieve full lifetime, it is recommended to operate the device with a maximum junction temperature of 105°C.
(5) Limit the junction temperature to 105°C at 1.6A output current for a lifetime of 25k hours.

6.4 Thermal Information

THERMAL METRIC (1)		TPS62684 YFF 6 TERMINALS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	
ψ_{JT}	Junction-to-top characterization parameter	4.1	
ψ_{JB}	Junction-to-board characterization parameter	17.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Minimum and maximum values are at V_I = 3.25V to 5.5V, EN = VIN and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at VIN = 3.6V, EN = VIN and T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT into VIN + AVIN						
I_Q	Operating quiescent current	I_O = 0mA		5.8		mA
I_{SD}	Shutdown current	EN = low; not including high side MOSFET leakage		0.2	1.5	µA
V_{UVLO}	Undervoltage lockout threshold	VIN rising		2.1	2.3	V
		VIN falling		1.95	2.1	V
ENABLE						
V_{IH}	High-level input voltage		0.9			V
V_{IL}	Low-level input voltage				0.4	V
$I_{lkg,EN}$	Input leakage current	EN connected to GND or VIN; T_J = –40°C to 85°C		0.01	0.1	µA
POWER SWITCH						
$R_{DS(on),HS}$	High Side MOSFET on resistance	VIN = 3.6V; T_J = –40°C to 125°C		95	155	mΩ
		VIN = 2.5V		170		mΩ
$I_{lkg,HS}$	High Side MOSFET leakage current	VIN = 5.5V; T_J = –40°C to 85°C			2.6	µA
$R_{DS(on),LS}$	Low Side MOSFET on resistance	VIN = 3.6V; T_J = –40°C to 125°C		75	155	mΩ
		VIN = 2.5V		100		mΩ
$I_{lkg,LS}$	Low Side MOSFET leakage current	VIN = 5.5V; T_J = –40°C to 85°C			1	µA
	Resistor in parallel to Low Side MOSFET			250		kΩ
R_{DIS}	Discharge resistor for power-down sequence	only active after a first power-up (EN = high to low after VIN applied)		12		Ω
	Average High Side MOSFET current limit		1680	2100	2850	mA
	Input current limit under short-circuit conditions	V_{OUT} shorted to ground		150		mA
	Thermal shutdown	Temperature rising		140		°C
	Thermal shutdown hysteresis	Temperature falling		10		°C
OSCILLATOR						
f_{SW}	Nominal oscillator frequency	I_{OUT} = 0mA		5.5		MHz
OUTPUT						
$V_{OUT,nom}$	Nominal output voltage			2.85		V
	Output voltage accuracy	3.25V ≤ VIN ≤ 3.85V, 0mA ≤ I_O ≤ 960 mA	$0.98\times V_{OUT,NOM}$	$V_{OUT,NOM}$	$1.02\times V_{OUT,NOM}$	V
		3.85V ≤ VIN ≤ 5.5V, 0mA ≤ I_O ≤ 1600 mA	$0.98\times V_{OUT,NOM}$	$V_{OUT,NOM}$	$1.02\times V_{OUT,NOM}$	V
	Line regulation	VIN = V_{OUT} + 0.5V (min 3.25V) to 5.5V, I_O = 200 mA		0.2		%/V
	Load regulation	I_O = 0mA to 1600 mA		–0.00085		%/mA
	FB pin input resistance			1.4		MΩ

6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
	Start-up delay time	I_O = 0mA, Time from EN = high to start switching		120	300	µs
t_{RAMP}	ramp time	I_O = 0mA, Time from start switching until 95% of nominal output voltage		150		µs
	Shutdown time	I_O = 0mA, Time from EN = low to V_O < 500mV, Effective Output Capacitance $C_{O\_effective}$ = 5µF		300		µs

6.7 Typical Characteristics

TABLE OF GRAPHS			FIGURE
η	Efficiency	vs Load current	Figure 1, Figure 2, Figure 3, Figure 4
		vs Input voltage	Figure 5
	Load transient response		Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14
	AC load transient response		Figure 15
	Line Transient Response		Figure 16
V_{OUT}	DC output voltage	vs Load current	Figure 6, Figure 7
f_{sw}	PWM switching frequency	vs Input voltage	Figure 17
	PWM switching frequency	vs Load Current	Figure 18
	PWM operation		Figure 19
	Spread spectrum frequency modulation operation		Figure 20
	Start-up		Figure 21, Figure 22
	Shutdown		Figure 23

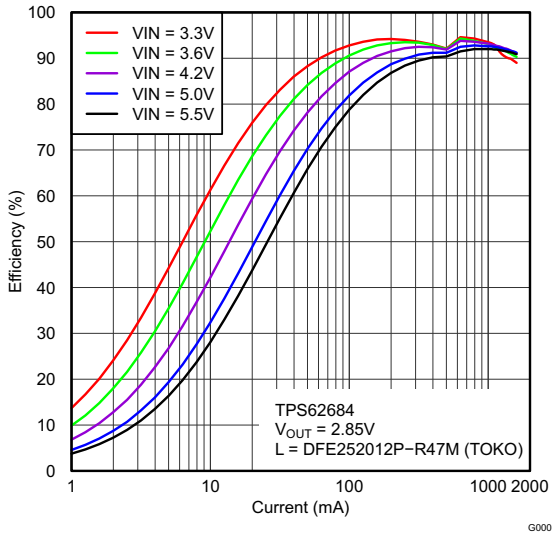


Figure 1. Efficiency Vs Load Current

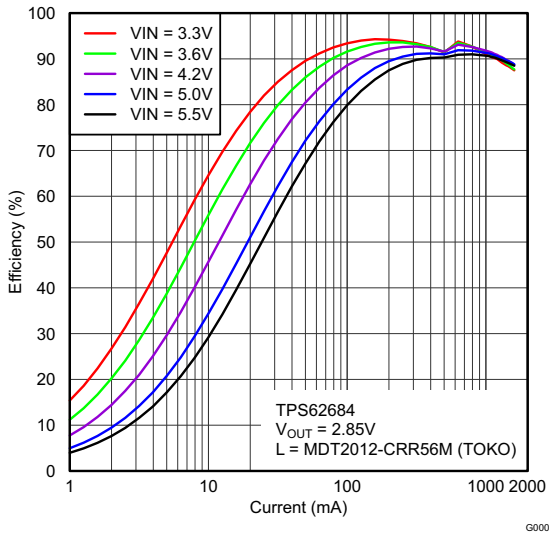


Figure 2. Efficiency Vs Load Current

Typical Characteristics (continued)

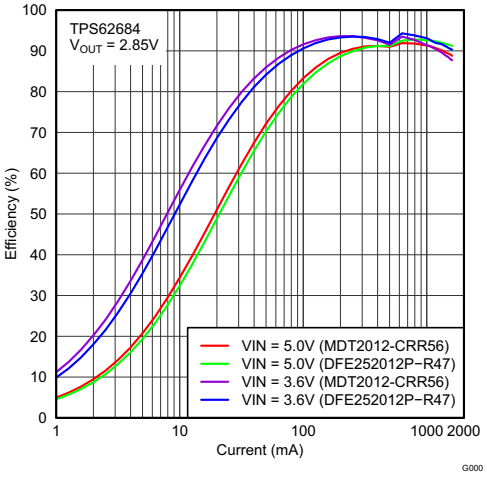


Figure 3. Efficiency Vs Load Current

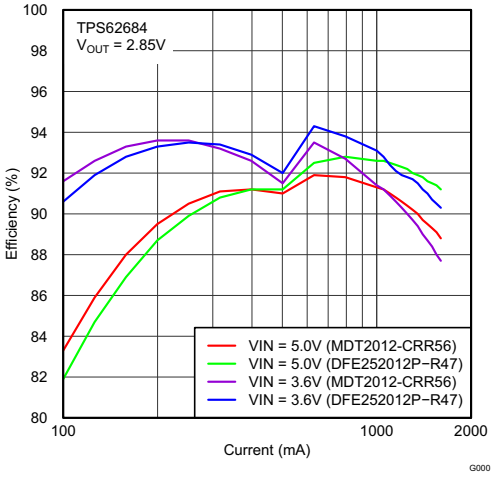


Figure 4. Efficiency Vs Load Current

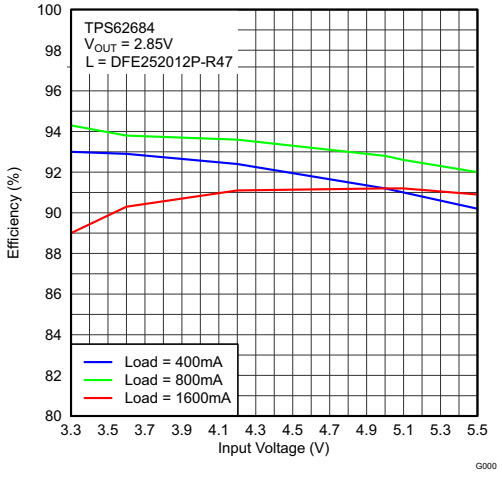


Figure 5. Efficiency Vs Input Voltage

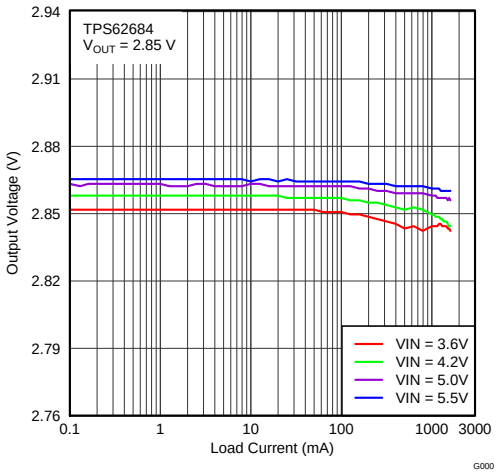


Figure 6. Output Voltage Vs Load Current

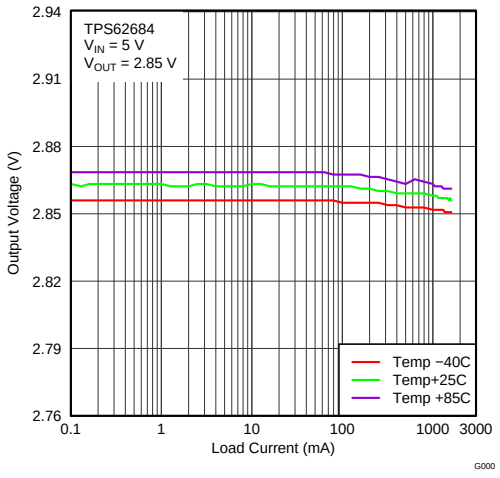


Figure 7. Output Voltage Vs Load Current

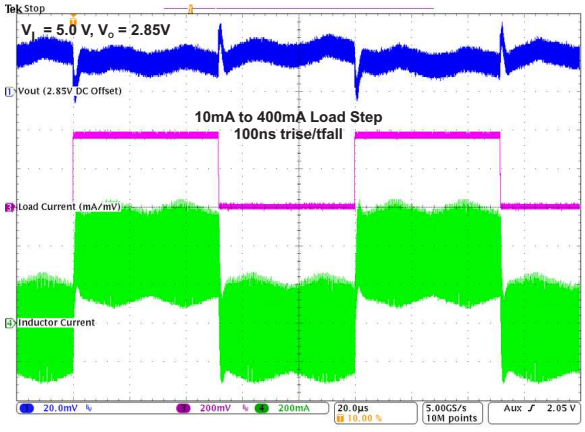


Figure 8. Load Transient Response

Typical Characteristics (continued)

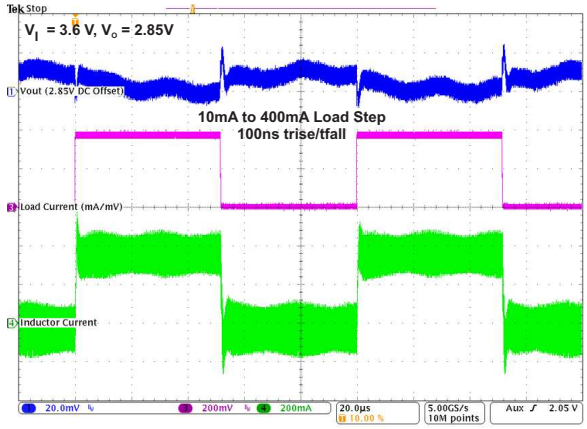


Figure 9. Load Transient Response

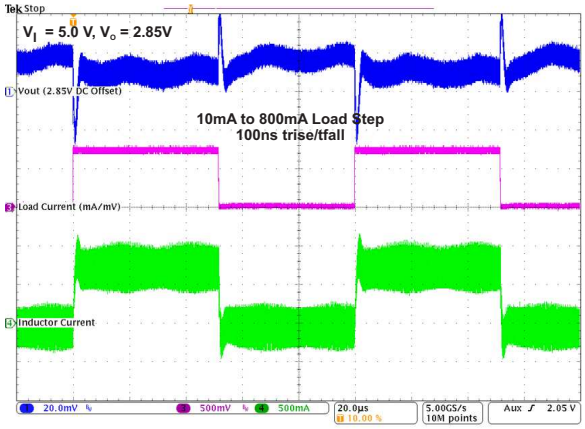


Figure 10. Load Transient Response

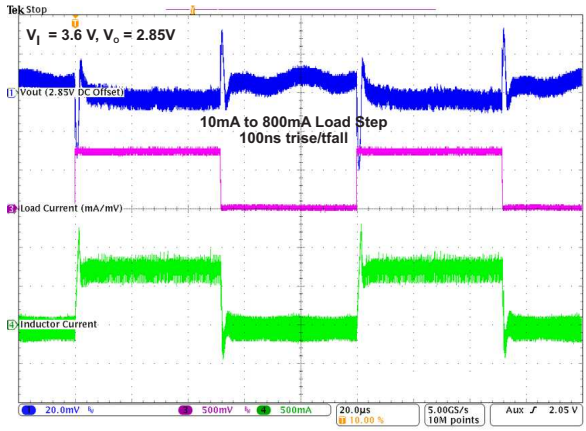


Figure 11. Load Transient Response

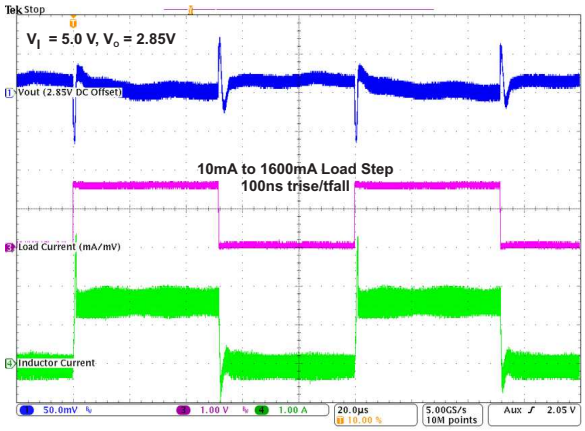


Figure 12. Load Transient Response

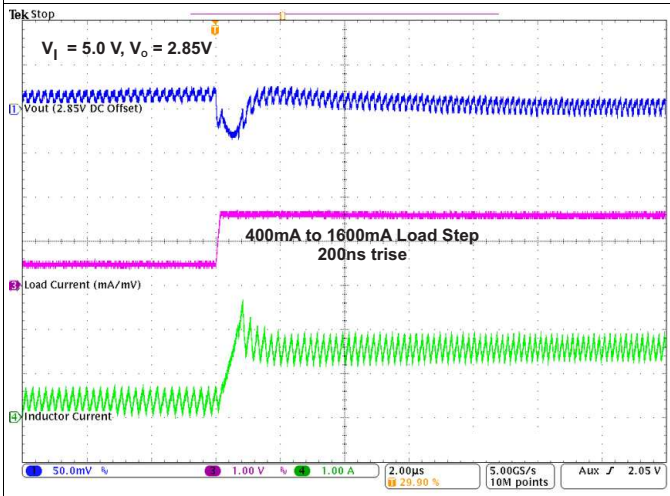


Figure 13. Load Transient Response

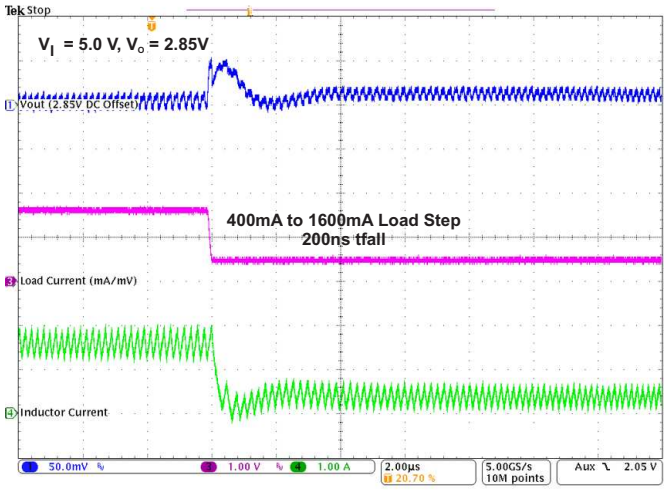


Figure 14. Load Transient Response

Typical Characteristics (continued)

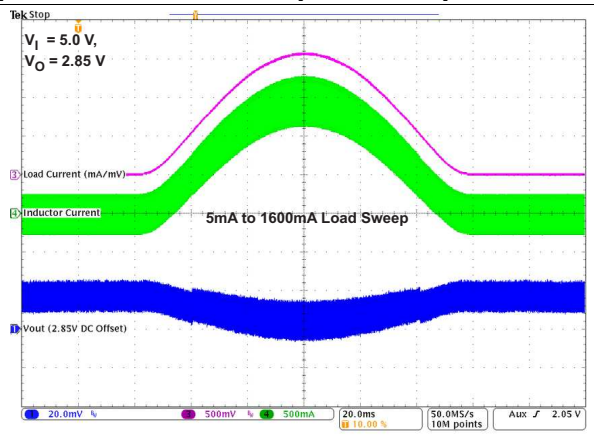


Figure 15. AC Load Transient Response

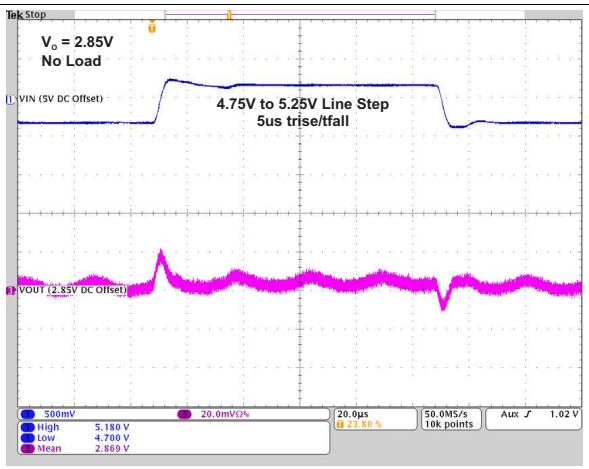


Figure 16. Line Transient Response

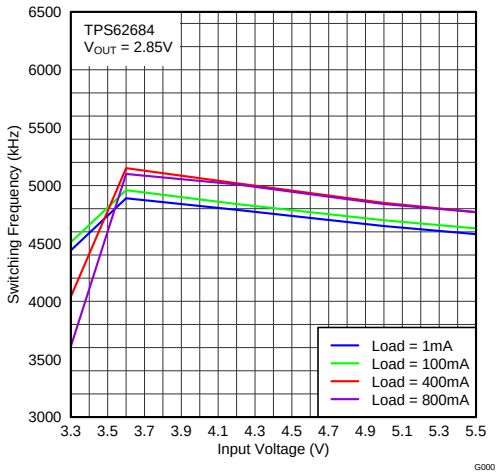


Figure 17. PWM Switching Frequency Vs Input Voltage

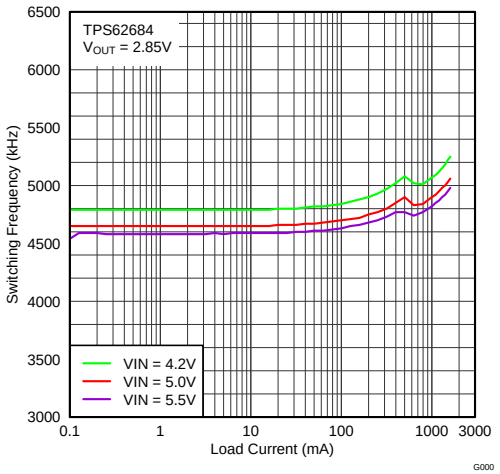


Figure 18. PWM Switching Frequency Vs Load Current

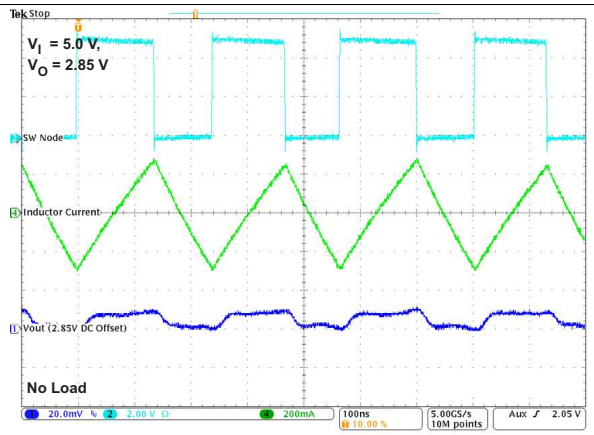


Figure 19. PWM Operation

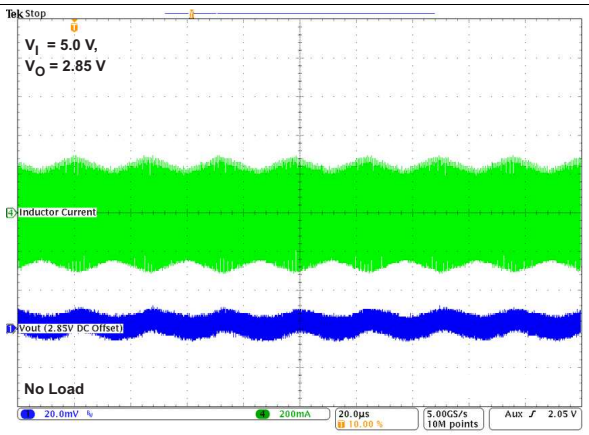


Figure 20. Spread Spectrum Frequency Modulation Operation

Typical Characteristics (continued)

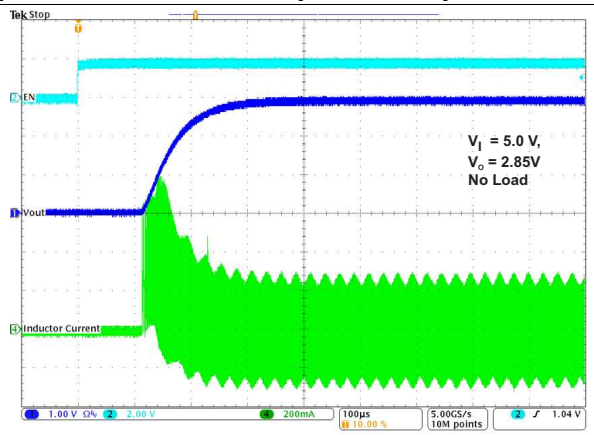


Figure 21. Start-Up

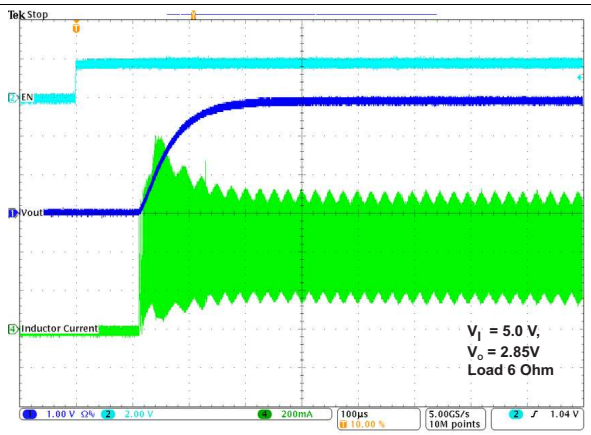


Figure 22. Start-Up

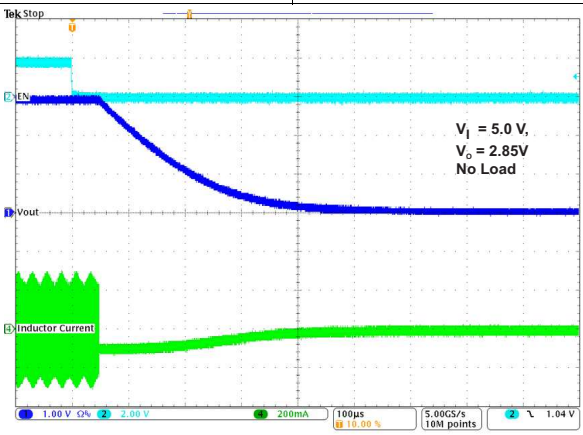
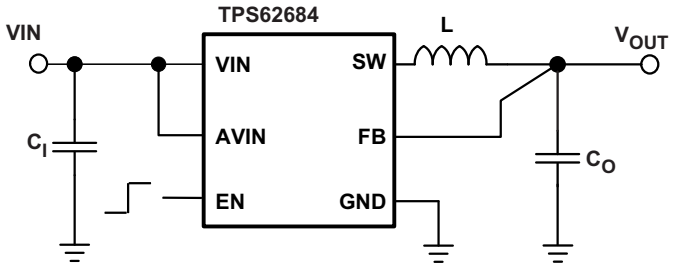


Figure 23. Shutdown

7 Parameter Measurement Information



List of components:

- L = TOKO MDT2012-CRR56M (if not otherwise noted)
- C_I = MURATA GRM155R60J155ME80D (1.5µF, 6.3V, 0402, X5R)
- C_O = MURATA GRM188R60J106ME84D (10µF, 6.3V, 0603, X5R)

8 Detailed Description

8.1 Overview

8.1.1 Operation

The TPS62684 is a synchronous step-down converter typically operating at a regulated 5.5-MHz pulse width modulation (PWM) frequency.

The converter uses a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response which allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the N-channel high side MOSFET switch is turned on and the inductor current ramps up. This raises the output voltage until the main comparator trips; then the control logic turns off the switch.

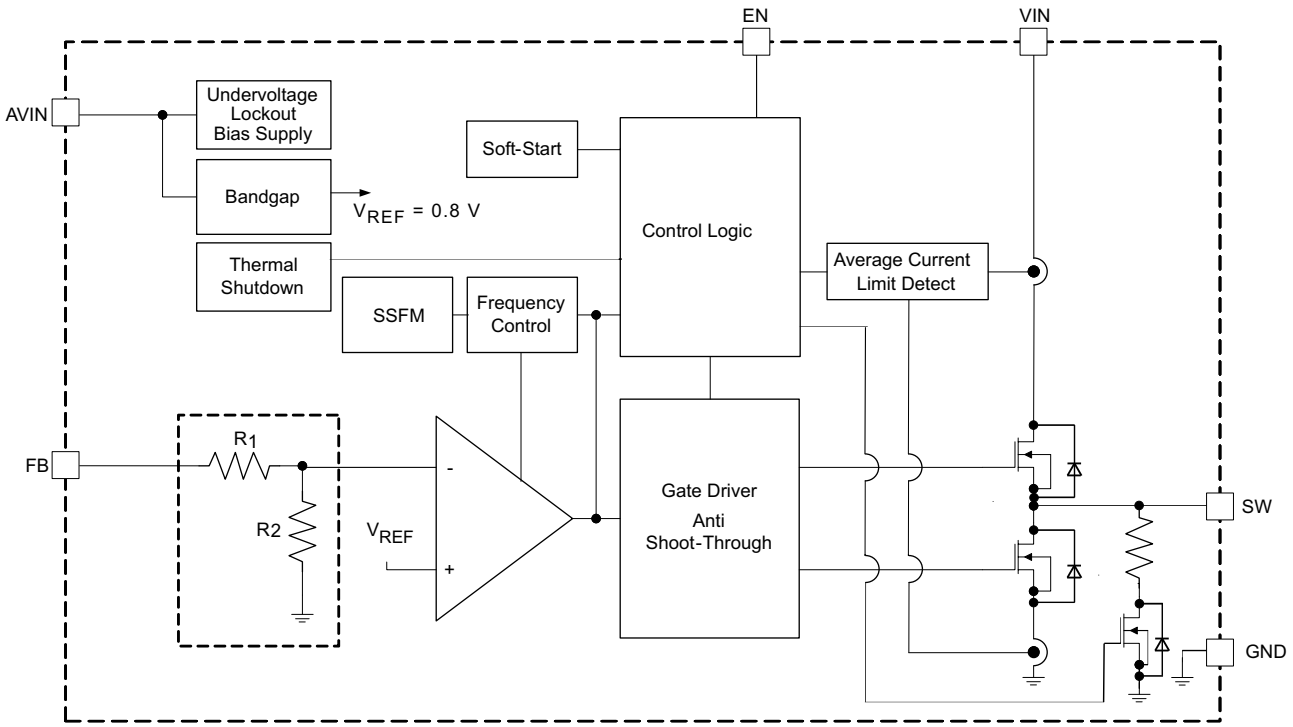
One key advantage of the non-linear architecture that there is no traditional feedback loop. The loop response time to a change in V_{OUT} is essentially instantaneous. The absence of a traditional, high-gain compensated linear loop means that the TPS62684 is inherently stable over a range of L and C_O.

8.1.2 Switching Frequency

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 5.5MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 5.5MHz nominal at extreme duty cycles, the application is assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent series inductance (ESL). This increases the *ESL step* seen at the FB pin input, decreasing the propagation delay which increases the switching frequency.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Spread Spectrum, PWM Frequency Dithering

The goal is to spread out the emitted RF energy over a larger frequency range, so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude, making it easier to comply with electromagnetic interference (EMI) standards and with power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to their output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The spread spectrum architecture varies the switching frequency by around ±10% of the nominal switching frequency, thereby significantly reducing the peak radiated and conducted noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

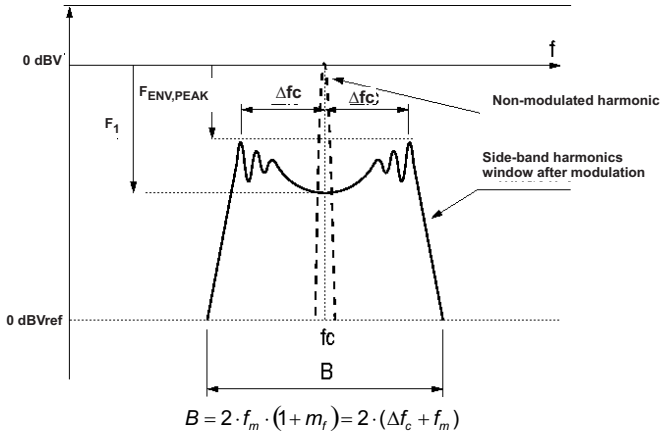


Figure 24. Spectrum Of A Frequency Modulated Sin. Wave With Sinusoidal Variation In Time

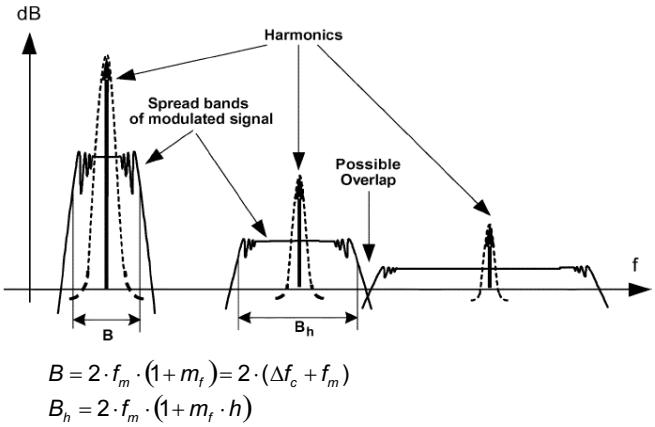


Figure 25. Spread Bands Of Harmonics In Modulated Square Signals (1)

The above figures show that after modulation the side-band harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (m_f), the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \tag{1}$$

where:

f_c is the carrier frequency (5.5MHz)

f_m is the modulating frequency (approx. 0.008*f_c)

δ is the modulation ratio (approx 0.1)

$$\delta = \frac{\Delta f_c}{f_c} \tag{2}$$

The maximum switching frequency f_c is limited by the device and finally the parameter modulation ratio (δ), together with f_m , which is the side-band harmonic´s bandwidth around the carrier frequency f_c . The bandwidth of a frequency modulated waveform is approximately given by Carson's rule and is summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \tag{3}$$

(1) Spectrum illustrations and formulae (Figure 24 and Figure 25) copyright IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO.3, AUGUST 2005. See References Section for full citation.

Feature Description (continued)

f_m < RBW (resolution bandwidth): The receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

8.4 Device Functional Modes

8.4.1 Enable

The TPS62684 device starts operation when EN is set high. For proper operation, the EN pin must be terminated and must not be left floating. The device should only be enabled when the input voltage is stable and has ramped above its minimum supply of 3.25V.

Pulling the EN pin low forces the device into shutdown, with a shutdown current of typically 0.2µA. In this mode, the internal high side and low side MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off. The TPS62684 device actively discharges the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 12Ω. This internal discharge transistor is only turned on after the device had been enabled at least once. The required time to discharge the output capacitor at the output node depends on load current and the effective output capacitance. The TPS62684 is designed such that it can start into a pre-biased output, in case the output discharge circuit was active for too short a time to fully discharge the output capacitor. In this case, the converter starts switching as soon as the internal reference has approximately reached the equivalent voltage to the output voltage present. It then ramps the output from that voltage level to its target value.

8.4.2 Soft Start

The TPS62684 has an internal soft start circuit that controls the ramp up of the output voltage. Once the converter is enabled and the input voltage is above the undervoltage lockout threshold V_{UVLO}, the output voltage ramps up to 95% of its nominal value within t_{Ramp} of typ. 150µs. This ensures a controlled ramp up of the output voltage and limits the input voltage drop when a battery or a high-impedance power source is connected to the input of the DC/DC converter.

The inrush current during start-up is directly related to the effective capacitance and load present at the output of the converter.

During soft start, the current limit is reduced to 2/3 of its nominal value. Once the internal reference voltage has reached 90% of its target value, the current limit is set to its nominal target value.

8.4.3 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on either MOSFET under undefined conditions. The TPS62684 has a rising UVLO threshold of 2.1V (typical).

8.4.4 Short-Circuit Protection

The TPS62684 integrates current limit circuitry to protect the device against heavy load or short circuits. When the average current in the high side MOSFET reaches its current limit, the high side MOSFET is turned off and the low side MOSFET is turned on ramping down the inductor current.

As soon as the converter detects a short circuit condition it shuts down. After a delay of approximately 20 µs, the converter restarts. In case the short circuit condition remains, the converter shuts down again after hitting the current limit threshold. In case the short circuit condition remains present on the converters output, the converter periodically re-starts with a small duty cycle as the output voltage is zero and shuts down again, thereby limiting the current drawn from the input.

Device Functional Modes (continued)

8.4.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the power stage is turned off. The device continues its operation when the junction temperature falls below typically 130°C.

9 Applications and Implementation

9.1 Application Information

9.1.1 Inductor Selection

The TPS62684 series of step-down converters have been optimized to operate with an effective inductance value in the range of 0.3µH to 1.2µH and with output capacitors in the range of 3µF up to 30µF effective capacitance. The internal compensation is optimized to operate with an output filter of $L_{nominal}$ = 0.47µH or 0.56µH and $C_{O\_effective}$ = 5µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *CHECKING LOOP STABILITY* section.

The inductor value affects its peak-to-peak ripple current, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher VIN or V_{OUT}.

$$\Delta I_L = \frac{V_{OUT}}{VIN} \times \frac{VIN - V_{OUT}}{L \times f_{SW}} \qquad I_{L(MAX)} = I_{O(\mathrm{MAX})} + \frac{\Delta I_L}{2}$$

with: f_{SW} = switching frequency (5.5 MHz typical)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current (4)

In high-frequency converter applications, the efficiency is primarily affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total inductor losses consist of both the losses in the DC resistance (DCR) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

For smallest solution size a 0805 size (2mm x 1.2mm) chip inductor can be used. Please note that the DC resistance of the inductor is directly related to its volume (LxWxH). Therefore designing for smallest solution size negatively impacts the overall efficiency at heavy load currents.

The following inductor series from different suppliers have been used with the TPS62684 converter.

Table 1. List Of Inductors(1)

MANUFACTURER	SERIES	DIMENSIONS (in mm)
TOKO	MDT2012-CRR56N	2.0 x 1.2 x 1.0 max. height
	DFE252012P-R47(2)	2.5 x 2.0 x 1.2 max. height
MURATA	LQM21PNR47MGO	2.0 x 1.2 x 1.0 max. height
	LQM2MPNR47MGH	2.0 x 1.6 x 1.0 max. height

(1) See Third-Party Products Disclaimer
(2) Planned to be available in mass production by Q2/2014. Contact manufacturer for details.

9.1.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS62684 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For best performance, the device should be operated with a minimum effective output capacitance of 5µF. A total effective output capacitance between 3µF and 30µF is required. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

The device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

9.1.3 Output Filter Design

The inductor and the output capacitor build the output filter. As recommended in the output capacitor and inductor sections, these components should be in the range:

- C_O = 3µF to 30µF (total effective capacitance)
- L = 0.3 µH to 1.2 µH (effective inductance)

For best transient performance, the internal control stage is optimized for a LC_O product of 0.5µH x 10µF (nominal values).

9.1.4 Input Capacitor Selection

Because the nature of the buck converter has a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 1.5-µF nominal capacitor (≥ 0.5µF effective capacitance) with a X5R or X7R dielectric is sufficient. If the application exhibits a noisy or erratic switching frequency, the remedy is likely found by increasing the value of the input capacitor.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing than occurs between the inductance of the power source leads and C_I.

9.1.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look, from a steady-state perspective, at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is typically caused by board layout and/or LC_O combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the high side MOSFET, the output capacitor supplies all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop usually has more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $R_{DS(on)}$) that are temperature dependent, the loop stability analysis should be done over the input voltage range, load current range, and temperature range.

9.2 Typical Application

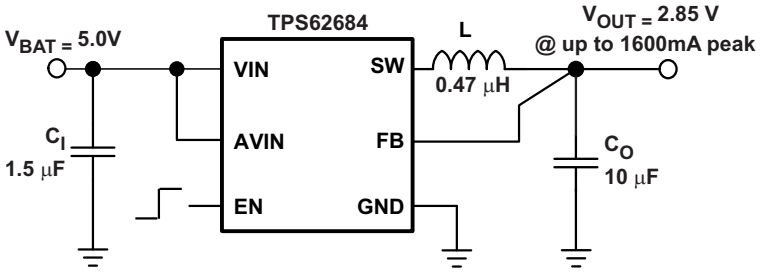


Figure 26. Typical Application Circuit

9.2.1 Design Requirements

Figure 26 shows the schematic of the typical application. The TPS62684 allows the design of a power supply with small solution size. In order to properly dissipate the heat, wide copper traces for the power connections should be used to distribute the heat across the PCB. If possible, a GND plane should be used as it provides a low impedance connection as well as serves as a heat sink. The EN pin should be set high after the supply voltage has ramped to at least the minimum input voltage level of 3.25V.

9.2.2 Detailed Design Procedure

The TPS62684 allows the design of a complete power supply with only 3 small external components. A X5R or X7R ceramic input capacitor close to the VIN pin and GND pin with a nominal value of 1.5uF or higher is required. The input capacitance can be increased in case the source impedance is large or if there are high load transients expected at the output. The inductor should be placed close to the SW node with a saturation current above the current limit. A X5R or X7R ceramic output capacitor should be placed close to the inductor terminal and GND. A low impedance GND connection on the output capacitor is required. The feedback (FB) pin should be routed to the terminal of the output capacitor. The dc bias effect of the input and output capacitors must be taken into account and the total capacitance on the output must not exceed the value given in the recommended operating conditions.

9.2.3 Application Curves

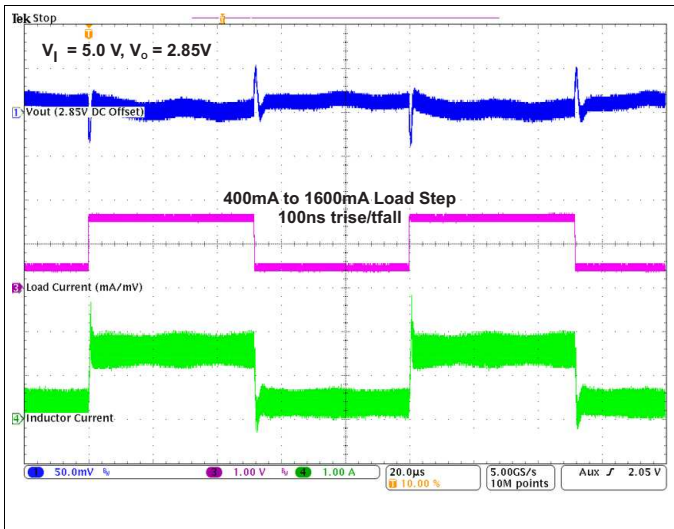


Figure 27. Load Transient Response

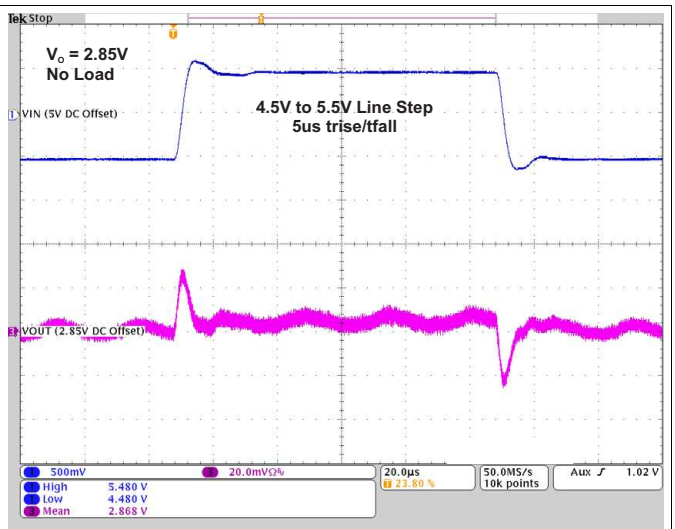


Figure 28. Line Transient Response

10 Power Supply Recommendations

The input voltage range is from 3.25V to 5.5V. The input power supply and the input capacitor(s) should be located as close to the device as possible to minimize the impedance of the power-supply line.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS62684 demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability and switching frequency issues as well as EMI problems. It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor as well as the inductor and output capacitor should be placed as close as possible to the IC pins. The feedback line should be routed away from noisy components and traces (e.g. SW line).

Figure 29 shows the recommended layout using a 0805 (2.0 mm x 1.2 mm) chip inductor, a 0402 input capacitor and a 0603 output capacitor. Total solution size is 12mm².

11.2 Layout Example

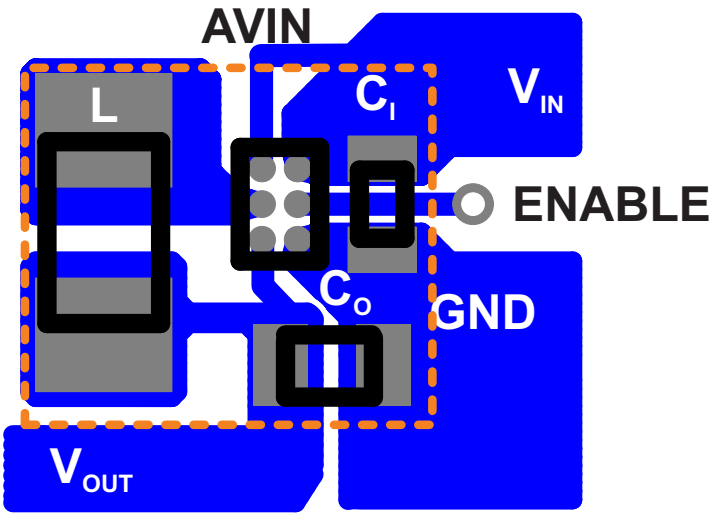


Figure 29. Suggested Layout (Top)

11.3 Thermal, Lifetime Information and Maximum Output Current

Implementation of integrated circuits in wafer chipscale packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

The maximum recommended junction temperature (T_J) of the TPS62684 for full 100k hour lifetime is 105°C. The thermal resistance of the 6-pin WCSP package (YFF-6) is $R_{\theta JA}$ = 108.9°C/W. Regulator operation is specified to a maximum steady-state ambient temperature T_A of 85°C. Therefore, the maximum power dissipation at T_J=105°C is about 180 mW and at T_J=125°C is about 367mW.

Thermal, Lifetime Information and Maximum Output Current (continued)

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{105℃ - 85℃}{109℃/W} = 180mW \quad (5)$$

Proper PCB layout with a focus on thermal performance results in a reduced junction-to-ambient thermal resistance $R_{\theta JA}$ and thereby reduces the device junction temperature, T_J.

The maximum peak output current of 1600mA for TPS62684 is defined by its internal current limit. The maximum dc output current over lifetime (100k hours at T_J= 105°C) is 890mA. The device can supply peak output currents above 890mA, so long as there are corresponding output currents below 890mA such that the average output current remains below 890mA, while keeping the junction temperature below 105°C. Operating at output currents above 890mA at junction temperatures above 105°C reduces the lifetime by electromigration effects.

For output currents above 960mA, a minimum supply voltage of 3.85V is recommended.

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.1.2 参考书目

“使用频率调制技术的开关电源转换器中的电磁干扰 (EMI) 减少”，*《电气与电子工程师协会 (IEEE) 电磁兼容性汇刊》，卷4，NO.3，2005 年 8 月，第 569-576 页* 作者 Josep Balcells，Alfonso Santolaria，Antonio Orlandi，David González，Javier Gago。

12.2 Trademarks

NanoFree is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62684YFFR	ACTIVE	DSBGA	YFF	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D1	Samples
TPS62684YFFT	ACTIVE	DSBGA	YFF	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

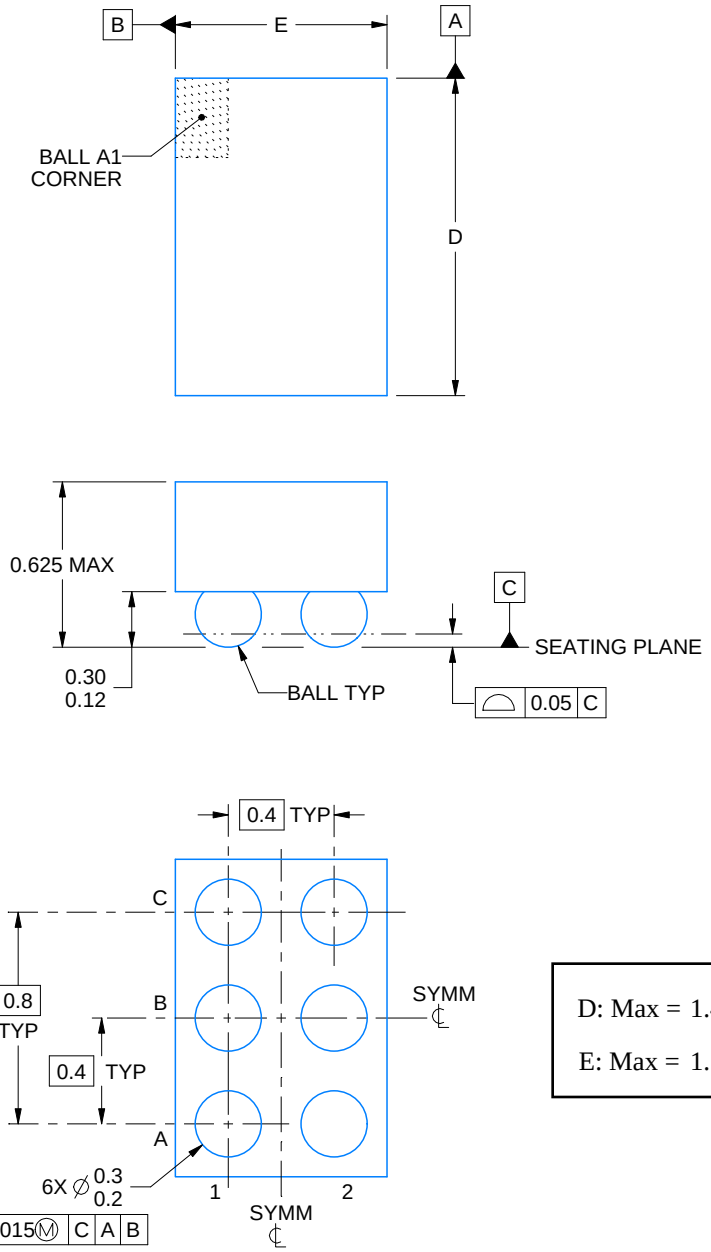
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.434 mm, Min =1.374 mm

E: Max = 1.138 mm, Min =1.078 mm

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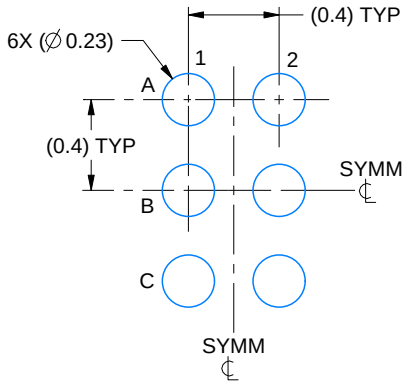
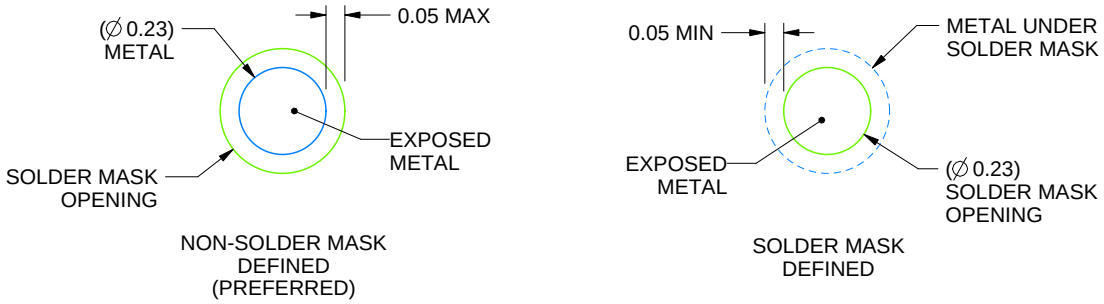
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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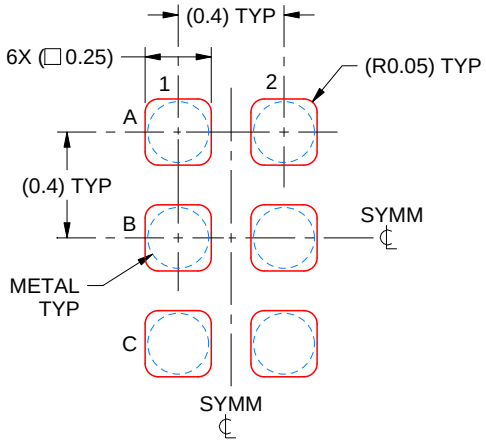
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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