

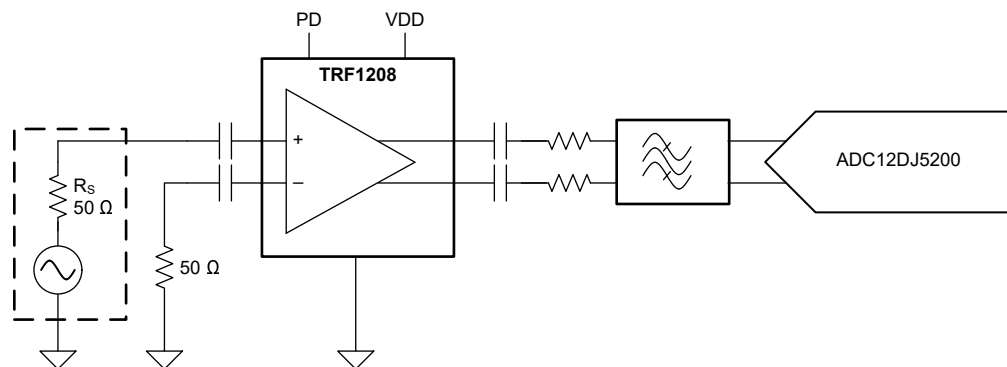
TRF1208 10MHz 至 11GHz、3dB BW ADC 驱动器放大器

1 特性

- 具有驱动射频 ADC 的卓越性能
 - 单端转差分
 - 差分转差分
- 两种固定增益变体：
 - 16dB (TRF1208)
 - 10dB (TRF1208B)
- 带宽：
 - TRF1208：8GHz (1dB)、11GHz (3dB)
 - TRF1208B：8.8GHz (1dB)、10.5GHz (3dB)
- OIP3：
 - TRF1208：37dBm (2GHz)、32dBm (6GHz)
 - TRF1208B：36dBm (2GHz)、28dBm (6GHz)
- P1dB：
 - TRF1208：15dBm (2GHz)、12.5dBm (6GHz)
 - TRF1208B：14dBm (2GHz)、11dBm (6GHz)
- 噪声系数：
 - TRF1208：7dB (2GHz)、7dB (8GHz)
 - TRF1208B：9.4dB (2GHz)、10.2dB (8GHz)
- 输出噪声频谱密度 (NSD)，dBm/Hz：
 - TRF1208：-151 (2GHz)、-151 (8GHz)
 - TRF1208B：-154.6 (2GHz)、-153.8 (8GHz)
- 增益和相位不平衡： $\pm 0.3\text{dB}$ 和 $\pm 3^\circ$
- 关断特性
- 3.3V 单电源运行
- 运行电流：138mA

2 应用

- 射频采样或 GPS ADC 驱动器



驱动高速 ADC 的 TRF1208

- 航天和国防
- 雷达导引头前端
- 相控阵雷达
- 军用无线电
- 测试和测量
- 高速数字转换器
- 矢量信号收发器 (VST)
- 4G/5G 无线 BTS
- 射频有源平衡-非平衡变压器

3 说明

TRF1208 是一款超高性能射频放大器，专门针对射频 (RF) 应用进行了优化。在驱动高性能 [ADC12DJ5200RF](#) 等模数转换器 (ADC) 时，交流耦合应用需要进行单端至差分转换，此款器件是这类应用的绝佳之选。片上匹配元件可对印刷电路板 (PCB) 实现方案进行简化，并在可用带宽内提供最高性能。此器件采用德州仪器 (TI) 先进的互补 BiCMOS 工艺制造，并采用节省空间的 WQFN-FCRLF 封装。

TRF1208 由单轨电源供电，消耗约 138mA 的运行电流。断电功能还有助于实现节能。

器件信息⁽¹⁾

器件型号	增益	封装	封装尺寸 ⁽²⁾
TRF1208	16dB	RPV (WQFN-FCRLF, 12)	2mm × 2mm
TRF1208B	10dB		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



Table of Contents

1 特性	1	7.3 Feature Description.....	24
2 应用	1	7.4 Device Functional Modes.....	24
3 说明	1	8 Application and Implementation	25
4 Revision History	2	8.1 Application Information.....	25
5 Pin Configuration and Functions	3	8.2 Typical Applications.....	28
6 Specifications	4	8.3 Power Supply Recommendations.....	32
6.1 Absolute Maximum Ratings.....	4	8.4 Layout.....	32
6.2 ESD Ratings.....	4	9 Device and Documentation Support	34
6.3 Recommended Operating Conditions.....	4	9.1 Device Support.....	34
6.4 Thermal Information.....	4	9.2 Documentation Support	34
6.5 Electrical Characteristics: TRF1208.....	5	9.3 接收文档更新通知.....	34
6.6 Electrical Characteristics: TRF1208B.....	7	9.4 支持资源.....	34
6.7 Typical Characteristics: TRF1208.....	9	9.5 Trademarks.....	34
6.8 Typical Characteristics: TRF1208B.....	16	9.6 静电放电警告.....	34
7 Detailed Description	23	9.7 术语表.....	34
7.1 Overview.....	23	10 Mechanical, Packaging, and Orderable Information	34
7.2 Functional Block Diagram.....	23		

4 Revision History

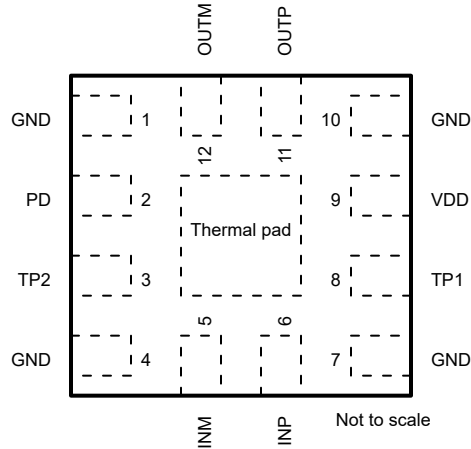
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2022) to Revision C (August 2023)	Page
• 添加了 TRF1208B 器件变体和相关内容.....	1

Changes from Revision A (March 2022) to Revision B (April 2022)	Page
• Changed <i>Pin 12</i> from: <i>OUTP</i> to: <i>OUTM</i> and <i>Pin 11</i> from: <i>OUTM</i> to <i>OUTP</i>	3
• Updated the <i>Interfacing with AFE7950 RX</i> and <i>Interfacing with AFE7950 TX</i> figures.....	25
• Updated the <i>TRF1208 in Receive Chain with AFE7950</i> figure.....	28
• Updated the <i>TRF1208 in Transmit Chain with AFE7950</i> figure.....	30

Changes from Revision * (October 2021) to Revision A (March 2022)	Page
• 将文档的状态从 <i>预告信息</i> 更改为 “ <i>量产数据</i> ”	1

5 Pin Configuration and Functions



**图 5-1. RPV Package,
12-Pin WQFN-FCRLF
(Top View)**

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
GND	1, 4, 7, 10	GND	Ground
INM	5	I	Differential signal input, negative
INP	6	I	Differential signal input, positive
OUTM	12	O	Differential signal output, negative
OUTP	11	O	Differential signal output, positive
PD	2	I	Power-down signal. Supports 1.8-V and 3.3-V Logic. 0 = Chip enabled 1 = Power down
TP1	8	—	Test pin. Short to ground.
TP2	3	—	Test pin. Short to ground.
VDD	9	P	3.3-V supply
Thermal pad	Pad	—	Thermal pad. Connect to ground on board.

(1) I = input, O = output, P = power, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage	- 0.3	3.7	V
INP, INM	Input pin power		20	dBm
V _{PD}	Power-down pin voltage	- 0.3	3.7	V
T _J	Junction temperature	- 40	150	°C
T _{stg}	Storage temperature	- 40	150	°C
Continuous power dissipation		See thermal information		

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±1000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	3.2	3.3	3.45	V
T _A	Ambient air temperature	- 40	25	105	°C
T _J	Junction temperature	- 40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TRF1208x	UNIT
		RPV (WQFN)	
		12 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	66.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	64.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	17.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	17.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	9.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics: TRF1208

at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $50\text{-}\Omega$ single-ended input, and $100\text{-}\Omega$ differential output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal 3-dB bandwidth	$V_O = 0.1 V_{PP}$		11		GHz
LSBW	Large-signal 3-dB bandwidth	$V_O = 1 V_{PP}$		11		GHz
1-dB BW	Bandwidth for 1-dB flatness			8		GHz
S21	Power gain	$f = 2\text{ GHz}$		16		dB
S11	Input return loss	$f = 10\text{ MHz to }8\text{ GHz}$		-10		dB
S12	Reverse isolation	$f = 2\text{ GHz}$		-35		dB
Imb _{GAIN}	Gain imbalance	$f = 10\text{ MHz to }8\text{ GHz}$		± 0.3		dB
Imb _{PHASE}	Phase imbalance	$f = 10\text{ MHz to }8\text{ GHz}$		± 3		°
CMRR	Common-mode rejection ratio ⁽¹⁾	$f = 2\text{ GHz}$		-45		dB
HD2	Second-order harmonic distortion	$f = 0.5\text{ GHz}, P_O = +3\text{ dBm}$		-70		dBc
		$f = 2\text{ GHz}, P_O = +3\text{ dBm}$		-65		
		$f = 6\text{ GHz}, P_O = +3\text{ dBm}$		-52		
		$f = 8\text{ GHz}, P_O = +3\text{ dBm}$		-45		
HD3	Third-order harmonic distortion	$f = 0.5\text{ GHz}, P_O = +3\text{ dBm}$		-68		dBc
		$f = 2\text{ GHz}, P_O = +3\text{ dBm}$		-63		
		$f = 6\text{ GHz}, P_O = +3\text{ dBm}$		-56		
		$f = 8\text{ GHz}, P_O = +3\text{ dBm}$		-63		
IMD2	Second-order intermodulation distortion	$f = 0.5\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-73		dBc
		$f = 2\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-69		
		$f = 6\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-56		
		$f = 8\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-45		
IMD3	Third-order intermodulation distortion	$f = 0.5\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-75		dBc
		$f = 2\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-84		
		$f = 6\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-72		
		$f = 8\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-51		
OP1dB	Output 1-dB compression point	$f = 0.5\text{ GHz}$		11		dBm
		$f = 2\text{ GHz}$		15		
		$f = 6\text{ GHz}$		12.5		
		$f = 8\text{ GHz}$		7.5		
OIP2	Output second-order intercept point	$f = 0.5\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		68		dBm
		$f = 2\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		63		
		$f = 6\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		55		
		$f = 8\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		42		

6.5 Electrical Characteristics: TRF1208 (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $50\text{-}\Omega$ single-ended input, and $100\text{-}\Omega$ differential output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OIP3	Output third-order intercept point	f = 0.5 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		34		dBm
		f = 2 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		37		
		f = 4 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		34		
		f = 6 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		30		
		f = 8 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		21		
NF	Noise figure	f = 0.5 GHz		6.5		dB
		f = 2 GHz		6.8		
		f = 6 GHz		7.2		
		f = 8 GHz		7		
IMPEDANCE						
$Z_{O\text{-DIFF}}$	Differential output impedance	f = dc (internal to the device)		3		Ω
Z_{IN}	Single-ended input impedance	INM pin terminated with $50\ \Omega$		50		Ω
TRANSIENT						
V_{OMAX}	Maximum output voltage (differential)			2		V_{PP}
V_{OSAT}	Saturated output voltage level (differential)	f = 2 GHz		3.9		V_{PP}
t_{REC}	Overdrive recovery time	Using a $-0.5\text{-}V_P$ input pulse of 2-ns duration		0.2		ns
POWER SUPPLY						
I_{QA}	Active current	Current on VDD pin, PD = 0		138		mA
I_{QPD}	Power-down quiescent current	Current on VDD pin, PD = 1		7		mA
ENABLE						
V_{PDHIGH}	PD pin logic high		1.45			V
V_{PDLLOW}	PD pin logic low				0.8	V
I_{PDBIAS}	PD bias current (current on PD pin)	PD = high (1.8-V logic)		50	100	μA
		PD = high (3.3-V logic)		200	250	
C_{PD}	PD pin capacitance			2		pF
t_{ON}	Turn-on time	50% V_{PD} to 90% RF		200		ns
t_{OFF}	Turn-off time	50% V_{PD} to 10% RF		50		ns

(1) Calculated using the formula $(S_{21}\text{-}S_{31})/(S_{21}\text{+}S_{31})$. Port-1: INP, Port-2: OUTP, Port-3: OUTM.

6.6 Electrical Characteristics: TRF1208B

at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $50\text{-}\Omega$ single-ended input, and $100\text{-}\Omega$ differential output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal 3-dB bandwidth	$V_O = 0.1 V_{PP}$		10.5		GHz
LSBW	Large-signal 3-dB bandwidth	$V_O = 1 V_{PP}$		10.5		GHz
1-dB BW	Bandwidth for 1-dB flatness			8.8		GHz
S21	Power gain	$f = 2\text{ GHz}$		10.5		dB
S11	Input return loss	$f = 10\text{ MHz to }8\text{ GHz}$		-10		dB
S12	Reverse isolation	$f = 2\text{ GHz}$		-32		dB
	Gain imbalance	$f = 10\text{ MHz to }8\text{ GHz}$		± 0.3		dB
	Phase imbalance	$f = 10\text{ MHz to }8\text{ GHz}$		± 3		$^\circ$
CMRR	Common-mode rejection ratio ⁽¹⁾	$f = 2\text{ GHz}$		-45		dB
HD2	Second-order harmonic distortion	$f = 0.5\text{ GHz}, P_O = +3\text{ dBm}$		-59		dBc
		$f = 2\text{ GHz}, P_O = +3\text{ dBm}$		-56		
		$f = 6\text{ GHz}, P_O = +3\text{ dBm}$		-57		
		$f = 8\text{ GHz}, P_O = +3\text{ dBm}$		-58		
HD3	Third-order harmonic distortion	$f = 0.5\text{ GHz}, P_O = +3\text{ dBm}$		-63		dBc
		$f = 2\text{ GHz}, P_O = +3\text{ dBm}$		-70		
		$f = 6\text{ GHz}, P_O = +3\text{ dBm}$		-62		
		$f = 8\text{ GHz}, P_O = +3\text{ dBm}$		-53		
IMD2	Second-order intermodulation distortion	$f = 0.5\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-60		dBc
		$f = 2\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-56		
		$f = 6\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-50		
		$f = 8\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-46		
IMD3	Third-order intermodulation distortion	$f = 0.5\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-74		dBc
		$f = 2\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-80		
		$f = 6\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-63		
		$f = 8\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		-50		
OP1dB	Output 1-dB compression point	$f = 0.5\text{ GHz}$		9.5		dBm
		$f = 2\text{ GHz}$		14		
		$f = 6\text{ GHz}$		11		
		$f = 8\text{ GHz}$		8		
OIP2	Output second-order intercept point	$f = 0.5\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		55		dBm
		$f = 2\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		51		
		$f = 6\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		45		
		$f = 8\text{ GHz}, P_O = -4\text{ dBm per tone (10-MHz spacing)}$		42		

6.6 Electrical Characteristics: TRF1208B (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $50\text{-}\Omega$ single-ended input, and $100\text{-}\Omega$ differential output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OIP3	Output third-order intercept point	f = 0.5 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		33		dBm
		f = 2 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		36		
		f = 6 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		28		
		f = 8 GHz, $P_O = -4\text{ dBm}$ per tone (10-MHz spacing)		21		
NF	Noise figure	f = 0.5 GHz		9.0		dB
		f = 2 GHz		9.4		
		f = 6 GHz		9.9		
		f = 8 GHz		10.2		
IMPEDANCE						
$Z_{O\text{-DIFF}}$	Differential output impedance	f = DC (internal to the device)		3		Ω
Z_{IN}	Single ended input impedance	INM pin terminated with $50\ \Omega$		50		Ω
TRANSIENT						
V_{OMAX}	Maximum output voltage (differential)			2		V_{PP}
V_{OSAT}	Saturated output voltage level (differential)	f = 2 GHz		2.8		V_{PP}
t_{REC}	Overdrive recovery time	Using a $-0.5\text{-}V_P$ input pulse of 2-ns duration		0.2		ns
POWER SUPPLY						
I_{QA}	Active current	Current on VDD pin, PD = 0		138		mA
I_{QPD}	Power-down quiescent current	Current on VDD pin, PD = 1		7		mA
ENABLE						
V_{PDHIGH}	PD pin logic high		1.45			V
V_{PDLLOW}	PD pin logic low				0.8	V
I_{PDBIAS}	PD bias current (current on PD pin)	PD = high (1.8-V logic)		50	100	μA
		PD = high (3.3-V logic)		200	250	
C_{PD}	PD pin capacitance			2		pF
t_{ON}	Turn-on time	50% V_{PD} to 90% RF		200		ns
t_{OFF}	Turn-off time	50% V_{PD} to 10% RF		50		ns

(1) Calculated using the formula $(S_{21}\text{-}S_{31})/(S_{21}\text{+}S_{31})$. Port-1: INP, Port-2: OUTP, Port-3: OUTM.

6.7 Typical Characteristics: TRF1208

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50- Ω single-ended input, and 100- Ω differential output (unless otherwise noted)

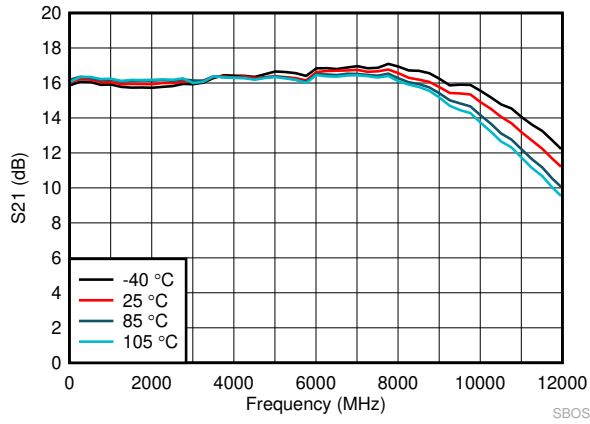


图 6-1. Power Gain Across Temperature

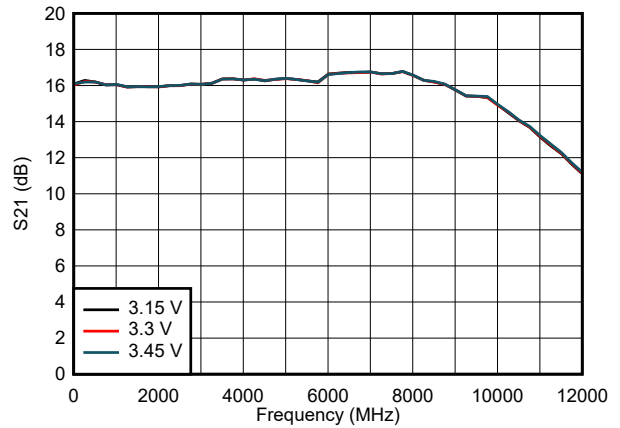


图 6-2. Power Gain Across VDD

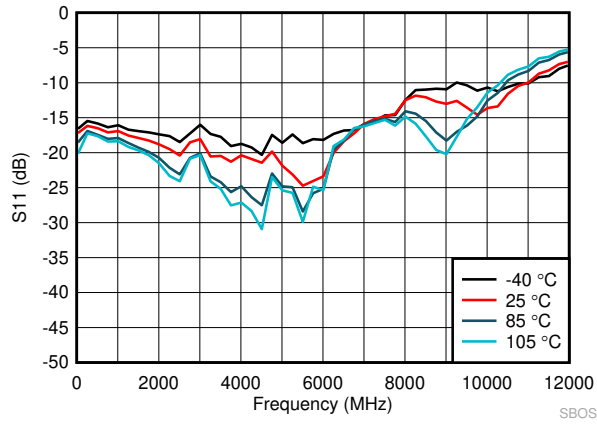


图 6-3. Return Loss Across Temperature

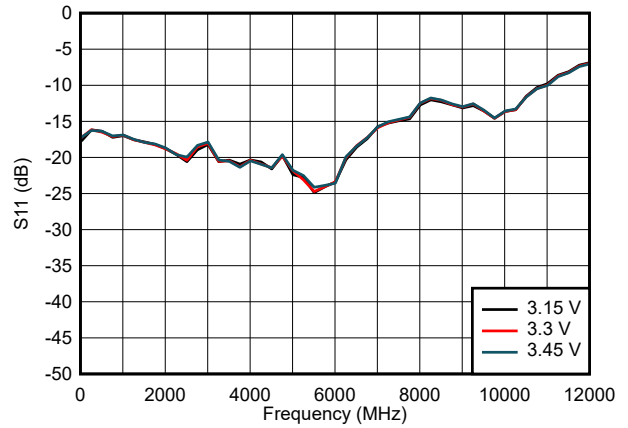


图 6-4. Return Loss Across VDD

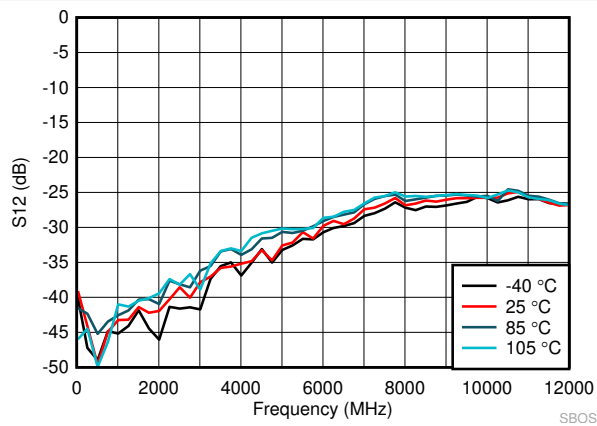


图 6-5. Reverse Isolation Across Temperature

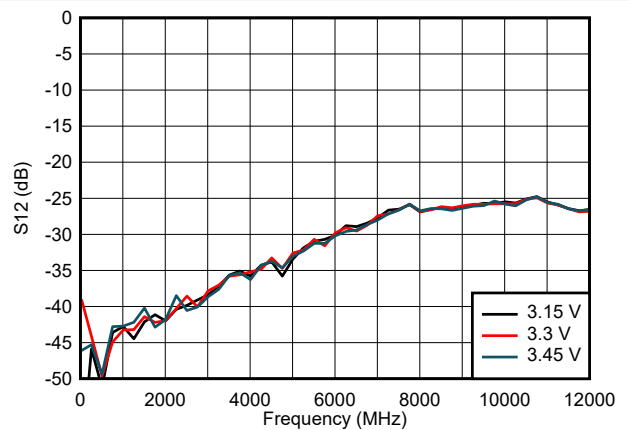
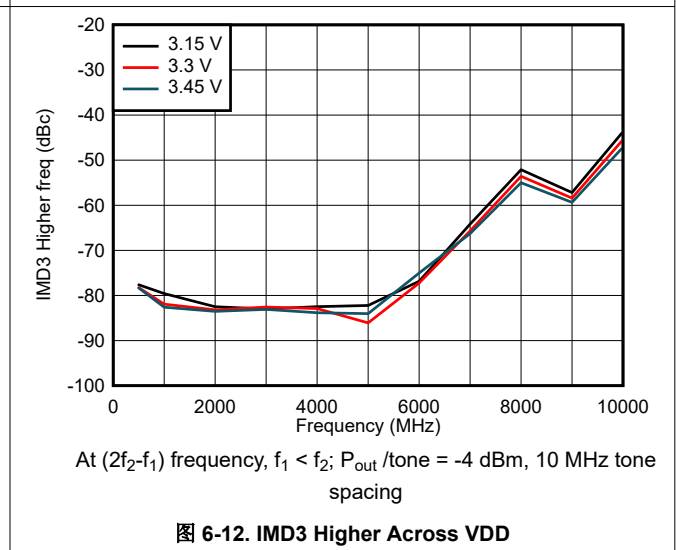
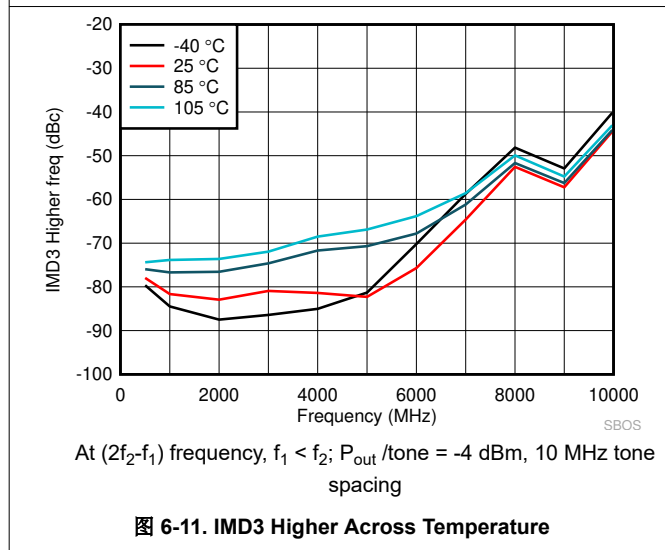
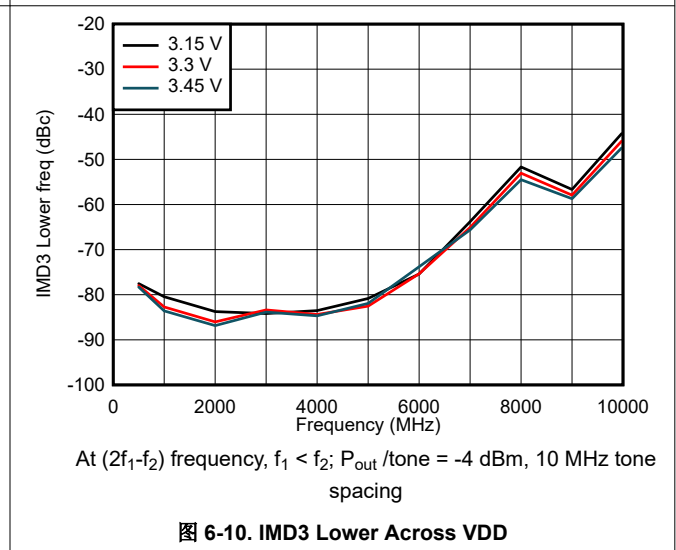
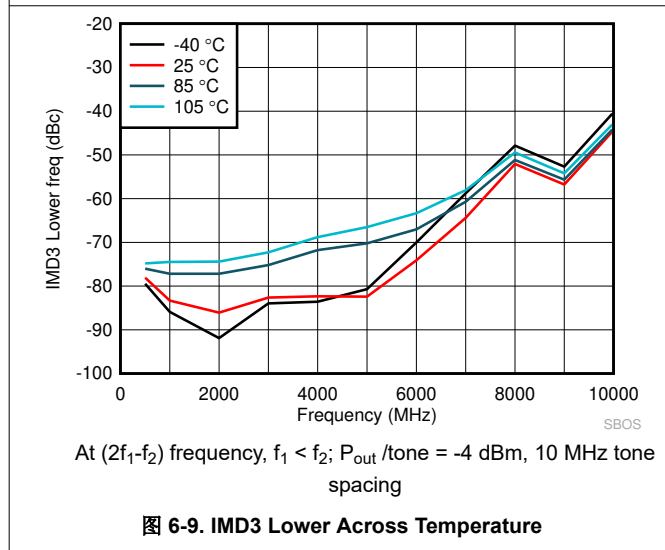
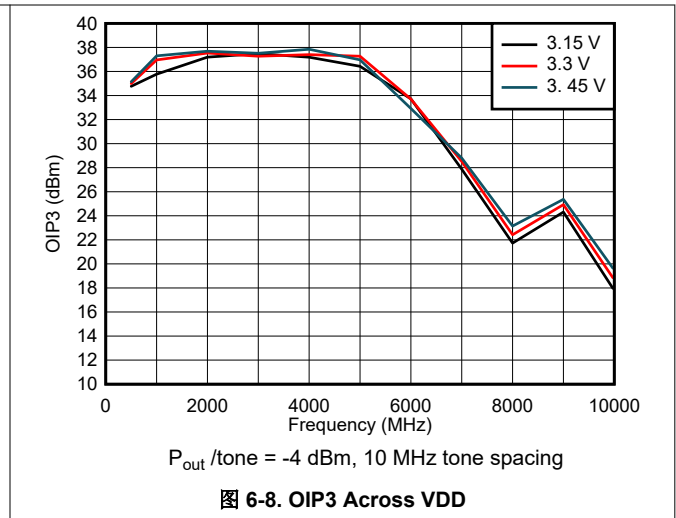
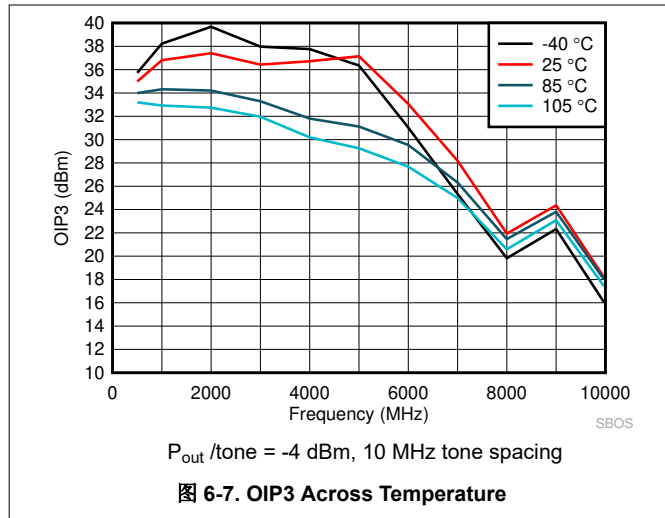


图 6-6. Reverse Isolation Across VDD

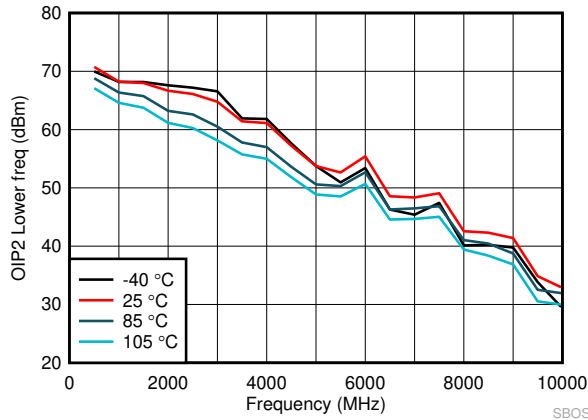
6.7 Typical Characteristics: TRF1208 (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50-Ω single-ended input, and 100-Ω differential output (unless otherwise noted)



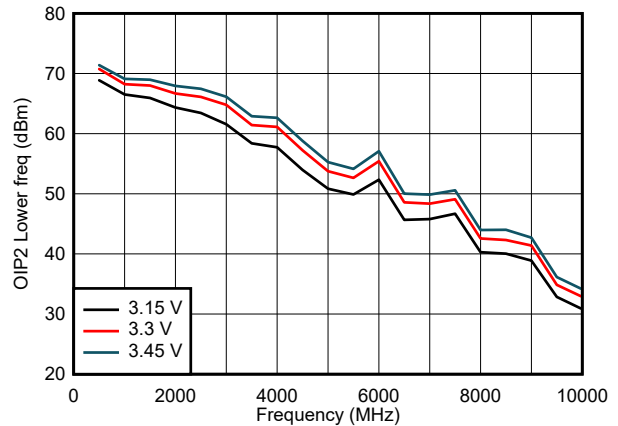
6.7 Typical Characteristics: TRF1208 (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50- Ω single-ended input, and 100- Ω differential output (unless otherwise noted)



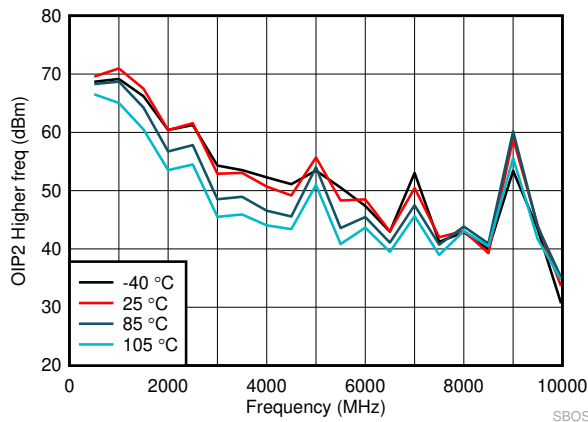
At $(f_2 - f_1)$ frequency, $f_2 > f_1$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-13. OIP2 Lower Across Temperature



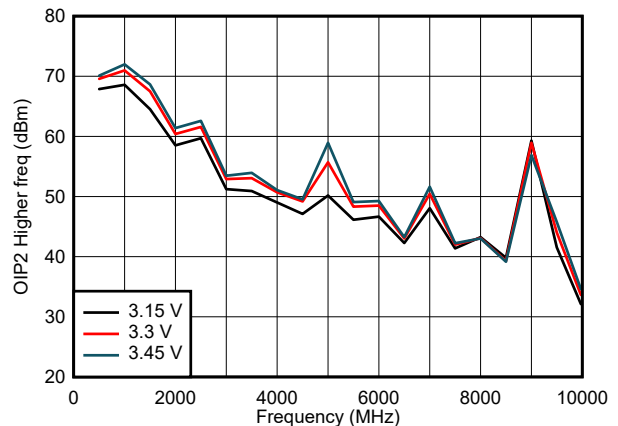
At $(f_2 - f_1)$ frequency, $f_2 > f_1$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-14. OIP2 Lower Across VDD



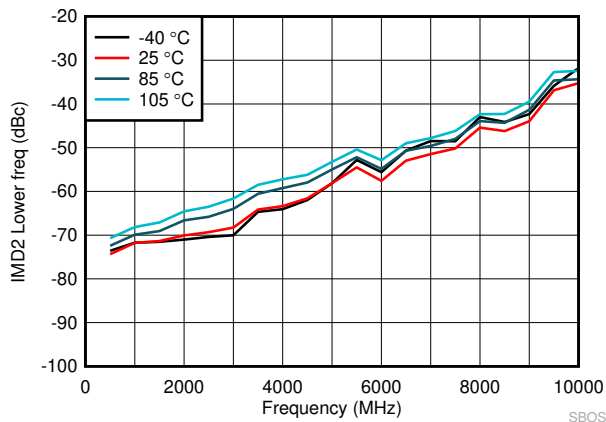
At $(f_2 + f_1)$ frequency, $f_2 > f_1$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-15. OIP2 Higher Across Temperature



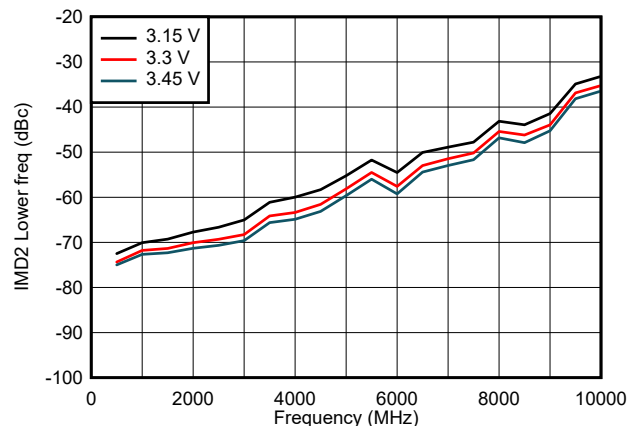
At $(f_2 + f_1)$ frequency, $f_2 > f_1$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-16. OIP2 Higher Across VDD



At $(f_2 - f_1)$ frequency, $f_2 > f_1$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-17. IMD2 Lower Across Temperature



At $(f_2 - f_1)$ frequency, $f_2 > f_1$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-18. IMD2 Lower Across VDD

6.7 Typical Characteristics: TRF1208 (continued)

at temperature = 25°C, V_{DD} = 3.3 V, 50-Ω single-ended input, and 100-Ω differential output (unless otherwise noted)

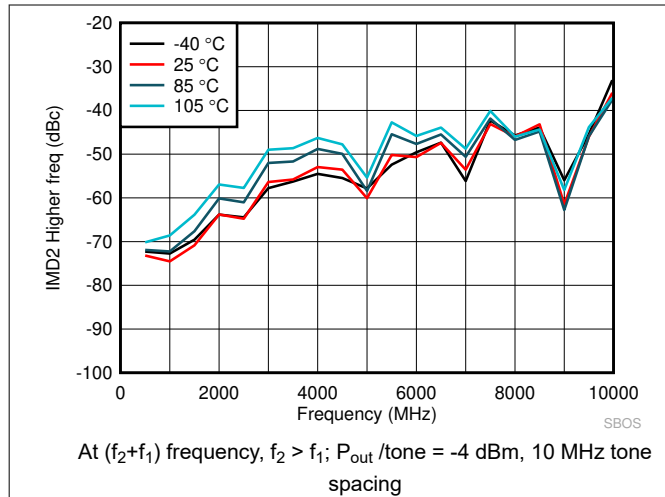


图 6-19. IMD2 Higher Across Temperature

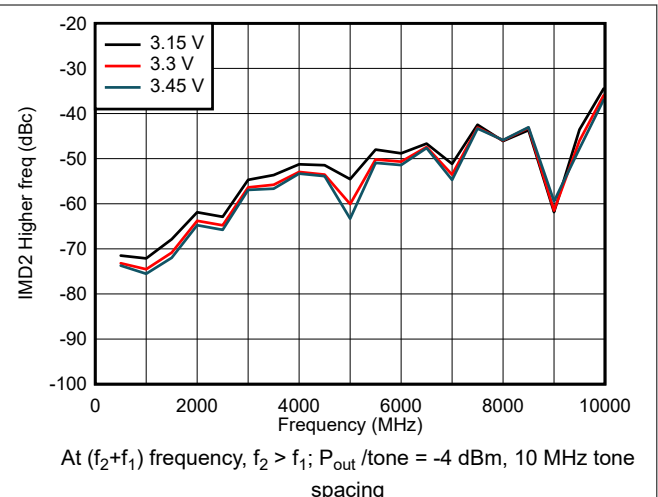


图 6-20. IMD2 Higher Across VDD

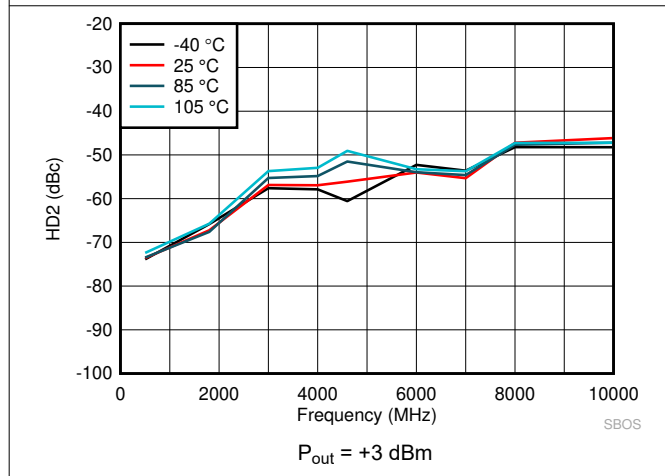


图 6-21. HD2 Across Temperature

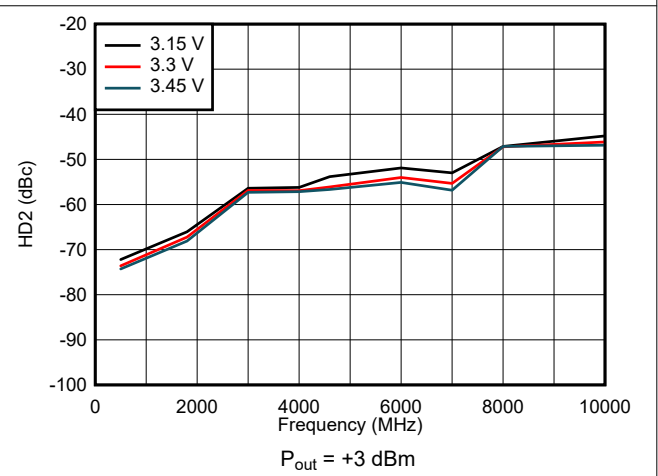


图 6-22. HD2 Across VDD

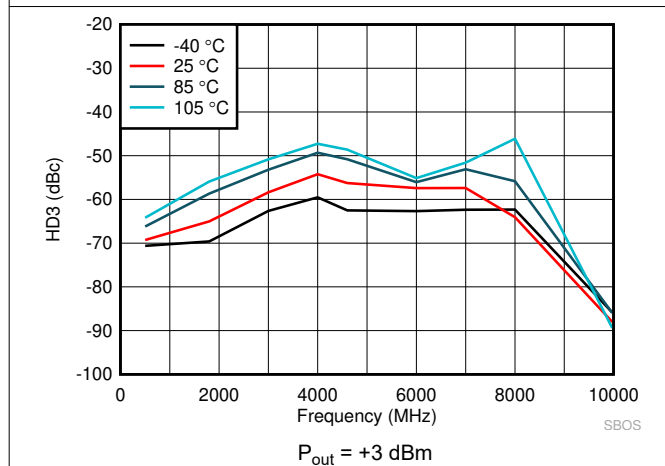


图 6-23. HD3 Across Temperature

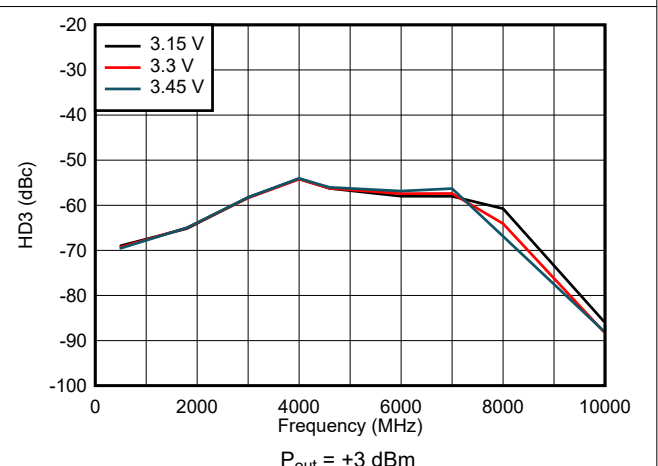
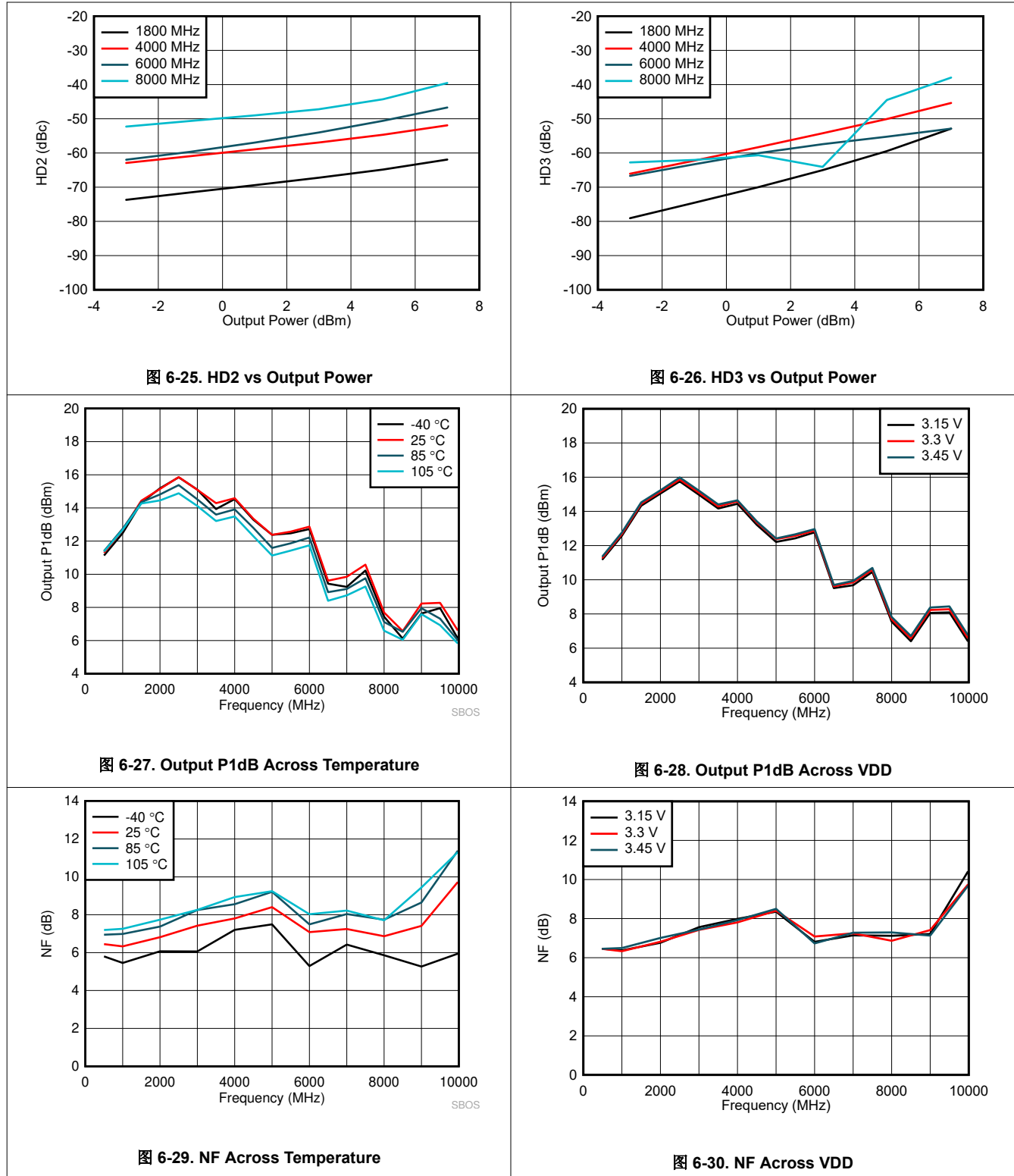


图 6-24. HD3 Across VDD

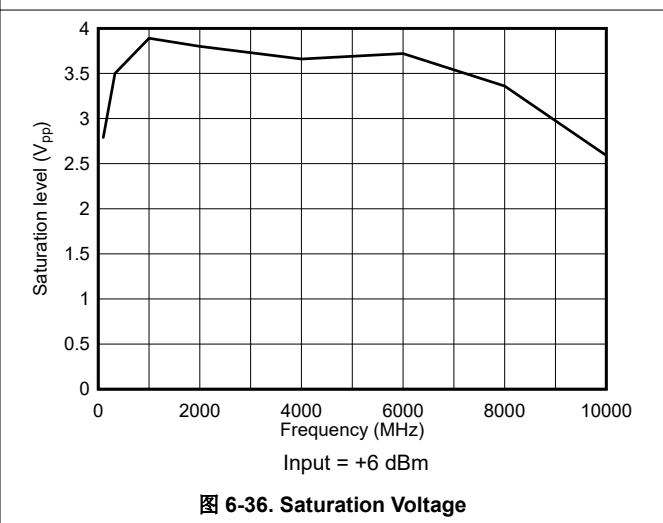
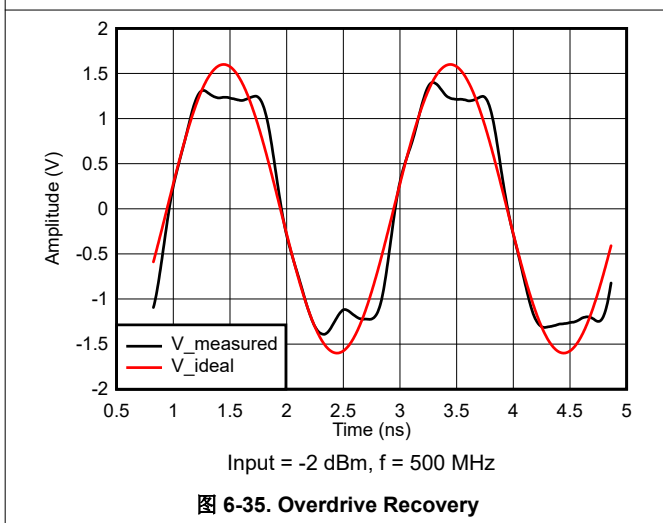
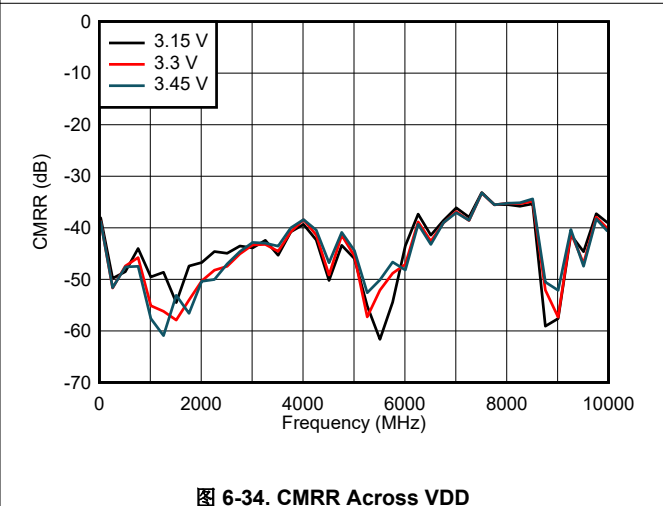
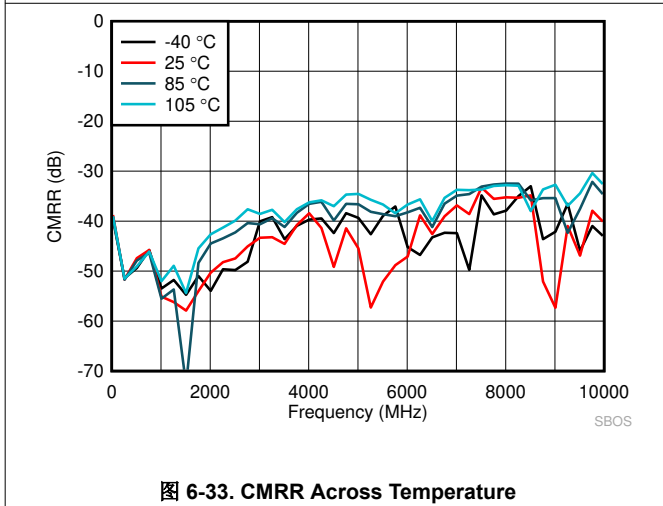
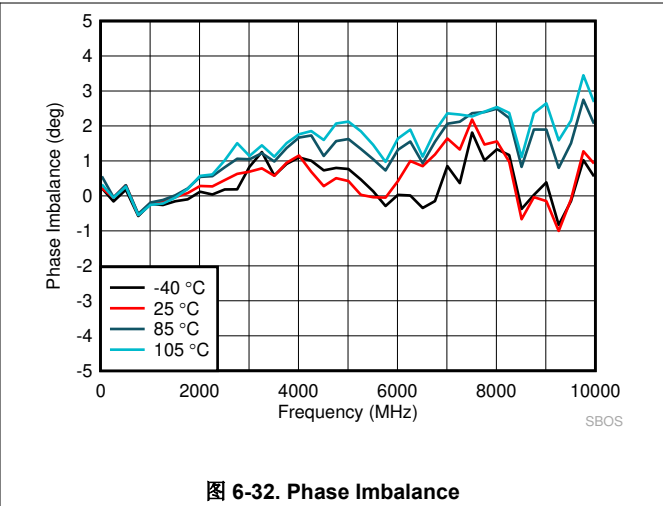
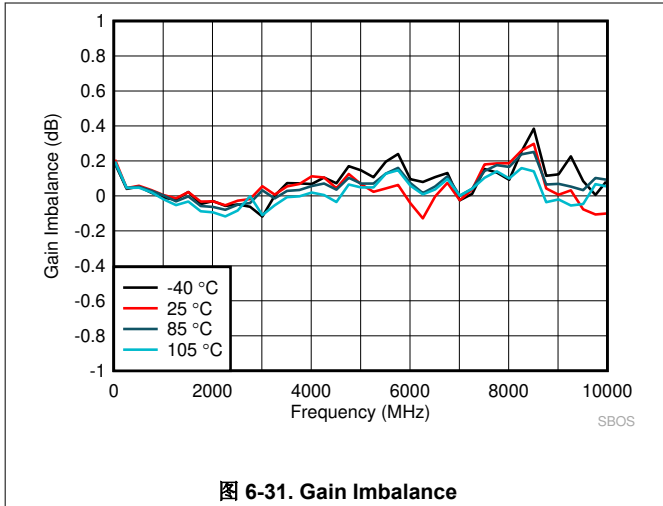
6.7 Typical Characteristics: TRF1208 (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50- Ω single-ended input, and 100- Ω differential output (unless otherwise noted)



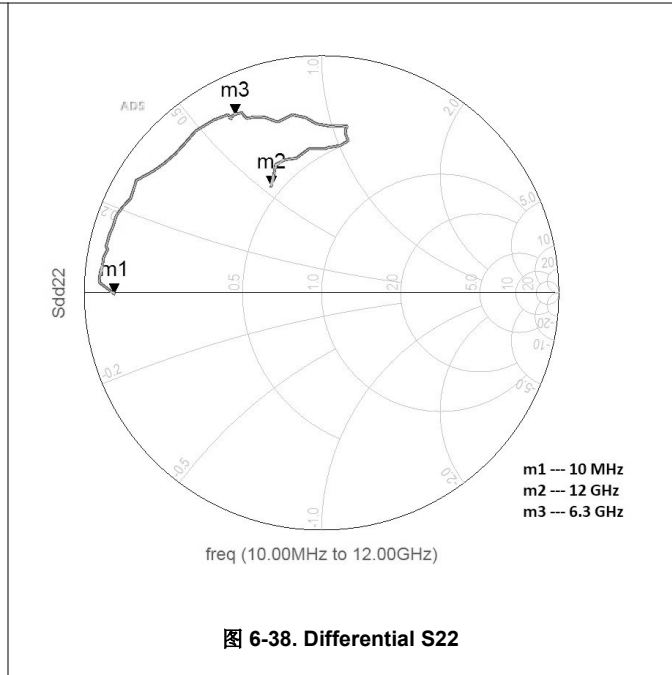
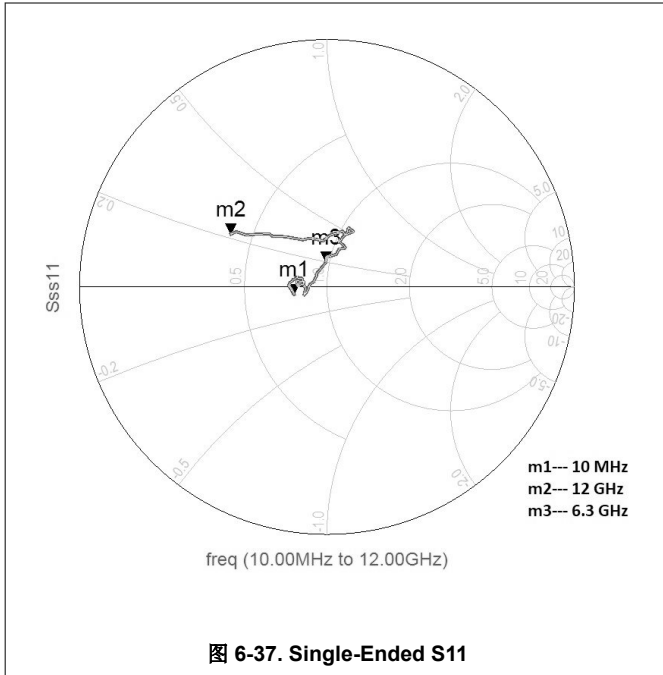
6.7 Typical Characteristics: TRF1208 (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50-Ω single-ended input, and 100-Ω differential output (unless otherwise noted)



6.7 Typical Characteristics: TRF1208 (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50- Ω single-ended input, and 100- Ω differential output (unless otherwise noted)



6.8 Typical Characteristics: TRF1208B

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50-Ω single-ended input, and 100-Ω differential output (unless otherwise noted)

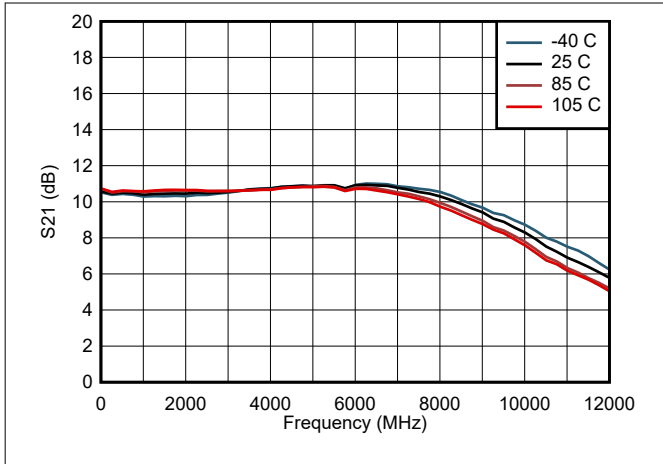


图 6-39. Power Gain Across Temperature

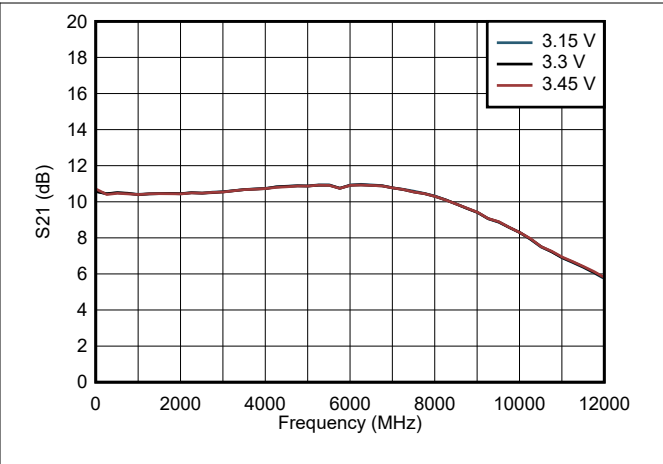


图 6-40. Power Gain Across VDD

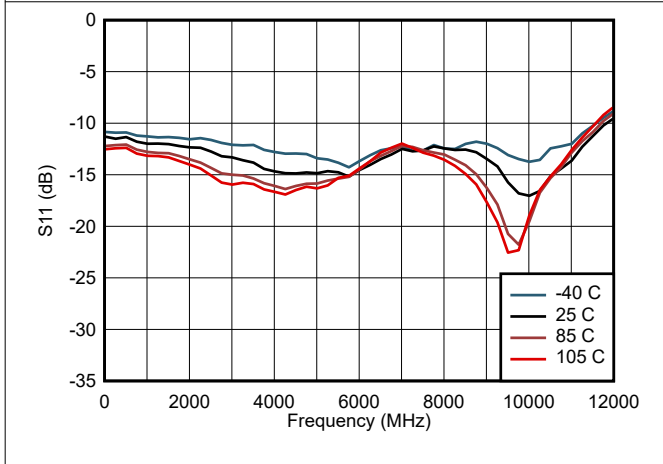


图 6-41. Return Loss Across Temperature

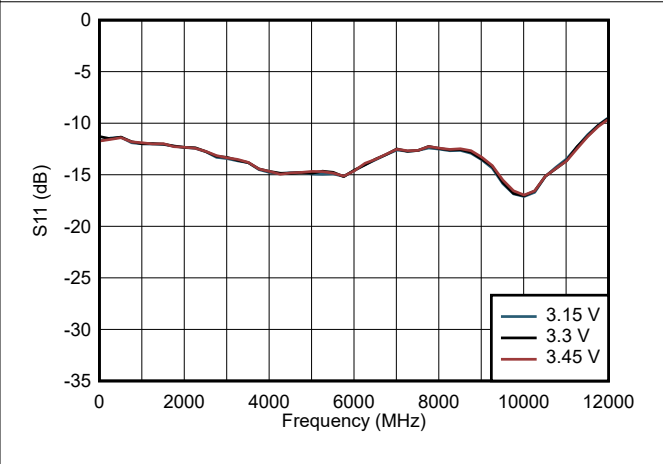


图 6-42. Return Loss Across VDD

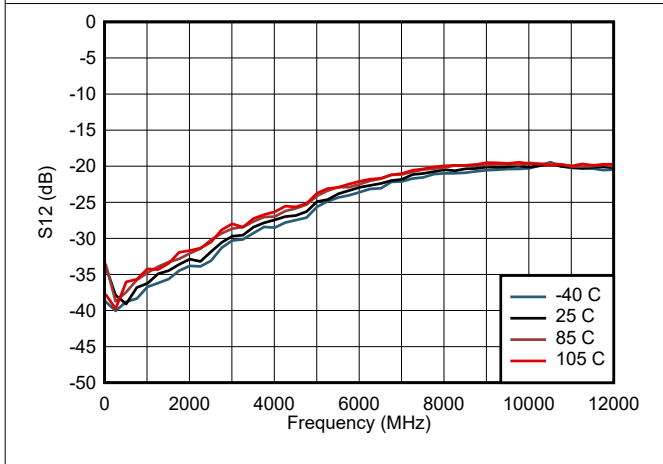


图 6-43. Reverse Isolation Across Temperature

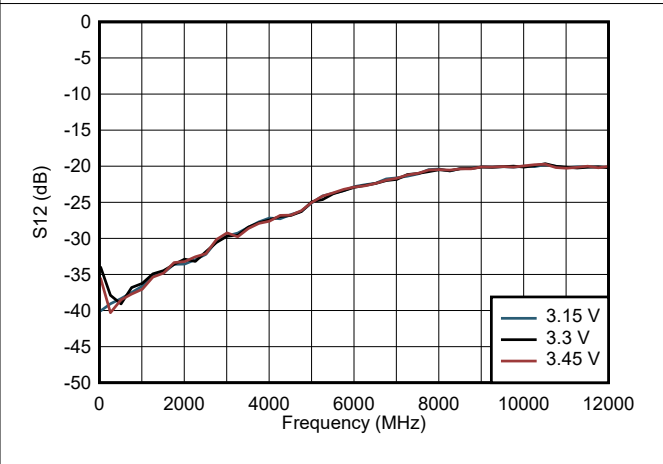
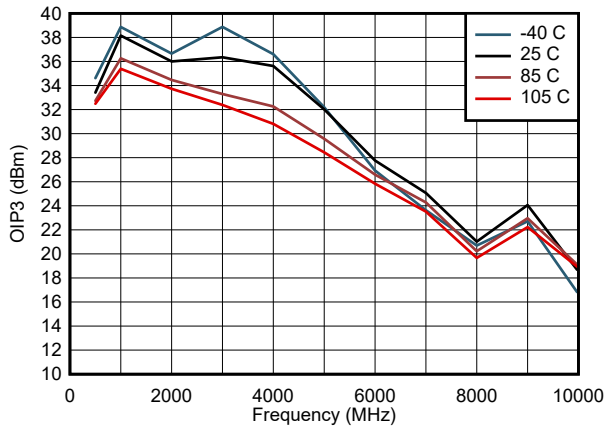


图 6-44. Reverse Isolation Across VDD

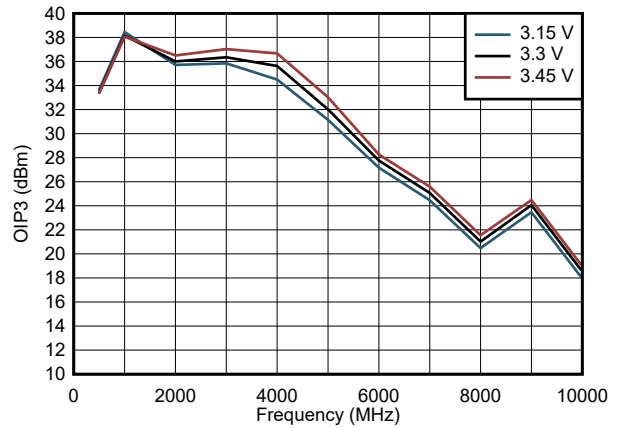
6.8 Typical Characteristics: TRF1208B (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50-Ω single-ended input, and 100-Ω differential output (unless otherwise noted)



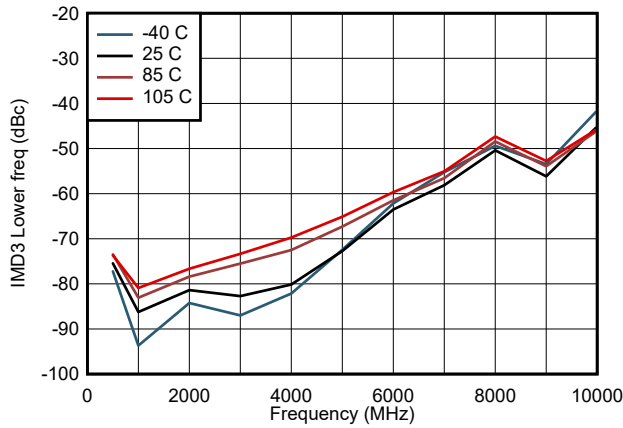
$P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-45. OIP3 Across Temperature



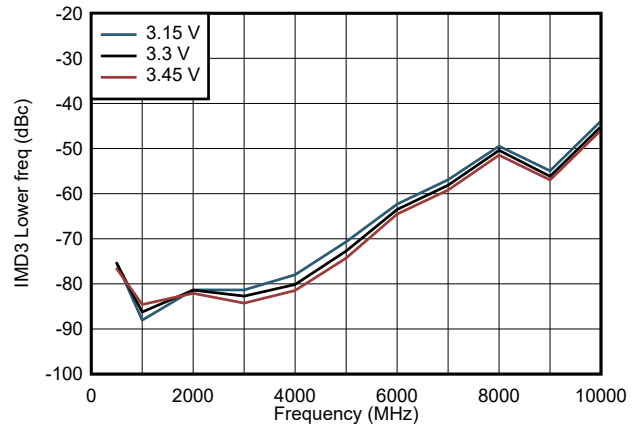
$P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-46. OIP3 Across VDD



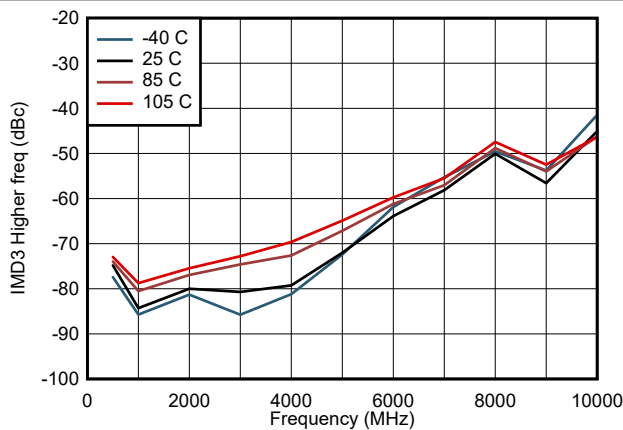
At $(2f_1 - f_2)$ frequency, $f_1 < f_2$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-47. IMD3 Lower Across Temperature



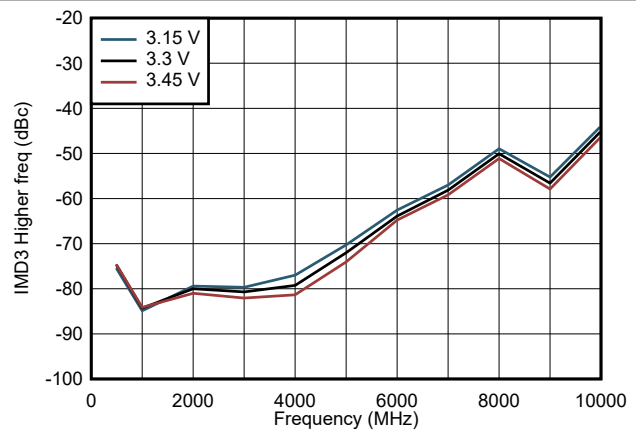
At $(2f_1 - f_2)$ frequency, $f_1 < f_2$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-48. IMD3 Lower Across VDD



At $(2f_2 - f_1)$ frequency, $f_1 < f_2$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-49. IMD3 Higher Across Temperature

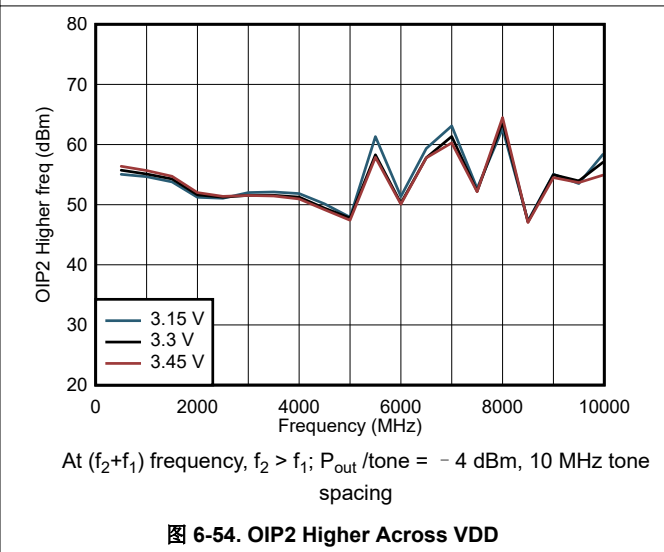
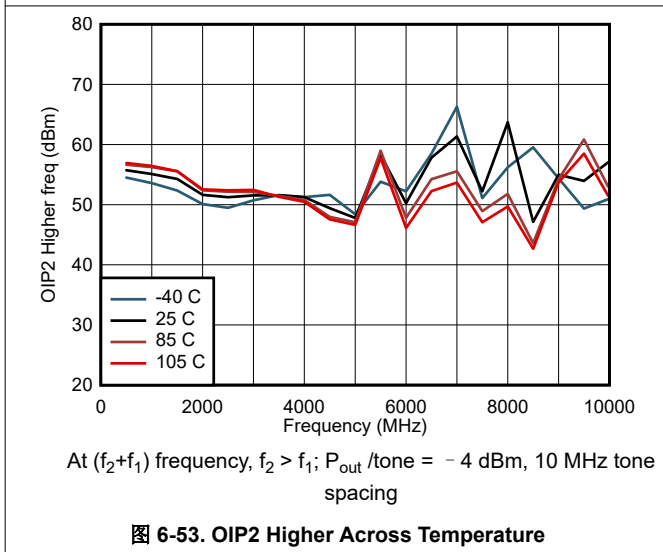
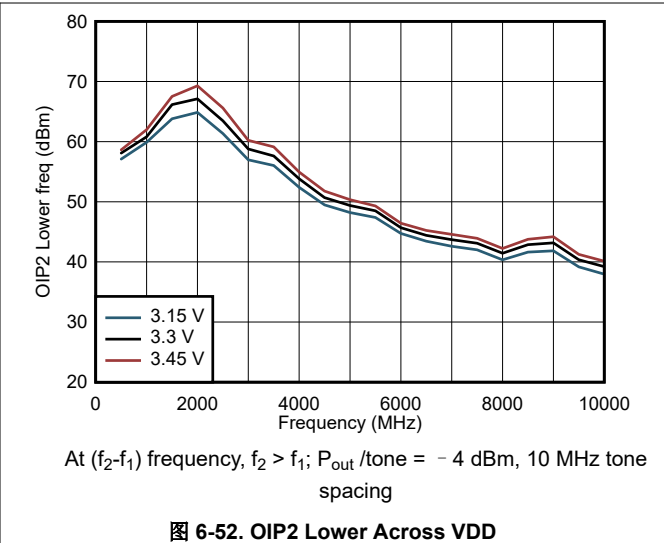
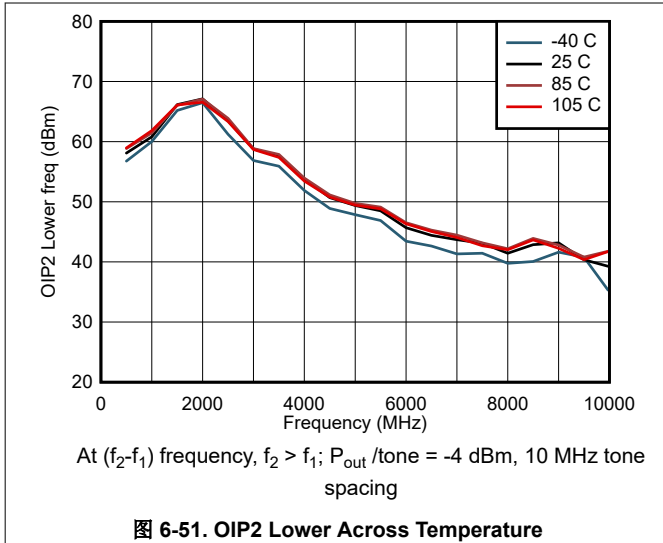


At $(2f_2 - f_1)$ frequency, $f_1 < f_2$; $P_{out}/tone = -4\text{ dBm}$, 10 MHz tone spacing

图 6-50. IMD3 Higher Across VDD

6.8 Typical Characteristics: TRF1208B (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50-Ω single-ended input, and 100-Ω differential output (unless otherwise noted)



6.8 Typical Characteristics: TRF1208B (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50- Ω single-ended input, and 100- Ω differential output (unless otherwise noted)

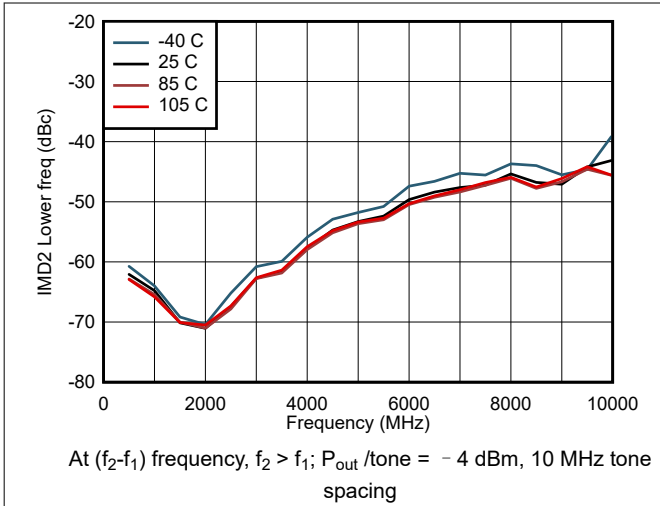


图 6-55. IMD2 Lower Across Temperature

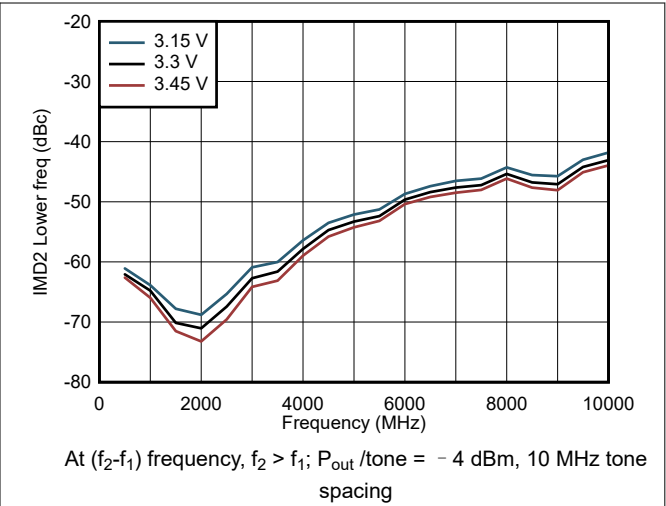


图 6-56. IMD2 Lower Across VDD

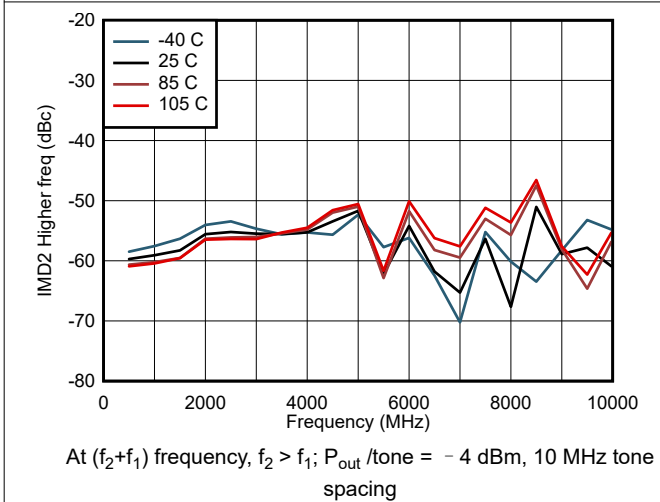


图 6-57. IMD2 Higher Across Temperature

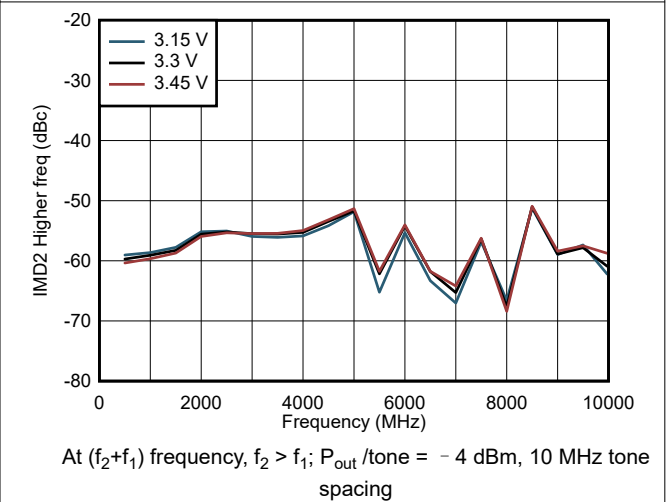


图 6-58. IMD2 Higher Across VDD

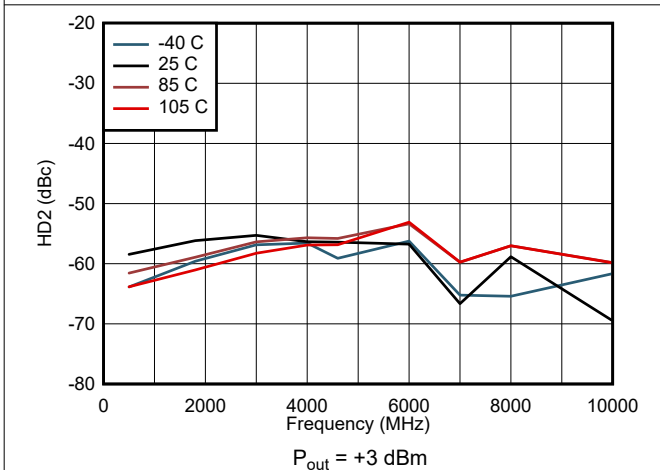


图 6-59. HD2 Across Temperature

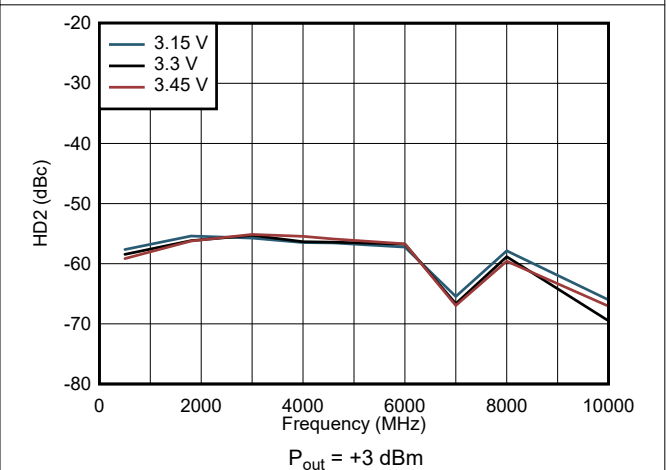


图 6-60. HD2 Across VDD

6.8 Typical Characteristics: TRF1208B (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50-Ω single-ended input, and 100-Ω differential output (unless otherwise noted)

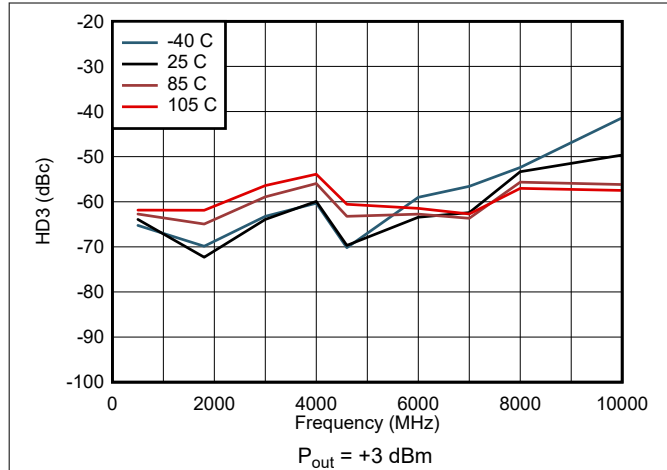


图 6-61. HD3 Across Temperature

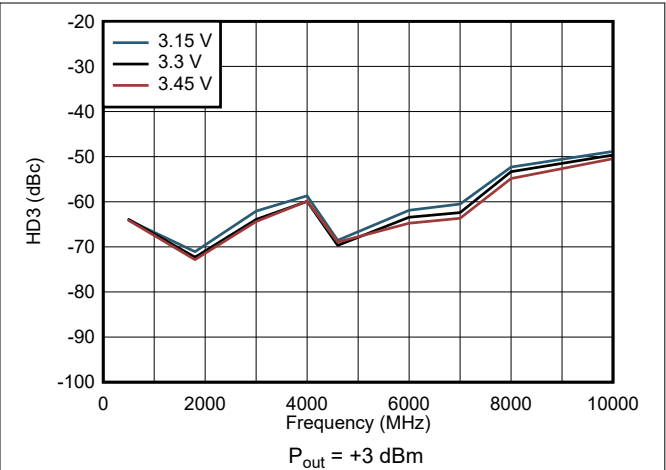


图 6-62. HD3 Across VDD

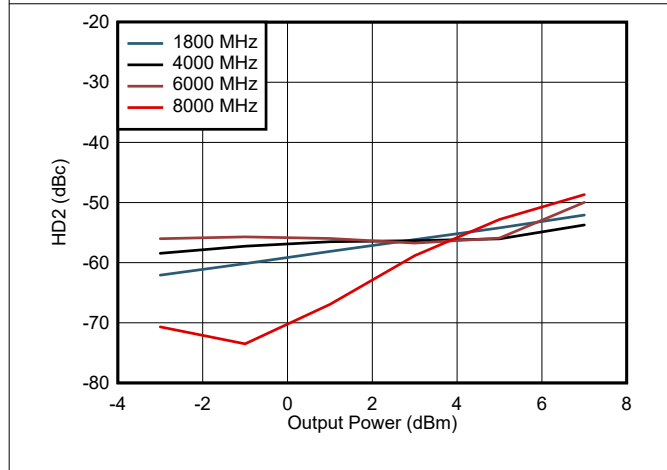


图 6-63. HD2 vs Output Power

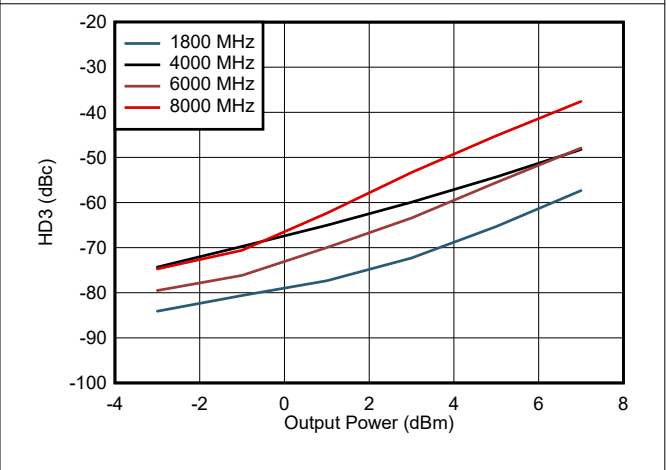


图 6-64. HD3 vs Output Power

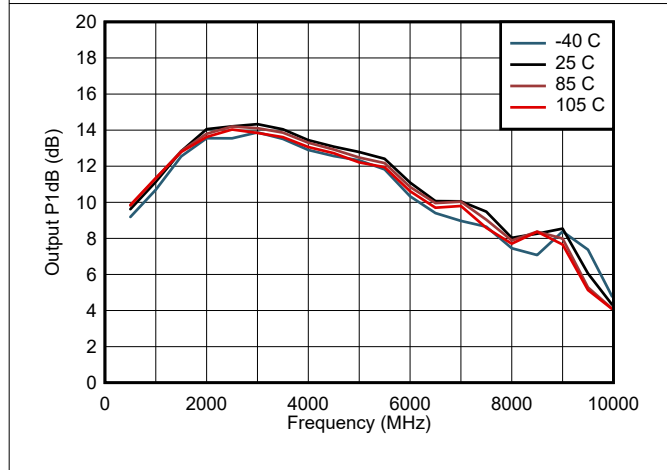


图 6-65. Output P1dB Across Temperature

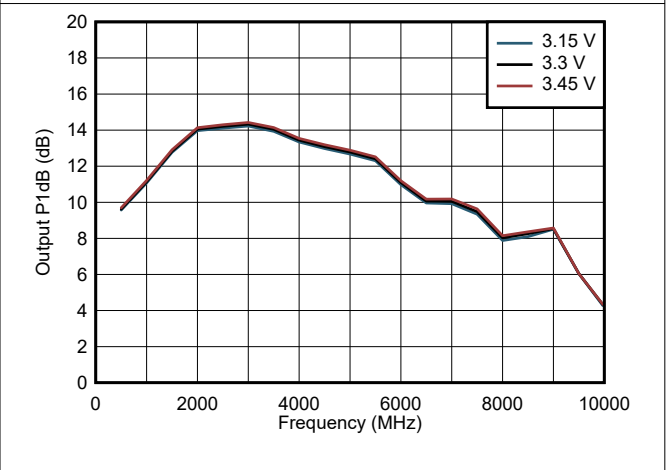


图 6-66. Output P1dB Across VDD

6.8 Typical Characteristics: TRF1208B (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50- Ω single-ended input, and 100- Ω differential output (unless otherwise noted)

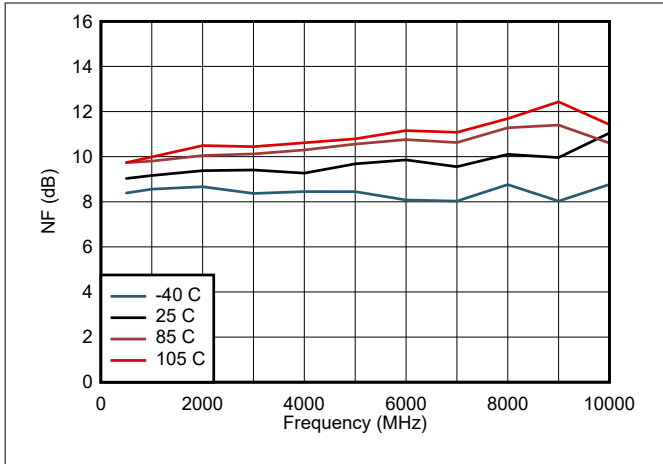


图 6-67. NF Across Temperature

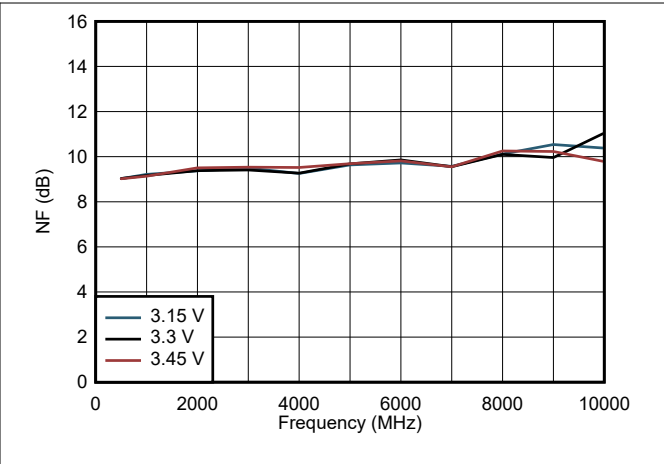


图 6-68. NF Across VDD

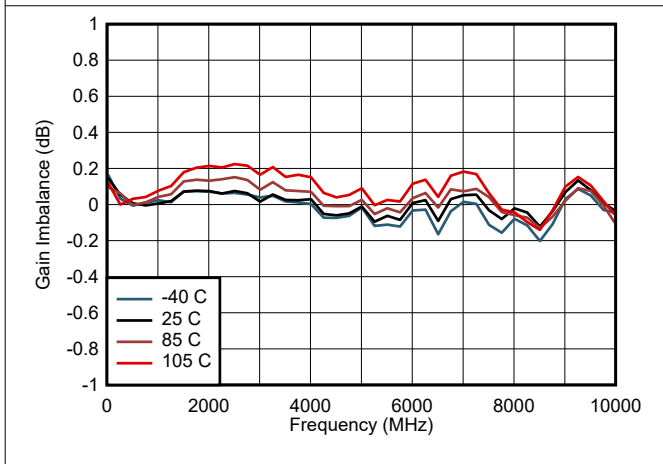


图 6-69. Gain Imbalance

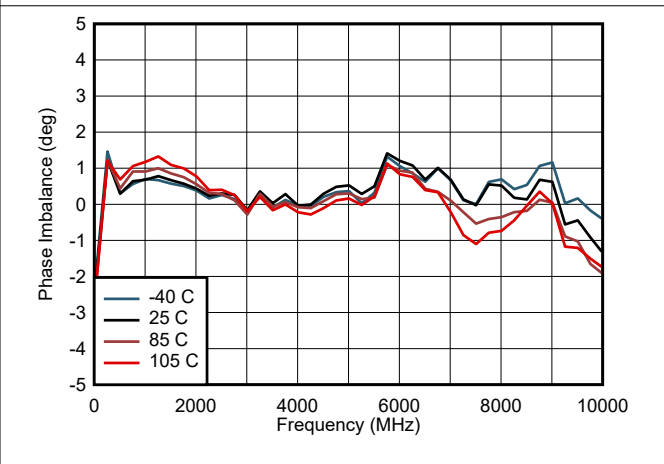


图 6-70. Phase Imbalance

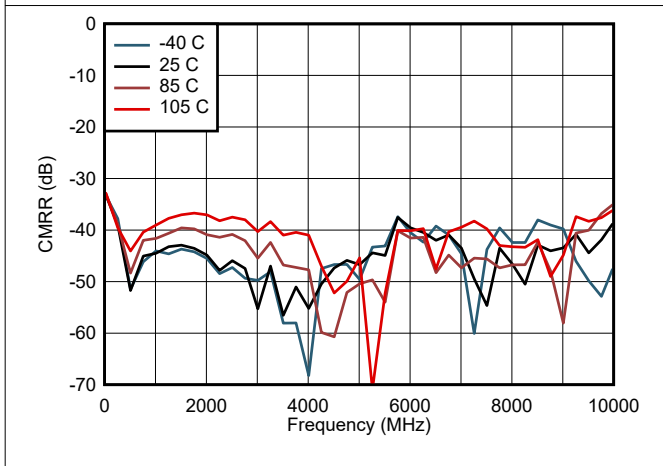


图 6-71. CMRR Across Temperature

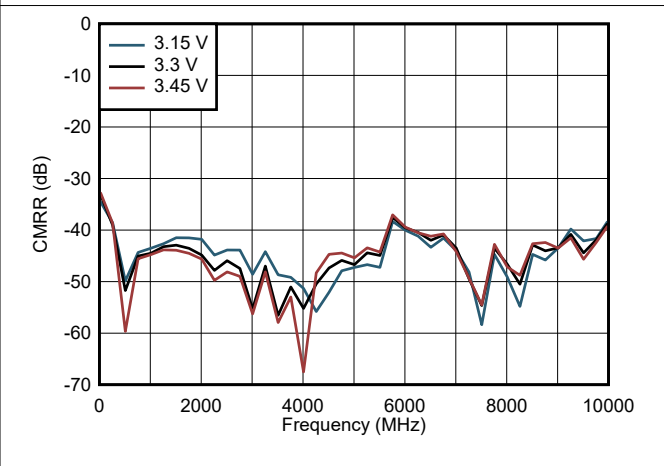
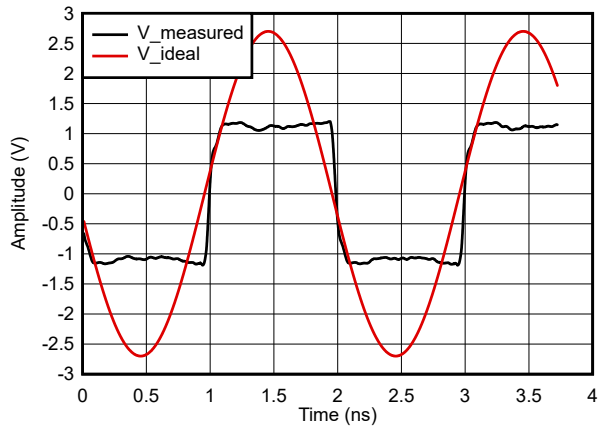


图 6-72. CMRR Across VDD

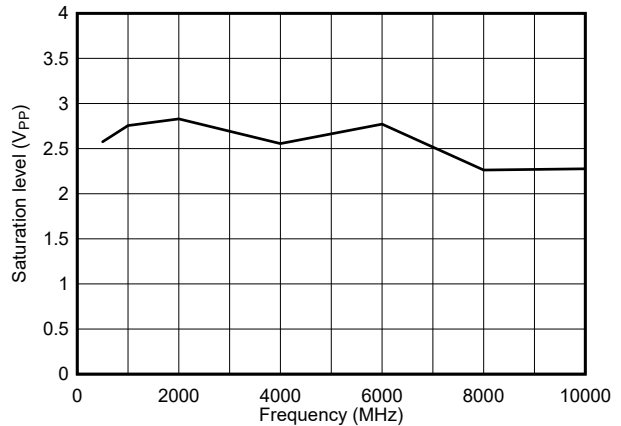
6.8 Typical Characteristics: TRF1208B (continued)

at temperature = 25°C, $V_{DD} = 3.3\text{ V}$, 50-Ω single-ended input, and 100-Ω differential output (unless otherwise noted)



Input = +8 dBm, f = 500 MHz

图 6-73. Overdrive Recovery



Input = +8 dBm

图 6-74. Saturation Voltage

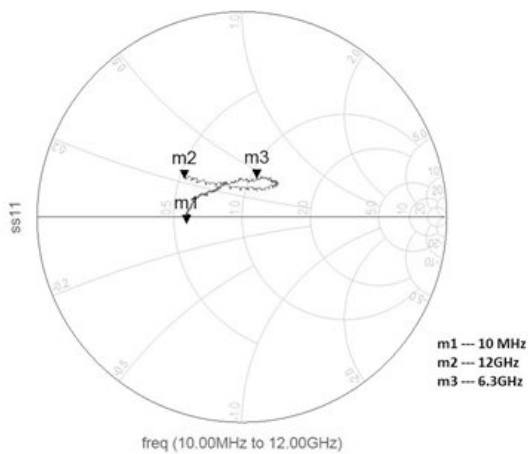


图 6-75. Single-Ended S11

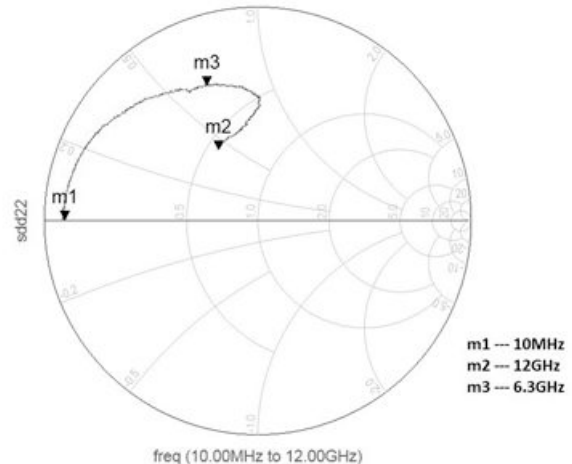


图 6-76. Differential S22

7 Detailed Description

7.1 Overview

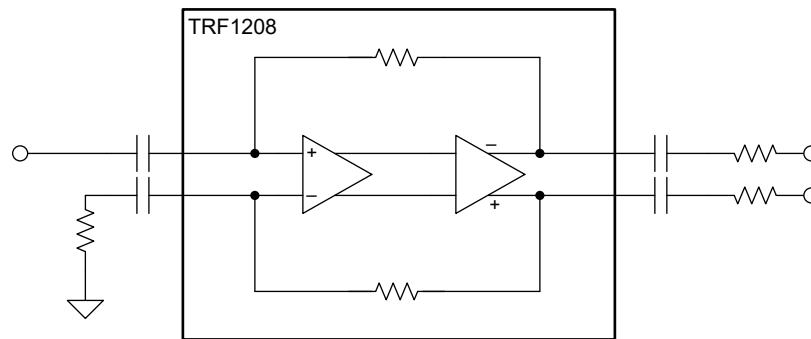
The TRF1208 is a very high-performance amplifier optimized for radio frequency (RF) and intermediate frequency (IF) with signal bandwidths up to 11 GHz. The low frequency response is limited only by the ac-coupling capacitor on the PCB. The device is designed for ac-coupled applications that require a single-ended to differential conversion when driving an analog-to-digital converter (ADC). The device has a two-stage architecture and provides approximately 16 dB of gain for the TRF1208 and approximately 10 dB of gain for TRF1208B when configured for single-ended inputs driven from a 50- Ω source. This device also works as a differential-to-single-ended amplifier to act as a DAC buffer.

This device does not require any pullup or pulldown components on the PCB, and thereby simplifies the layout and provides the highest performance over the entire bandwidth.

The input and output are ac coupled. The TRF1208 is powered with 3.3-V supply. A power-down feature is also available.

7.2 Functional Block Diagram

The following figure shows the functional block diagram of TRF1208. The device essentially has two stages with a voltage-feedback configuration.



7.3 Feature Description

7.3.1 Fully-Differential Amplifier

The TRF1208 is a voltage-feedback fully differential amplifier (FDA) with a fixed gain by architecture. The TRF1208 operates best as a single-ended to differential amplifier by terminating the INM pin with a 50- Ω resistor and driving the INP pin directly with no external components.

This amplifier has nonlinearity cancellation circuits that provide excellent linearity performance over a wide range of frequencies.

The output of the amplifier has a low dc impedance. Therefore, if required, the output of the amplifier can be matched to a load if required by adding the appropriate series resistors or attenuator pad.

7.3.2 Single Supply Operation

The TRF1208 operates on a single 3.3-V supply. The input and output bias voltages are set internally. Therefore, ac-couple the signal path on the board at all four RF input and output pins. Single-supply operation simplifies the board design.

7.4 Device Functional Modes

The TRF1208 has two functional modes: active and power-down. These functional modes are controlled by the PD pin as described in the previous section.

7.4.1 Power-Down Mode

The device features a power-down option. The PD pin is used to power down the amplifier. This pin supports both 1.8-V and 3.3-V digital logic, and is referenced to ground. A logic 1 turns the device off and places the device into a low-quiescent-current state.

When disabled, the signal path is still present through the internal circuits. Input signals applied to a disabled device still appear at the outputs at some lower level through this path, as is the case for any disabled feedback amplifier.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Driving a High-Speed ADC

A common application of the TRF1208 is to drive a high-speed ADC, such as the [ADC12DJ5200RF](#) or [AFE7950](#) that have differential input. Conventionally, passive baluns are used to drive Gbps ADCs because of nonavailability of high-bandwidth, linear amplifiers. The TRF1208 is an active balun that has excellent bandwidth flatness, gain, and phase imbalance comparable to or exceeding costly passive baluns.

图 8-1 shows a typical interface circuit for the ADC12DJ5200RF. Depending on the ADC and system requirement, this circuit can be simplified or can be more complex.

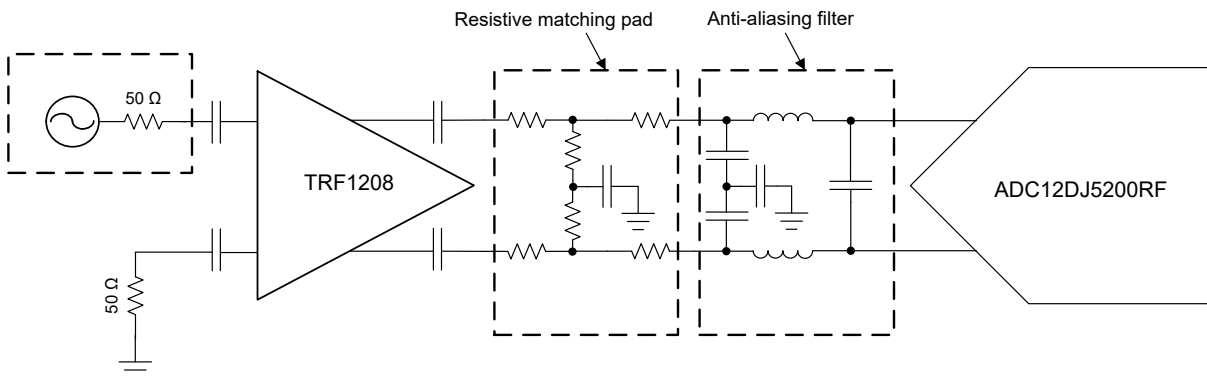
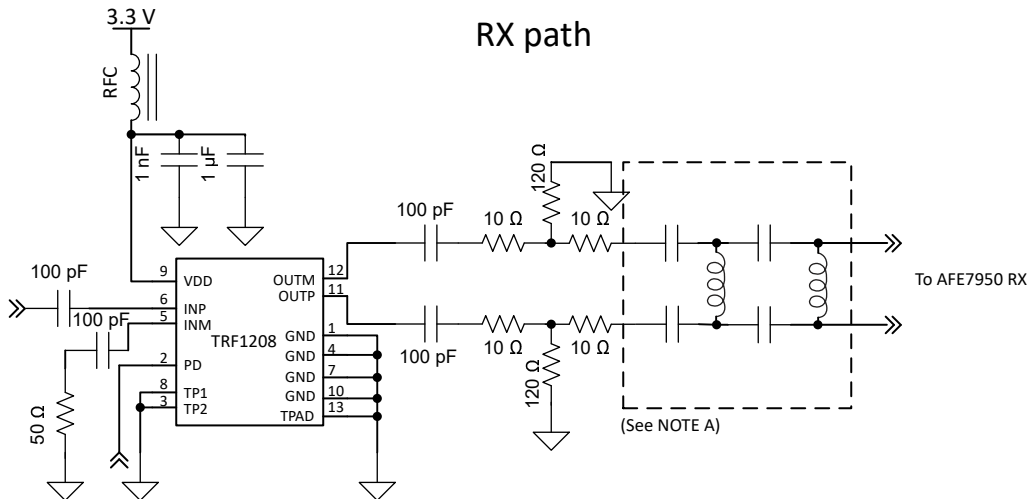


图 8-1. Interfacing With the ADC12DJ5200RF

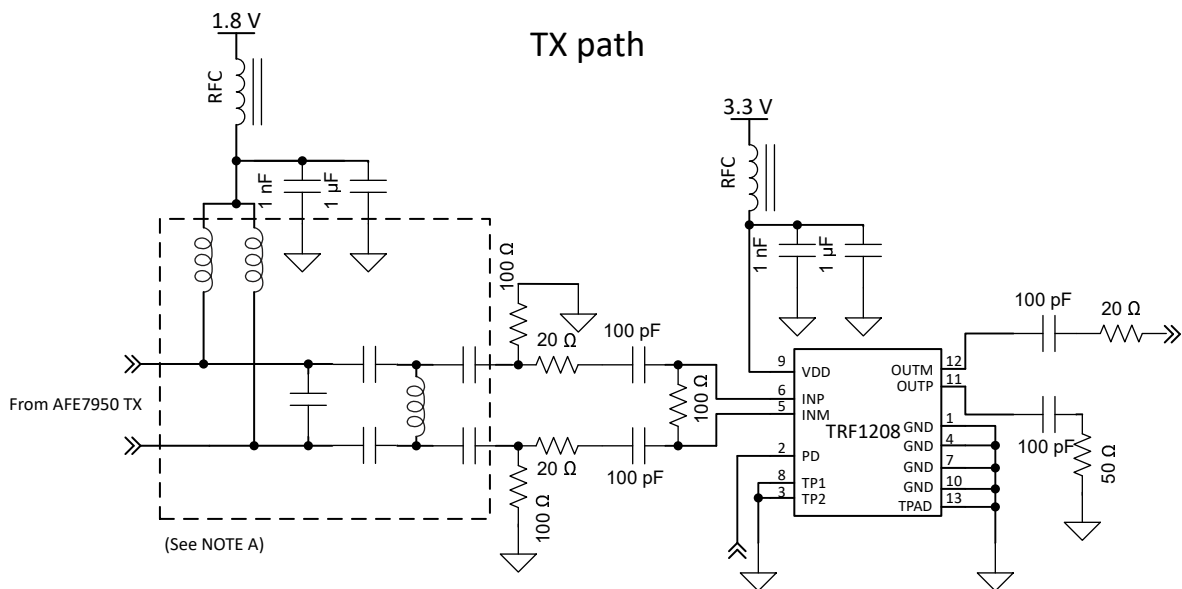
The figure shows two sections of the circuit between the driver amp and the ADC: namely, the matching pad (or attenuator pad) and the antialiasing filter. Use small, form-factor, RF-quality, passive components for these circuits. The output swing of the TRF1208 is designed to drive these ADCs full-scale, while at the same time not overdrive the device. This functionality avoids the need for any voltage limiting device at the ADC.

The following figures show typical interface circuits for AFE7950 RX and TX chains in which TRF1208 is the S2D and D2S amplifier, respectively.



- A. AFE matching network - component type (whether L or C) and values depend on the channel (A, B, C, D, FB1, FB2) and frequency band.

图 8-2. Interfacing With the AFE7950 RX



- A. AFE matching network - component type (whether L or C) and values depend on the channel (A, B, C, D) and frequency band.

图 8-3. Interfacing With the AFE7950 TX

8.1.2 Calculating Output Voltage Swing

This section gives a quick reference of the output voltage swings for different input power levels. In this example, the output is terminated with a 100-Ω differential load and a power gain of 16 dB is assumed.

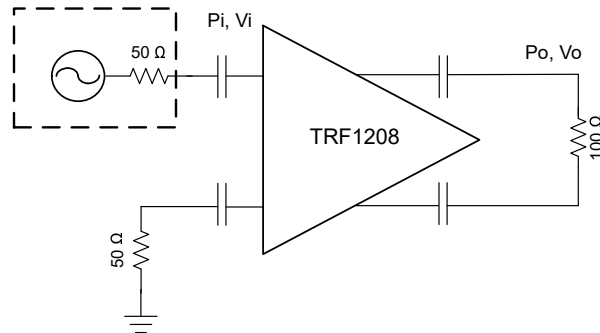


图 8-4. Power and Voltage Levels

$$\text{Voltage gain} = 20 \times \log(V_O / V_I) \quad (1)$$

$$\text{Power gain} = 10 \times \log(P_O / P_I) = 10 \times \log((V_O^2 / 100) / (V_I^2 / 50)) = 20 \times \log(V_O / V_I) - 3 \text{ dB} \quad (2)$$

表 8-1. Output Voltage Swings for Different Input Power Levels

INPUT		OUTPUT (TRF1208)		OUTPUT (TRF1208B)	
P _I (dBm)	V _I (V _{PP})	P _O (dBm)	V _O (V _{PP})	P _O (dBm)	V _O (V _{PP})
- 20	0.063	- 4	0.564	- 10	0.283
- 15	0.112	1	1.004	- 5	0.503
- 10	0.2	6	1.785	0	0.894
- 9	0.224	7	2.002	1	1.004

8.1.3 Thermal Considerations

The TRF1208 is available in a 2-mm × 2-mm, WQFN-FCRLF package that has excellent thermal properties. Connect the thermal pad underneath the chip to a ground plane. Short the ground plane to the other ground pins of the chip at four corners, if possible, to allow heat propagation to the top layer of PCB. Use a thermal via that connects the thermal pad plane on the top layer of the PCB to the inner layer ground planes to allow heat propagation to the inner layers.

The total power dissipation needs to be limited to keep the device junction temperature below 150°C for instantaneous power and below 125°C for continuous power.

8.2 Typical Applications

An example of TRF1208 acting as ADC and DAC amplifiers for AFE7950 is explained in this section.

8.2.1 TRF1208 in Receive Chain

This section describes an RF receiver chain in which TRF1208 is working as a S2D (SE-to-diff) amp and driving a receive channel of AFE7950.

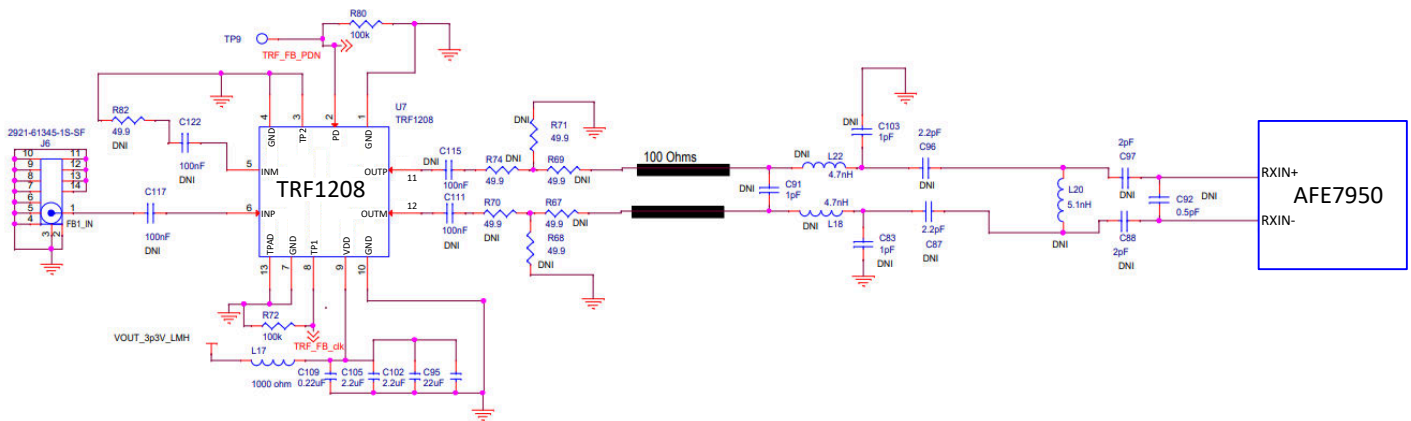


图 8-5. TRF1208 in a Receive Chain With the AFE7950

The previous figure is a generic schematic of a design in which TRF1208 drives an AFE7950 receive channel. The exact values of the components depend on the frequency band for which the AFE7950 front-end is matched.

8.2.1.1 Design Requirements

The AFE7950 channel is required to be matched to 8.2 GHz.

8.2.1.2 Detailed Design Procedure

The TRF1208 is configured as an S2D amplifier. The section close to TRF1208 output is an attenuator pad that is meant for robust matching. The section close to AFE7950 is the matching network for the AFE that is channel dependent. The matching components are chosen based on the AFE return-loss data and some trial and error because the manufactured board parameters can influence the exact component values

表 8-2 shows the bill of materials (BOM) values of the design for a channel that is matched to center frequency of 8.2 GHz.

表 8-2. Component Values of RX Chain With Center Frequency = 8.2 GHz

SECTION	DESIGNATOR	TYPE	VALUE	PART NUMBER	INSTALL / DNI
DC block cap	C117	Capacitor	100 nF	530L104KT	Install
DC block cap	C115	Capacitor	100 nF	530L104KT	Install
DC block cap	C111	Capacitor	100 nF	530L104KT	Install
DC block cap	C122	Capacitor	100 nF	530L104KT	Install
Attenuator	R74	Resistor	10 Ω	ERJ-1GEF10R0C	Install
Attenuator	R70	Resistor	10 Ω	ERJ-1GEF10R0C	Install
Attenuator	R69	Resistor	10 Ω	ERJ-1GEF10R0C	Install
Attenuator	R67	Resistor	10 Ω	ERJ-1GEF10R0C	Install
Attenuator	R71	Resistor	140 Ω	ERJ-1GNF1400C	Install
Attenuator	R68	Resistor	140 Ω	ERJ-1GNF1400C	Install
INM term	R82	Resistor	50 Ω	ERJ-1GEF49R9C	Install
Matching	C91	—	—	—	DNI
Matching	L20	—	—	—	DNI
Matching	C103	—	—	—	DNI
Matching	C83	—	—	—	DNI
Matching	L22	Inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	L18	Inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	C96	Inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	C87	Inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	C97	Capacitor	0.8 pF	02015J0R8PBSTR	Install
Matching	C88	Capacitor	0.8 pF	02015J0R8PBSTR	Install
Matching	C92	Inductor	0.3 nH	LQP03TG0N3B02#	Install

TRF1208

ZHCSLL7C - OCTOBER 2021 - REVISED AUGUST 2023

8.2.2 TRF1208 in a Transmit Chain

This section describes an RF transmit chain in which the TRF1208 works as a differential-to-single-ended converter that converts the DAC output of the AFE7950 into a single-ended signal that drives a PA or a mixer.

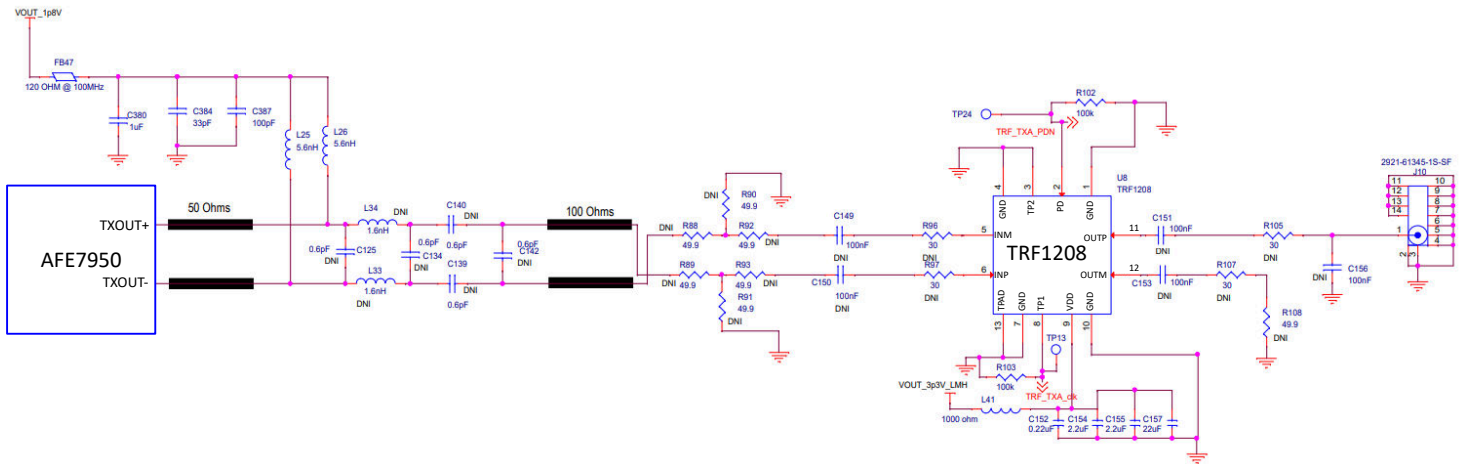


图 8-6. TRF1208 in a Transmit Chain With the AFE7950

The previous figure is a generic schematic of a design in which the TRF1208 is used with the AFE7950 in the transmit chain. The exact values of the components depend on the frequency band for which the AFE7950 front-end is matched.

8.2.2.1 Design Requirements

The AFE7950 channel is required to be matched to 8.2 GHz.

8.2.2.2 Detailed Design Procedure

The TRF1208 is configured as a D2S amplifier. The OUTM pin of the TRF1208 is terminated with 50 Ω and OUTP is taken out as the SE output. The section close to TRF1208 input is an attenuator pad that is meant for robust matching. The section close to AFE7950 is the matching network for the AFE, which is channel dependent. Choose matching components based on the AFE return-loss data and some trial and error because the board parameters can influence the exact values.

表 8-3 shows the BOM values of the design for a channel that is matched to center frequency of 8.2 GHz.

表 8-3. Component Values of TX Chain With Center Frequency = 8.2 GHz

SECTION	DESIGNATOR	TYPE	VALUE	PART NUMBER	INSTALL / DNI
Supply inductor	L25	Inductor	2 nH	LQP03TG2N0B02#	Install
Supply inductor	L26	Inductor	2 nH	LQP03TG2N0B02#	Install
Matching	C125	—	—	—	DNI
Matching	C142	—	—	—	DNI
Matching	C156	—	—	—	DNI
Matching	L34	Capacitor	0.7 pF	02015J0R7PBSTR	Install
Matching	L33	Capacitor	0.7 pF	02015J0R7PBSTR	Install
Matching	C134	Inductor	0.5 nH	LQP03TG0N5B02#	Install
Matching	C140	Inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	C139	Inductor	0.1 nH	LQP03TG0N1B02#	Install
DC block cap	C149	Capacitor	100 nF	530L104KT	Install
DC block cap	C150	Capacitor	100 nF	530L104KT	Install
DC block cap	C151	Capacitor	100 nF	530L104KT	Install
DC block cap	C153	Capacitor	100 nF	530L104KT	Install
Attenuator	R88	Resistor	20 Ω	ERJ-1GNF20R0C	Install
Attenuator	R89	Resistor	20 Ω	ERJ-1GNF20R0C	Install
Attenuator	R92	Resistor	20 Ω	ERJ-1GNF20R0C	Install
Attenuator	R93	Resistor	20 Ω	ERJ-1GNF20R0C	Install
Attenuator	R90	Resistor	57.6 Ω	ERJ-1GNF57R6C	Install
Attenuator	R91	Resistor	57.6 Ω	ERJ-1GNF57R6C	Install
Term	R105	Resistor	0 Ω	ERJ-1GN0R00C	Install
Term	R107	Resistor	0 Ω	ERJ-1GN0R00C	Install
Term	R96	Resistor	10 Ω	ERJ-1GEF10R0C	Install
Term	R97	Resistor	10 Ω	ERJ-1GEF10R0C	Install
Term	R108	Resistor	50 Ω	ERJ-1GEF49R9C	Install

8.3 Power Supply Recommendations

The TRF1208 requires a single 3.3-V supply. Supply decoupling is critical to high-frequency performance. Typically two or three capacitors are used for supply decoupling. For the lowest-value capacitor, use a small, form-factor component that is placed closest to the VDD pin of the device. Use a bulk decoupling capacitor of a larger value and size that can be placed next to the small capacitor. Additional layout recommendations are given in the *Layout* section.

8.4 Layout

8.4.1 Layout Guidelines

The TRF1208 is a wideband, voltage-feedback amplifier with approximately 10 dB or 16 dB of gain. When designing with a wideband RF amplifier with relatively high gain, make sure to take certain board layout precautions to maintain stability and optimized performance. Use a multilayer board to maintain signal and power integrity and thermal performance. 图 8-7 shows an example of a good layout. In this figure, only the top layer is shown.

Route the RF input and output lines as grounded coplanar waveguide (GCPW) lines. For the second layer, use a continuous ground layer without any ground-cuts near the amplifier area. Match the output differential lines in length to minimize phase imbalance. Use small footprint passive components wherever possible. Also take care of the input side layout. Use a 50-ohm line for the INP routing, and make sure the termination on INM pin has low parasitics by placing the ac-coupling capacitor and the 50- Ω resistor very close to the device. Use an RF-quality, 50- Ω resistor for termination. Make sure that the ground planes on the top and internal layers are well stitched with vias.

Place thermal vias under the device that connect the top thermal pad with ground planes in the inner layers of the PCB. For improved heat dissipation, connect the thermal pad to the top layer ground plane through the ground pins (see the *Layout Example* in the next section).

8.4.2 Layout Example

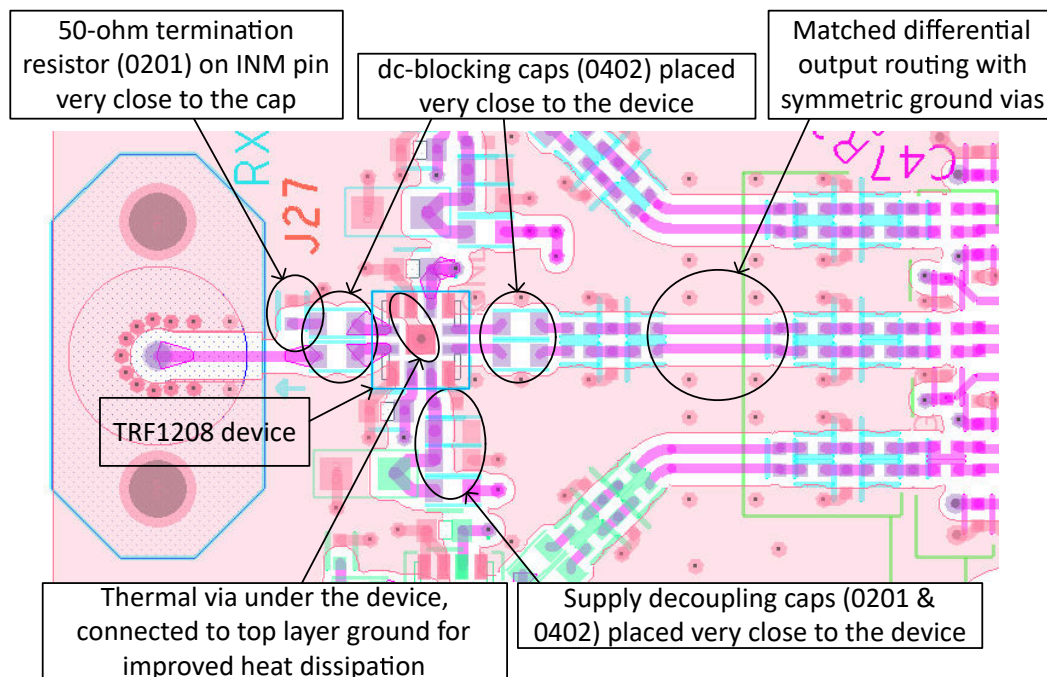


图 8-7. Layout Example: Placement and Top Layer Layout

The TRF1208 can be evaluated using the TRF1208 EVM board, which can be ordered from [TRF1208](#) product folder. Additional information about the evaluation board construction and test setup is given in the [TRF1208 EVM User's Guide](#).

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TRF0206-SP EVM User's Guide](#)

9.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF1208BRPVR	ACTIVE	WQFN-HR	RPV	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	128L	Samples
TRF1208RPVR	ACTIVE	WQFN-HR	RPV	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1208	Samples
TRF1208RPVT	ACTIVE	WQFN-HR	RPV	12	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1208	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1208BRPVR	WQFN-HR	RPV	12	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q1
TRF1208RPVR	WQFN-HR	RPV	12	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q1
TRF1208RPVT	WQFN-HR	RPV	12	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q1

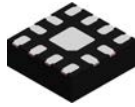
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

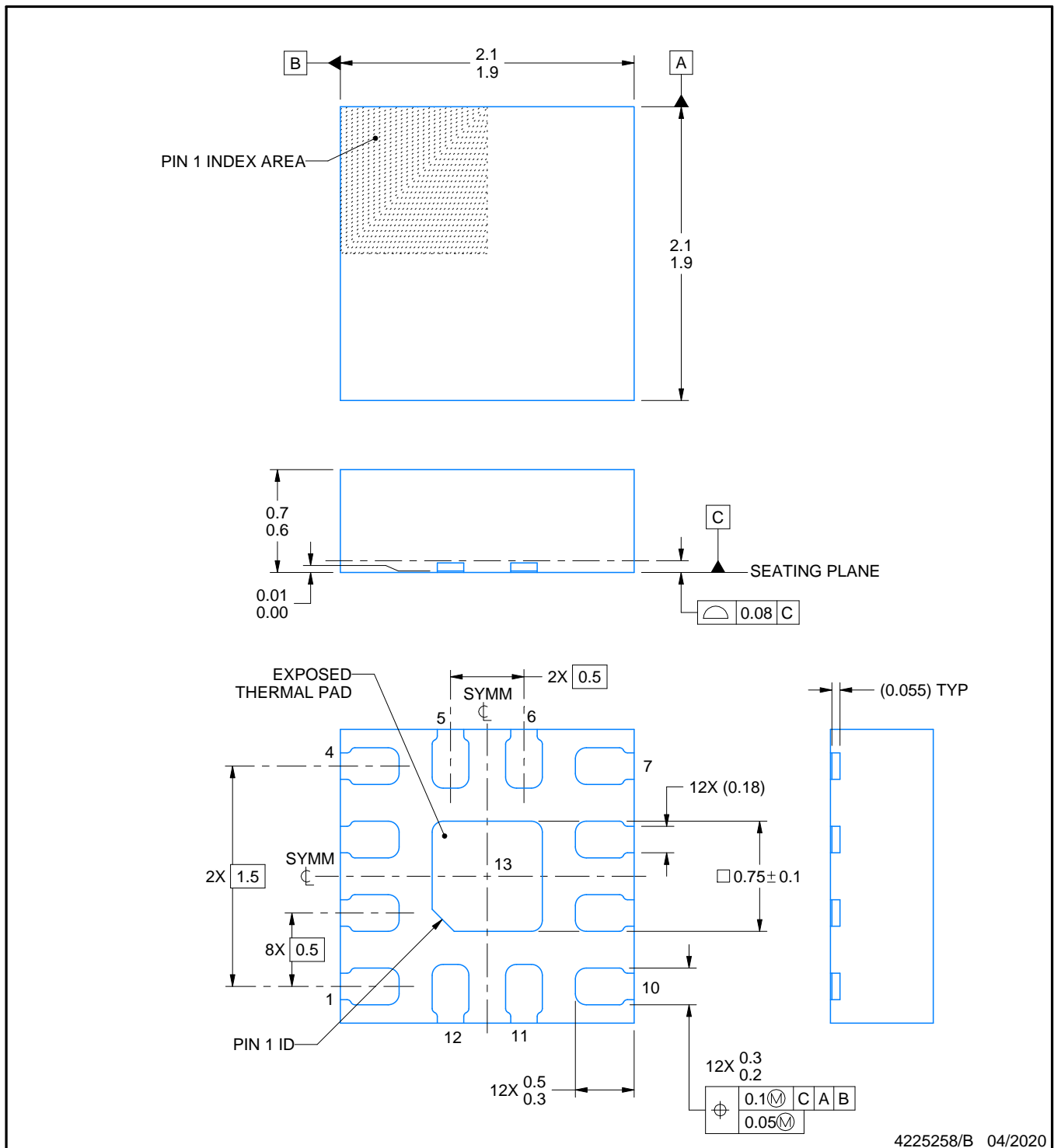
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1208BRPVR	WQFN-HR	RPV	12	3000	205.0	200.0	33.0
TRF1208RPVR	WQFN-HR	RPV	12	3000	205.0	200.0	33.0
TRF1208RPVT	WQFN-HR	RPV	12	250	205.0	200.0	33.0

RPV0012A



PACKAGE OUTLINE WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

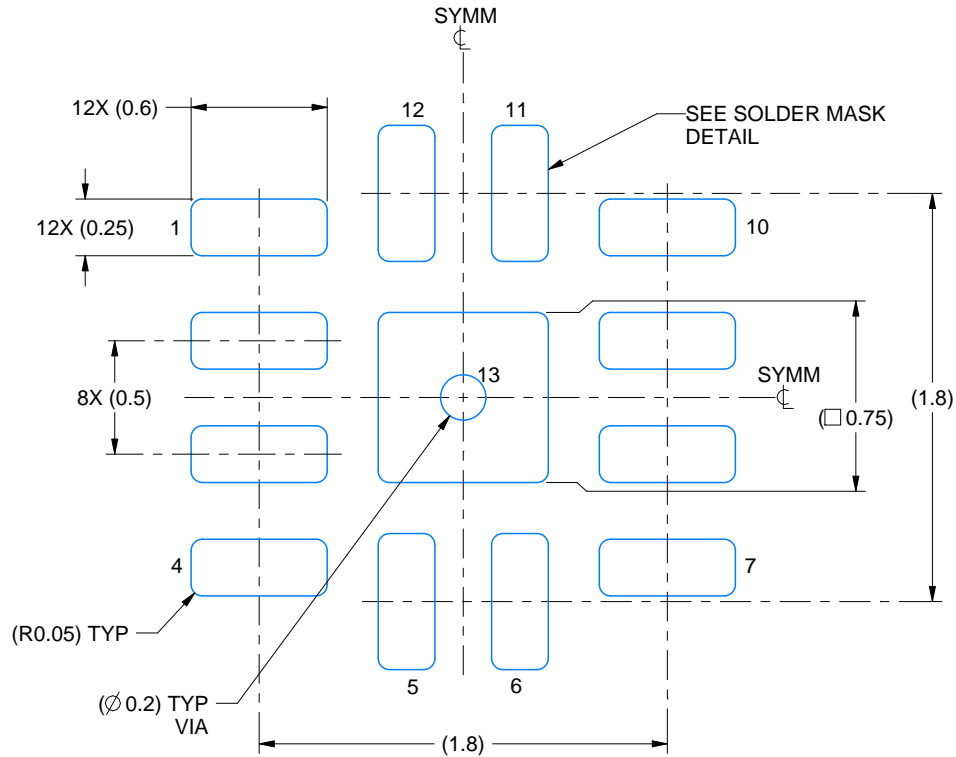
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RPV0012A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4225258/B 04/2020

NOTES: (continued)

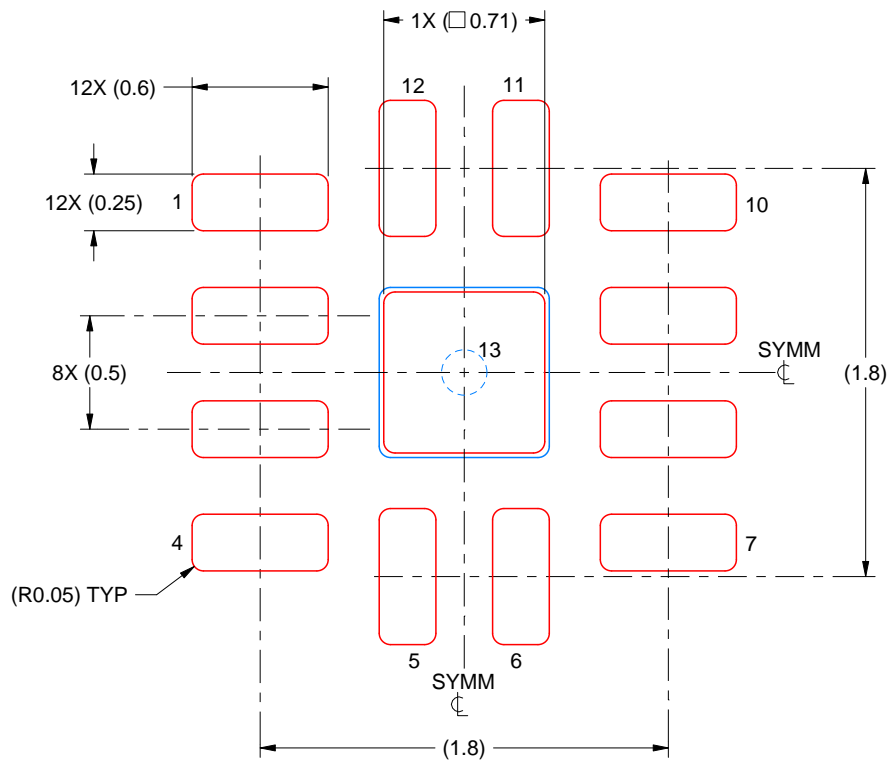
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RPV0012A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225258/B 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司