# TUSB4020BI-Q1 汽车级双端口 USB 2.0 集线器

## 1 特性

- 符合汽车应用要求的 AEQ-Q100 标准
  - 器件温度等级 3：–40°C 至 85°C $T_A$
- 双端口 USB 2.0 集线器
- USB 2.0 集线器特性：
  - 多事务转换器 (MTT) 集线器：两个事务转换器
  - 每个事务转换器具有四个异步端点缓冲器
- 兼容 Type C
- 支持电池充电
  - CDP 模式（上行端口已连接）
  - DCP 模式（上行端口未连接）
  - DCP 模式符合中国电信行业标准 YD/T 1591-2009
  - D+/D– 分压器模式
- 支持每端口或成组电源开关以及过流通知输入
- OTP ROM、串行 EEPROM 或 $I^2C$/SMBus 从接口可实现定制配置：
  - VID 和 PID
  - 端口定制
  - 制造商和产品字符串（非通过 OTP ROM）
  - 序列号（非通过 OTP ROM）
- 可使用端子选择或 EEPROM 或 $I^2C$/SMBus 从接口选择应用特性
- 提供 128 位通用唯一标识符 (UUID)
- 支持通过 USB 2.0 上行端口进行板载和系统内 OTP/EEPROM 编程
- 单个时钟输入、24MHz 晶体或晶振
- 无特殊驱动程序要求；可与任一支持 USB 堆叠的操作系统无缝工作
- 48 引脚 HTQFP 封装 (PHP)

## 2 应用

- 汽车
- 计算机系统
- 扩展坞
- 监视器
- 机顶盒

## 3 说明

TUSB4020BI-Q1 是一款双端口 USB 2.0 集线器。该器件可在上行端口上提供高速/全速 USB 连接，在两个下行端口上提供高速、全速或者低速 USB 连接。当上行端口被连接至一个支持高速和全速/低速连接的电气环境中时，下行端口上的高速和全速/低速 USB 连接被启用。当上行端口被连接到一个只支持全速/低速连接的电气环境中时，下行端口上的高速连接被禁用。

TUSB4020BI-Q1 支持每端口或者成组电源开关和过流保护。

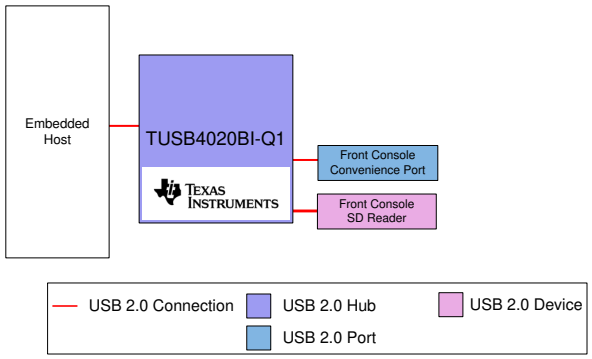
按照 USB 主机的要求，一个端口电源单独控制集线器开关为每个下行端口上电或者断电。同样地，当一个端口电源单独控制集线器感测到一个过流事件时，它只关闭到受影响的下行端口的电源。

当需要为任一端口供电时，一个成组集线器开关打开到其所有下行端口的电源。只有当所有端口处于电源可被移除的状态时，到下行端口的电源才可被关闭。同样，当一个成组集线器感测到一个过流事件时，将关闭所有下行端口的电源。

**器件信息**(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TUSB4020BI-Q1 | HTQFP (48) | 7.00mm × 7.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




**方框图**

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision A (February 2021) to Revision B (December 2021)** **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- 删除了第 4 页、第 11 页、第 12 页和第 31 页上的晶体 *1M 反馈电阻器* 要求.....1
- Corrected the default register setting for the *Register offset 9h* .....19

**Changes from Revision * (July 2015) to Revision A (February 2021)** **Page**

- 向特性列表中添加了 AEQ-Q100 器件温度等级 3 要点.....1
- From: SMBus slave address bits 2 and 3 are always 1 for TUSB4020BI-Q1 To: SMBus slave address bit 3 is always 1 for TUSB4020BI-Q1.....4

## 5 说明（续）

TUSB4020BI-Q1 能够为包括电池充电支持在内的一些特性提供引脚设置配置，还能够通过 OTP ROM、$I^2C$ EEPROM 或 $I^2C$/SMBus 受控接口为 PID、VID、自定义端口和物理层配置提供定制服务。使用 $I^2C$ EEPROM 或 $I^2C$/SMBus 受控接口时，还可以提供定制字串支持。

该器件采用 48 引脚 HTQFP 封装，专用于在 -40°C 到 85°C 的工业温度范围内工作。

# 6 Pin Configuration and Functions

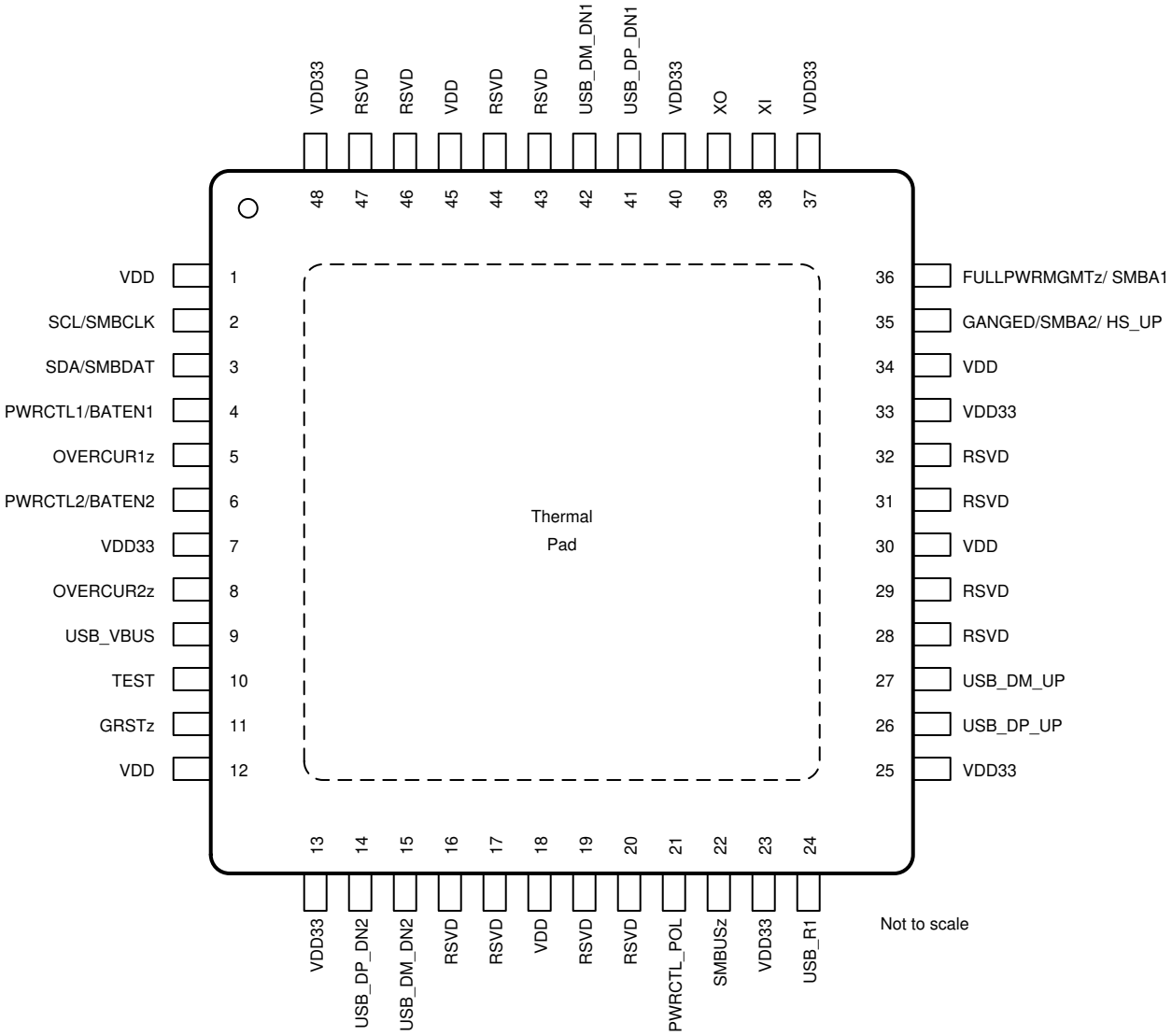



**图 6-1. PHP Package 48-Pin HTQFP Top View**

**表 6-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **CLOCK AND RESET SIGNALS** | | | |
| GRSTz | 11 | I<br>PU | Global power reset. This reset brings all of the TUSB4020BI-Q1 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional. |
| XI | 38 | I | Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. |
| XO | 39 | O | Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. |
| **USB UPSTREAM SIGNALS** | | | |
| USB_DP_UP | 26 | I/O | USB high-speed differential transceiver (positive) |
| USB_DM_UP | 27 | I/O | USB high-speed differential transceiver (negative) |
| USB_R1 | 24 | I | Precision resistor reference. A 9.53-kΩ ±1% resistor should be connected between USB_R1 and GND. |
| USB_VBUS | 9 | I | USB upstream port power monitor. The VBUS detection requires a voltage divider. The signal USB_VBUS must be connected to VBUS through a 90.9-kΩ ±1% resistor, and to ground through a 10-kΩ ±1% resistor from the signal to ground. |

**表 6-1. Pin Functions (continued)**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **USB DOWNSTREAM SIGNALS** | | | |
| USB_DP_DN1 | 41 | I/O | USB high-speed differential transceiver (positive) downstream port 1. |
| USB_DM_DN1 | 42 | I/O | USB high-speed differential transceiver (negative) downstream port 1. |
| PWRCTL1/BATEN1 | 4 | I/O<br>PD | USB port 1 power-on control for downstream power or battery charging enable. The terminal is used for control of the downstream power switch for Port 1.<br>In addition, the value of the terminal is sampled at the deassertion of reset to determine the value of the battery charging support for Port 1 as indicated in the Battery Charging Support register.<br>0 = Battery charging not supported<br>1 = Battery charging supported |
| OVERCUR1z | 5 | I<br>PU | USB DS port 1 overcurrent detection input. This terminal is used to connect the over current output of the downstream port power switch for port 1.<br>0 = An overcurrent event has occurred<br>1 = An overcurrent event has not occurred<br>If power management is enabled, the external circuitry needed should be determined by the power switch. In ganged mode, either OVERCUR1z or OVERCUR2z can be used. In ganged mode, the overcurrent will be reported as a hub event instead of a port event. |
| USB_DP_DN2 | 14 | I/O | USB high-speed differential transceiver (positive) downstream port 2. |
| USB_DM_DN2 | 15 | I/O | USB high-speed differential transceiver (negative) downstream port 2. |
| PWRCTL2/BATEN2 | 6 | I/O<br>PD | Power-on control /battery charging enable for downstream port 2. This terminal is used for control of the downstream power switch for port 2.<br>The value of the terminal is sampled at the deassertion of reset to determine the value of the battery charging support for port 2 as indicated in the Battery Charging Support register.<br>0 = Battery charging not supported<br>1 = Battery charging supported |
| OVERCUR2z | 8 | I<br>PU | Overcurrent detection for downstream port 2. This terminal is used to connect the over current output of the downstream port power switch for port 2.<br>0 = An overcurrent event has occurred<br>1 = An overcurrent event has not occurred<br>If power management is enabled, the external circuitry needed should be determined by the power switch. In ganged mode either OVERCUR1z or OVERCUR2z can be used. In ganged mode the overcurrent will be reported as a hub event instead of a port event. |
| **$I^2C$/SMBUS SIGNALS** | | | |
| SCL/SMBCLK | 2 | I/O<br>PD | $I^2C$ clock/SMBus clock. Function of terminal depends on the setting of the SMBUSz input.<br>When SMBUSz = 1, this terminal acts as the serial clock interface for an $I^2C$ EEPROM.<br>When SMBUSz = 0, this terminal acts as the serial clock interface for an SMBus host.<br>This pin must be pulled up to use the OTP ROM.<br>Can be left unconnected if external interface not implemented. |
| SDA/SMBDAT | 3 | I/O<br>PD | $I^2C$ data/SMBus data. Function of terminal depends on the setting of the SMBUSz input.<br>When SMBUSz = 1, this terminal acts as the serial data interface for an $I^2C$ EEPROM.<br>When SMBUSz = 0, this terminal acts as the serial data interface for an SMBus host.<br>This pin must be pulled up to use the OTP ROM.<br>Can be left unconnected if external interface not implemented. |

**表 6-1. Pin Functions (continued)**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **TEST AND MISCELLANEOUS SIGNALS** | | | |
| SMBUSz | 22 | I<br>PU | SMBUS mode.<br>The value of the terminal is sampled at the deassertion of reset to enable $I^2C$ or SMBus mode.<br>0 = SMBus mode selected<br>1 = $I^2C$ mode selected<br>After reset, this signal is driven low by the TUSB4020BI-Q1. Due to this behavior, it is recommended to not tie directly to supply but instead pull-up or pull-down using external resistor. |
| PWRCTL_POL | 21 | I/O<br>PD | Power control polarity.<br>The value of the terminal is sampled at the deassertion of reset to set the polarity of PWRCTL[2:1].<br>0 = PWRCTL polarity is active high.<br>1 = PWRCTL polarity is active low.<br>After reset, this signal is driven low by the TUSB4020BI-Q1. Due to this behavior, it is recommended to not tie directly to supply but instead pull-up or pull-down using external resistor. |
| GANGED/SMBA2/<br>HS_UP | 35 | I<br>PU | Ganged operation enable/SMBus address bit 2/ high-speed status for upstream port<br>The value of the terminal is sampled at the deassertion of reset to set the power switch and over current detection mode as follows:<br>0 = Individual power control supported when power switching is enabled.<br>1 = Power control gangs supported when power switching is enabled.<br>When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 2. SMBus slave address bit 3 is always 1 for the TUSB4020BI-Q1.<br>After reset, this signal indicates the high-speed USB connection status of the upstream port. A value of 1 indicates the upstream port is connected to a high-speed USB capable port.<br>Note: Individual power control must be enabled for battery charging applications. |
| FULLPWRMGMTz/<br>SMBA1 | 36 | I, PU | Full power management enable/ SMBus Address bit 1.<br>The value of the terminal is sampled at the deassertion of reset to set the power switch control follows:<br>0 = Power switching supported<br>1 = Power switching not supported<br>Full power management is the ability to control power to the downstream ports of the TUSB4020BI-Q1 using PWRCTL[2:1]/BATEN[2:1].<br>When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 1. SMBus slave address bit 3 is always 1 for the TUSB4020BI-Q1.<br>Can be left unconnected if full power management and SMBus are not implemented.<br>After reset, this signal is driven low by the TUSB4020BI-Q1. Due to this behavior, it is recommended to not tie directly to supply but instead pull-up or pull-down using external resistor.<br>Note: Power switching must be supported for battery charging applications. |
| RSVD | 16, 17, 19, 20, 28, 29, 31, 32, 43, 44, 46, 47 | I/O | Reserved. These pins are for internal use only and should be left unconnected on PCB. |
| TEST | 10 | I<br>PD | TEST mode enable. When this terminal is asserted high at reset enables test mode. This terminal is reserved for factory use. It is recommended to pull-down this terminal to ground. |
| **POWER AND GROUND SIGNALS** | | | |
| VDD | 1, 12, 18, 30, 34, 45 | PWR | 1.1-V power rail |
| VDD33 | 7, 13, 23, 25, 33, 37, 40, 48 | PWR | 3.3-V power rail |
| GND | PAD | — | Ground |

(1) I = input, O = output, I/O = input/output, PU = internal pullup resistor, PD = internal pulldown resistor, and PWR = power signal

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

over operating free-air temperature (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDD | Steady-state supply voltage | –0.3 | 1.4 | V |
| VDD33 | Steady-state supply voltage | –0.3 | 3.8 | V |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM) per AEC Q100-002(1) | | ±4000 | V |
| | | Charged device model (CDM) per AEQ Q100-011 | Corner pins | ±1000 | |
| | | | Other pins | ±1000 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD(1) | 1.1-V supply voltage | 0.99 | 1.1 | 1.26 | V |
| VDD33 | 3.3-V supply voltage | 3 | 3.3 | 3.6 | V |
| USB_VBUS | Voltage at USB_VBUS pin | 0 | | 1.155 | V |
| $T_A$ | Operating free-air temperature range | –40 | 25 | 85 | °C |
| $T_J$ | Operating junction temperature range | –40 | 25 | 105 | °C |

(1) A 1.05-V, 1.1-V, or 1.2-V supply may be used as long as minimum and maximum supply conditions are met.

## 7.4 Thermal Information

| THERMAL METRIC(1) | | TUSB4020BI-Q1 PHP (HTQFP) 48 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 31.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 16.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 12.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 3.3-V I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | OPERATION | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage(1) | VDD33 | | 2 | | VDD33 | V |
| $V_{IL}$ | Low-level input voltage(1) | VDD33 | | 0 | | 0.8 | V |
| $V_I$ | Input voltage | | | 0 | | VDD33 | V |
| $V_O$ | Output voltage(2) | | | 0 | | VDD33 | V |
| $t_t$ | Input transition time ($t_{rise}$ and $t_{fall}$) | | | 0 | | 25 | ns |
| $V_{hys}$ | Input hysteresis(3) | | | | | 0.13 × VDD33 | V |
| $V_{OH}$ | High-level output voltage | VDD33 | $I_{OH}$ = –4 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | VDD33 | $I_{OL}$ = 4 mA | | | 0.4 | V |
| $I_{OZ}$ | High-impedance, output current(2) | VDD33 | $V_I$ = 0 to VDD33 | | | ±20 | µA |
| $I_{OZP}$ | High-impedance, output current with internal pullup or pulldown resistor(4) | VDD33 | $V_I$ = 0 to VDD33 | | | ±225 | µA |
| $I_I$ | Input current(5) | VDD33 | $V_I$ = 0 to VDD33 | | | ±15 | µA |

(1) Applies to external inputs and bidirectional buffers
(2) Applies to external outputs and bidirectional buffers
(3) Applies to GRSTz
(4) Applies to pins with internal pullups/pulldowns
(5) Applies to external input buffers

## 7.6 Hub Input Supply Current

typical values measured at $T_A$ = 25°C

| PARAMETER | VDD33 | VDD11 | UNIT |
|---|---|---|---|
| | 3.3 V | 1.1 V | |
| **LOW-POWER MODES** | | | |
| Power-on (after reset) | 5 | 39 | mA |
| Disconnect from host | 5 | 39 | mA |
| Suspend | 5 | 39 | mA |
| **ACTIVE MODES (US STATE / DS STATE)** | | | |
| 2.0 host / 1 HS device active | 48 | 71 | mA |
| 2.0 host / 2 HS devices active | 60 | 80 | mA |

## 7.7 Power-Up Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d1}$ | VDD33 stable before VDD stable(1) | see (2) | | | ms |
| $t_{d2}$ | VDD and VDD33 stable before deassertion of GRSTz | 3 | | | ms |
| $t_{su\_io}$ | Setup for MISC inputs(3) sampled at the deassertion of GRSTz | 0.1 | | | µs |
| $t_{hd\_io}$ | Hold for MISC inputs(3) sampled at the deassertion of GRSTz. | 0.1 | | | µs |
| $t_{VDD33\_RAMP}$ | VDD33 supply ramp requirements | 0.2 | | 100 | ms |
| $t_{VDD\_RAMP}$ | VDD supply ramp requirements | 0.2 | | 100 | ms |

(1) An active reset is required if the VDD33 supply is stable before the VDD11 supply. This active Reset shall meet the 3ms power-up delay counting from both power supplies being stable to the de-assertion of GRSTz.
(2) There is no power-on relationship between VDD33 and VDD unless GRSTz is only connected to a capacitor to GND. Then VDD must be stable minimum of 10 µs before the VDD33.
(3) MISC pins sampled at deassertion of GRSTz: FULLPWRMGMTz, GANGED, PWRCTL_POL, SMBUSz, BATEN[4:1], and AUTOENz.

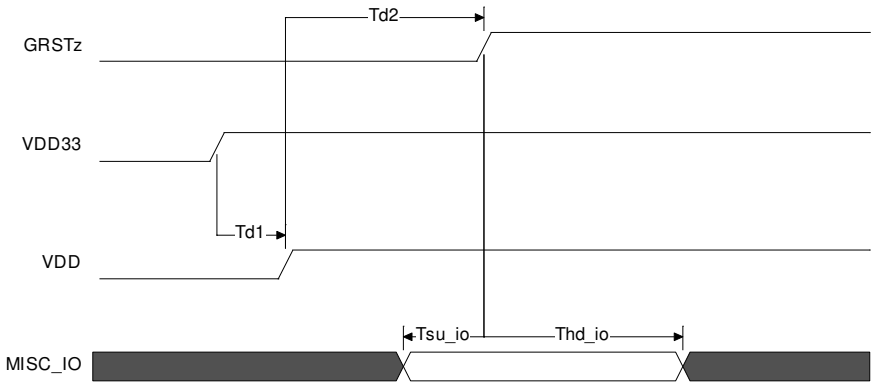


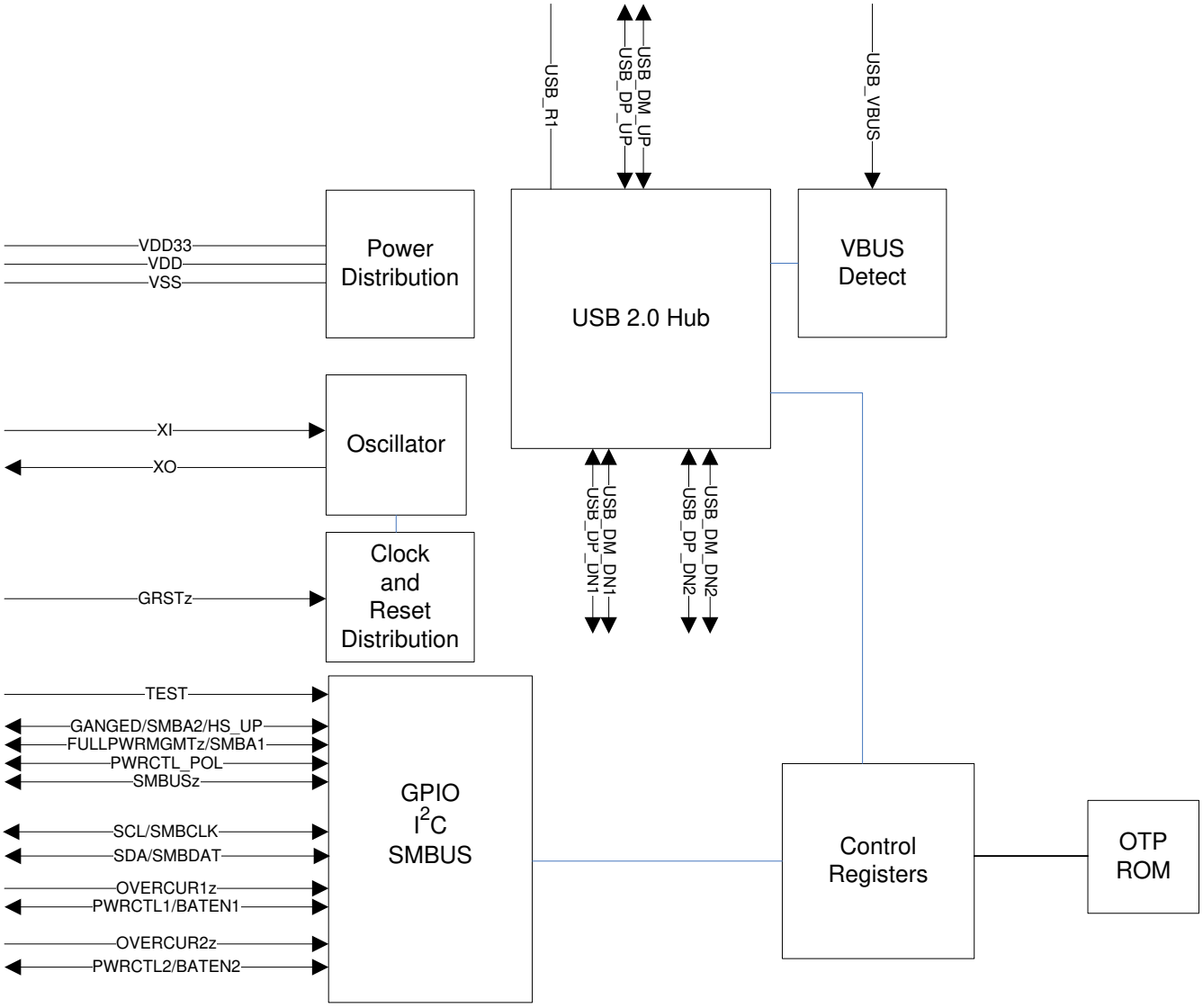

**图 7-1. Power-Up Timing Requirements**

# 8 Detailed Description

## 8.1 Overview

The TUSB4020BI-Q1 is a two-port USB 2.0 hub. It provides USB high-speed/full-speed connections on the upstream port and provides USB high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that supports high-speed and full-speed/low-speed connections, USB high-speed and full-speed/low-speed connectivity is enabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, USB high-speed connectivity are disabled on the downstream ports.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Battery Charging Features

The TUSB4020BI-Q1 provides support for battery charging. Battery charging support may be enabled on a per port basis through the REG_6h(batEn[1:0]).

Battery charging support includes both charging downstream port (CDP) and dedicated charging port (DCP) modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009.

In addition to standard DCP mode, the TUSB4020BI-Q1 provides a mode (AUTOMODE) which automatically provides support for DCP devices and devices that support custom charging indication. AUTOMODE is disabled by default. When in AUTOMODE, the port automatically switches between a divider mode and the DCP mode depending on the portable device connected. The divider mode places a fixed DC voltage on the ports DP and DM signals which allows some devices to identify the capabilities of the charger. The default divider mode indicates support for up to 5 W. The divider mode can be configured to report a high-current setting (up to 10 W) through REG_Ah(HiCurAcpModeEn). When AUTOMODE is enabled through REG_Ah(autoModeEnz), the CDP mode is not functional. CDP mode can not be used when AUTOMODE is enabled.

The battery charging mode for each port depends on the state of Reg_6h(batEn[n]), the status of the VBUS input, and the state of REG_Ah(autoModeEnz) upstream port, as identified in 表 8-1. Battery charging can also be enabled through the PWRCTL1/BATEN1 and PWRCTL2/BATEN2 pins.

**表 8-1. TUSB4020BI-Q1 Battery Charging Modes**

| batEn[n] | VBUS | autoModeEnz | BC Mode Port x (x = n + 1) |
|---|---|---|---|
| 0 | Do not care | Do not care | Do not care |
| 1 | <4 V | 0 | Automode(3) (4) |
| | | 1 | DCP(1) (2) |
| | >4 V | 1 | CDP(1) |

(1) USB device is USB Battery Charging Specification Revision 1.2 Compliant
(2) USB device is Chinese Telecommunications Industry Standard YD/T 1591-2009
(3) Auto-mode automatically selects divider-mode or DCP mode.
(4) Divider mode can be configured for high-current mode through register or OTP settings.

### 8.3.2 USB Power Management

The TUSB4020BI-Q1 can be configured for power switched applications using either per-port or ganged power-enable controls and overcurrent status inputs.

Power switch support is enabled by REG_5h(fullPwrMgmtz) and the per-port or ganged mode is configured by REG_5h(ganged). It can also be enabled through the FULLPWRMGMTz pin. Also ganged or individual control can be controlled by the GANGED pin.

The TUSB4020BI-Q1 supports both active-high and active-low power-enable controls. The PWRCTL[2:1] polarity is configured by REG_Ah(pwrctlPol). The polarity can also be configured by the PWRCTL_POL pin.

### 8.3.3 Clock Generation

The TUSB4020BI-Q1 accepts a crystal input to drive an internal oscillator or an external clock source. Keep the XI and XO traces as short as possible and away from any switching leads to minimize noise coupling.

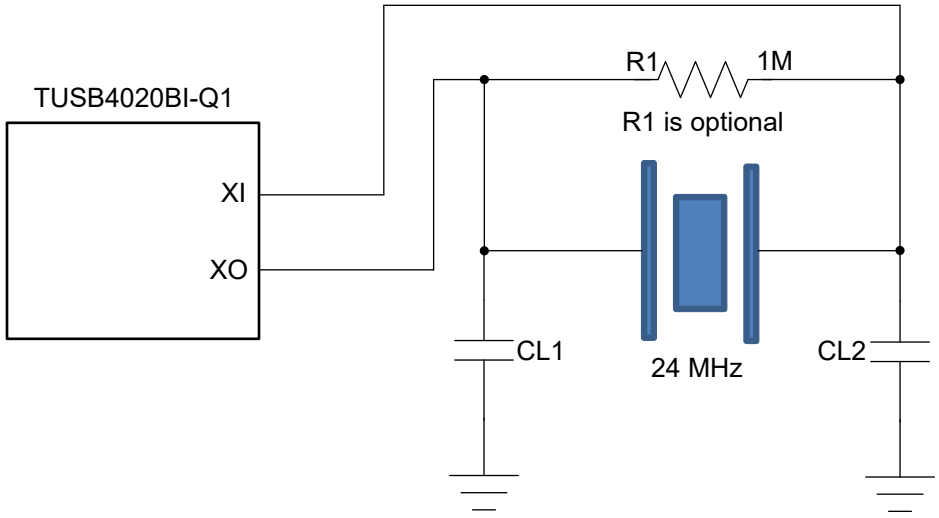



**图 8-1. TUSB4020BI-Q1 Clock**

### 8.3.4 Power-Up and Reset

The TUSB4020BI-Q1 does not have specific power sequencing requirements with respect to the VDD or VDD33 power rails. The VDD or VDD33 power rails may be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered-up must be limited to 100 hours over the projected lifetime of the device.
- Bus contention while VDD33 is powered-down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. A supply bus is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required, which is defined as the time when the power supplies are in the recommended operating range to the deassertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

## 8.4 Device Functional Modes

### 8.4.1 External Configuration Interface

The TUSB4020BI-Q1 supports a serial interface for configuration register access. The device may be configured by an attached $I^2C$ EEPROM or accessed as a slave by a SMBus-capable host controller. The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT terminals are pulled up to 3.3 V at the deassertion of reset. The mode, $I^2C$ master, or SMBus slave is determined by the state of SMBUSz terminal at reset.

## 8.5 Programming

### 8.5.1 One-Time Programmable (OTP) Configuration

The TUSB4020BI-Q1 allows device configuration through OTP non-volatile memory (OTP). The programming of the OTP is supported using vendor-defined USB device requests. For details using the OTP features, contact your TI representative.

表 8-2 provides a list features which may be configured using the OTP. The bit field section in 表 8-2 shows which features can be controlled by OTP ROM. The bits not listed in the table are not accessible by the OTP ROM.

**表 8-2. OTP Configurable Features**

| CONFIGURATION REGISTER OFFSET | BIT FIELD | DESCRIPTION |
|---|---|---|
| REG_01h | [7:0] | Vendor ID LSB |
| REG_02h | [7:0] | Vendor ID MSB |
| REG_03h | [7:0] | Product ID LSB |
| REG_04h | [7:0] | Product ID MSB |
| REG_07h | [0] | Port removable configuration for downstream ports 1. OTP configuration is inverse of rmbl[1:0], that is:<br>1 = Not removable<br>0 = Removable |
| REG_07h | [1] | Port removable configuration for downstream ports 2. OTP configuration is inverse of rmbl[1:0], that is:<br>1 = Not removable<br>0 = Removable |
| REG_0Ah | [1] | Automode enable |
| REG_0Ah | [4] | High-current divider mode enable. |
| REG_F2h | [3:1] | USB power switch power-on delay. |

### 8.5.2 $I^2C$ EEPROM Operation

The TUSB4020BI-Q1 supports a single-master, standard mode (100 kbit/s) connection to a dedicated $I^2C$ EEPROM when the $I^2C$ interface mode is enabled. In $I^2C$ mode, the TUSB4020BI-Q1 reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0.

If the value of the EEPROM contents at byte 00h equals 55h, the TUSB4020BI-Q1 loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB4020BI-Q1 exits the $I^2C$ mode and continues execution with the default values in the configuration registers. The hub will not connect on the upstream port until the configuration is completed. If the TUSB4020BI-Q1 detects an unprogrammed EEPROM (value other than 55h), it enters programming mode and a programming endpoint within the hub is enabled.

Note, the bytes located above offset Ah are optional. The requirement for data in those addresses depends on the options configured in the Device Configuration, Phy Custom Configuration, and Device Configuration 2 registers.

For details on $I^2C$ operation, refer to the UM10204 $I^2C$-bus Specification and User Manual.

### 8.5.3 SMBus Slave Operation

When the SMBus interface mode is enabled, the TUSB4020BI-Q1 supports read block and write block protocols as a slave-only SMBus device.

The TUSB4020BI-Q1 slave address is 1000 1xyz, where:

- x is the state of GANGED/SMBA2/HS_UP terminal at reset
- y is the state of FULLPWRMGMTz/SMBA1 terminal at reset
- z is the read/write bit; 1 = read access, 0 = write access.

If the TUSB4020BI-Q1 is addressed by a host using an unsupported protocol, it does not respond. The TUSB4020BI-Q1 waits indefinitely for configuration by the SMBus host and does not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements, refer to the System Management Bus Specification.

## 8.6 Register Maps

### 8.6.1 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be overwritten when the TUSB4020BI-Q1 is in $I^2C$ or SMBus mode.

**表 8-3. TUSB4020BI-Q1 Register Map**

| BYTE ADDRESS | CONTENTS | EEPROM CONFIGURABLE |
|---|---|---|
| 00h | ROM Signature Register | No |
| 01h | Vendor ID LSB | Yes |
| 02h | Vendor ID MSB | Yes |
| 03h | Product ID LSB | Yes |
| 04h | Product ID MSB | Yes |
| 05h | Device Configuration Register | Yes |
| 06h | Battery Charging Support Register | Yes |
| 07h | Device Removable Configuration Register | Yes |
| 08h | Port Used Configuration Register | Yes |
| 09h | Reserved | Yes, program to 00h |
| 0Ah | Device Configuration Register 2 | Yes |
| 0Bh to 0Fh | Reserved | |
| 10h to 1Fh | UUID Byte [15:0] | No |
| 20h to 21h | LangID Byte [1:0] | Yes, if customStrings is set |
| 22h | Serial Number String Length | Yes, if customSerNum is set |
| 23h | Manufacturer String Length | Yes, if customStrings is set |
| 24h | Product String Length | Yes, if customStrings is set |
| 25h to 2Fh | Reserved | Yes |
| 30h to 4Fh | Serial Number String Byte [31:0] | Yes, if customSerNum is set |
| 50h to 8Fh | Manufacturer String Byte [63:0] | Yes, if customStrings is set |
| 90h to CFh | Product String Byte [63:0] | Yes, if customStrings is set |
| D0 to DFh | Reserved | No |
| F0h | Additional Feature Configuration Register | Yes |
| F1h | Reserved | Yes |
| F2h | Charging Port Control Register | Yes |
| F3 to F7h | Reserved | No |
| F8h | Device Status and Command Register | No |
| F9 to FFh | Reserved | No |

### 8.6.1.1 ROM Signature Register (offset = 0h) [reset = 0h]

**图 8-2. Register Offset 0h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-4. ROM Signature Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | romSignature | R/W | 0h | ROM Signature Register. This register is used by the TUSB4020BI-Q1 in $I^2C$ mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB4020BI-Q1 aborts the EEPROM load and executes with the register defaults. |

### 8.6.1.2 Vendor ID LSB Register (offset = 1h) [reset = 51h]

**图 8-3. Register Offset 51h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-5. Vendor ID LSB Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | vendorIdLsb | R/W | 51h | Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value may be overwritten to indicate a customer vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value. |

### 8.6.1.3 Vendor ID MSB Register (offset = 2h) [reset = 4h]

**图 8-4. Register Offset 2h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-6. Vendor ID MSB Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | vendorIdMsb | R/W | 4h | Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value may be overwritten to indicate a customer vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value. |

### 8.6.1.4 Product ID LSB Register (offset = 3h) [reset = 25h]

**图 8-5. Register Offset 3h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-7. Product ID LSB Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | productIdLsb | R/W | 25h | Product ID LSB. Least significant byte of the product ID assigned by TI. The default value of this register is 25h representing the LSB of the product ID assigned by TI. The value reported in the USB 2.0 device descriptor is the value of this register bit wise XORed with 00000010b. The value may be overwritten to indicate a customer product ID.<br>This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value. |

### 8.6.1.5 Product ID MSB Register (offset = 4h) [reset = 80h]

**图 8-6. Register Offset 4h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-8. Bit Descriptions – Product ID MSB Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | productIdLsb | R/W | 80h | Product ID MSB. Most significant byte of the product ID assigned by TI; the default value of this register is 80h representing the MSB of the product ID assigned by TI. The value may be overwritten to indicate a customer product ID.<br>This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register will reflect the OTP ROM value. |

### 8.6.1.6 Device Configuration Register (offset = 5h) [reset = 1Xh]

**图 8-7. Register Offset 5h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | X | X | 0 | 0 |
| R/W | R/W | R/W | R | R/W | R/W | R/W | R |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-9. Device Configuration Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | customStrings | R/W | 1Xh | Custom strings enable. This bit controls the ability to write to the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers.<br>0 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are read only.<br>1 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers may be loaded by EEPROM or written by SMBus.<br>The default value of this bit is 0. |
| 6 | customSernum | R/W | 1Xh | Custom serial number enable. This bit controls the ability to write to the serial number registers.<br>0 = The Serial Number String Length and Serial Number String registers are read only.<br>1 = The Serial Number String Length and Serial Number String registers may be loaded by EEPROM or written by SMBus.<br>The default value of this bit is 0. |
| 5 | RSVD | R/W | 1Xh | Reserved. This bit is reserved. |
| 4 | RSVD | R | 1Xh | Reserved. This bit is reserved and returns 1 when read. |
| 3 | ganged | R/W | 1Xh | Ganged. This bit is loaded at the deassertion of reset with the value of the GANGED/SMBA2/HS_UP terminal.<br>0 = When fullPwrMgmtz = 0, each port is individually power switched and enabled by the PWRCTL[2:1]/BATEN[2:1] terminals<br>1 = When fullPwrMgmtz = 0, the power switch control for all ports is ganged and enabled by the PWRCTL1/BATEN1 terminal<br>When the TUSB4020BI-Q1 is in $I^2C$ mode, the TUSB4020BI-Q1 loads this bit from the contents of the EEPROM.<br>When the TUSB4020BI-Q1 is in SMBUS mode, the value may be overwritten by an SMBus host. |
| 2 | fullPwrMgmtz | R/W | 1Xh | Full Power Management. This bit is loaded at the deassertion of reset with the value of the FULLPWRMGMTz/SMBA1 terminal.<br>0 = Port power switching and over-current status reporting is enabled<br>1 = Port power switching and over-current status reporting is disabled<br>When the TUSB4020BI-Q1 is in $I^2C$ mode, the TUSB4020BI-Q1 loads this bit from the contents of the EEPROM.<br>When the TUSB4020BI-Q1 is in SMBUS mode, the value may be overwritten by an SMBus host. |
| 1 | RSVD | R/W | 1Xh | Reserved. This bit is reserved and should not be altered from the default. |
| 0 | RSVD | R | 1Xh | Reserved. This field is reserved and returns 0 when read. |

### 8.6.1.7 Battery Charging Support Register (offset = 6h) [reset = 0Xh]

**图 8-8. Register Offset 6h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | X | X |
| R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-10. Battery Charging Support Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:2 | RSVD | R | 0Xh | Reserved. Read only, returns 0 when read. |
| 1:0 | batEn[1:0] | R/W | 0Xh | Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features.<br>0 = The port is not enabled for battery charging support features<br>1 = The port is enabled for battery charging support features<br>Each bit corresponds directly to a downstream port, that is batEn0 corresponds to downstream port 1, and batEN1 corresponds to downstream port 2.<br>The default value for these bits are loaded at the deassertion of reset with the value of PWRCTL/BATEN[1:0].<br>When in I2C/SMBus mode the bits in this field may be overwritten by EEPROM contents or by an SMBus host. |

### 8.6.1.8 Device Removable Configuration Register (offset = 7h) [reset = 0Xh]

**图 8-9. Register Offset 7h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | X | X |
| R/W | R | R | R | R | R | R | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-11. Device Removable Configuration Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | customRmbl | R/W | 0Xh | Custom removable status. When this field is a 1, the TUSB4020BI-Q1 uses rmbl bits in this register to identify removable status for the ports. |
| 6:2 | RSVD | R | 0Xh | Reserved. Read only, returns 0 when read. Bits 3:2 are RW. They are reserved and return 0 when read. |
| 1:0 | rmbl[1:0] | R/W | 0Xh | Removable. The bits in this field indicate whether a device attached to downstream ports 2 through 1 are removable or permanently attached.<br>0 = The device attached to the port is not removable<br>1 = The device attached to the port is removable<br>Each bit corresponds directly to a downstream port n + 1, that is rmbl0 corresponds to downstream port 1, rmbl1 corresponds to downstream port 2, and so forth.<br>This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this filed reflects the inverted values of the OTP ROM non_rmb[1:0] field. |

### 8.6.1.9 Port Used Configuration Register (offset = 8h) [reset = 0h]

**图 8-10. Register Offset 8h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-12. Port Used Configuration Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | RSVD | R | 0h | Reserved. Read only. |

### 8.6.1.10 PHY Custom Configuration Register (offset = 9h) [reset = 0h]

**图 8-11. Register Offset 9h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R | R/W | R | R | R | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-13. PHY Custom Configuration Register**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | RSVD | R | 0h | Reserved. Read only, returns 0 when read. |
| 5 | RSVD | R/W | 0h | Reserved. This bit is reserved and should not be altered from the default. |
| 4:2 | RSVD | R | 0h | Reserved. Read only, returns 0 when read. |
| 1:0 | RSVD | R/W | 0h | Reserved. This field is reserved and should not be altered from the default. |

### 8.6.1.11 Device Configuration Register 2 (offset = Ah)

**图 8-12. Register Offset Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | X | 0 | 0 | 0 | 0 | 0 |
| R | RW | RW | RW | RW | RW | RW | R |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-14. Bit Descriptions – Device Configuration Register 2**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7 | RSVD | RO | | Reserved. Read only, returns 0 when read. |
| 6 | customBCfeatures | RW | | Custom Battery Charging Feature Enable. This bit controls the ability to write to the battery charging feature configuration controls.<br>0 = The HiCurAcpModeEn and AutoModeEnz bits are read only and the values are loaded from the OTP ROM.<br>1 = The HiCurAcpModeEn and AutoModeEnz bits are read/write and can be loaded by EEPROM or written by SMBus. from this register.<br>This bit may be written simultaneously with HiCurAcpModeEn and AutoModeEnz. |
| 5 | pwrctlPol | RW | | Power enable polarity. This bit is loaded at the deassertion of reset with the inverse value of the PWRCTL_POL terminal.<br>0 = PWRCTL polarity is active low<br>1 = PWRCTL polarity is active high<br>When the TUSB4020BI-Q1 is in $I^2C$ mode, the TUSB4020BI-Q1 loads this bit from the contents of the EEPROM.<br>When the TUSB4020BI-Q1 is in SMBUS mode, the value may be overwritten by an SMBus host. |
| 4 | HiCurAcpModeEn | RO/RW | | High-current ACP mode enable. This bit enables the high-current tablet charging mode when the automatic battery charging mode is enabled for downstream ports.<br>0 = High current divider mode disabled<br>1 = High current divider mode enabled<br>This bit is read only unless the customBCfeatures bit is set to 1. Otherwise the value of this bit reflects the value of the OTP ROM HiCurAcpModeEn bit. |
| 3 | RSVD | RW | | Reserved |
| 2 | dsportEcrEn | RW | | DSPort ECR enable. This bit enables full implementation of the DSPORT ECR (April 2013).<br>0 = DSPort ECR (April 2013) is enabled with the exception of changes related to the CCS bit is set upon entering U0, and changes related to avoiding or reporting compliance mode entry.<br>1 = The full DSport ECR (April 2013) is enabled. |
| 1 | autoModeEnz | RO/RW | | Automatic Mode Enable. This bit is loaded from the OTP ROM.<br>The automatic mode only applies to downstream ports with battery charging enabled when the upstream port is not connected. Under these conditions:<br>0 = Automatic mode battery charging features are enabled. Only battery charging DCP and custom BC (divider mode) is enabled.<br>1 = Automatic mode is disabled; only battery charging DCP and CDP mode is supported.<br>Note: When the upstream port is connected, battery charging CDP mode is supported on all ports when this field is one.<br>This bit is read only unless the customBCfeatures bit is set to 1. Otherwise the value of this bit reflects the value of the OTP ROM AutoModeEnz bit. |
| 0 | RSVD | RO | | Reserved. Read only, returns 0 when read. |

### 8.6.1.12 UUID Registers (offset = 10h to 1Fh)

**图 8-13. Register Offset 10h to 1Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |
| R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-15. Bit Descriptions – UUID Byte N Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:0 | uuidByte[n] | RO | | UUID byte N. The UUID returned in the Container ID descriptor. The value of this register is provided by the device and is meets the UUID requirements of Internet Engineering Task Force (IETF) RFC 4122 A UUID URN Namespace. |

### 8.6.1.13 Language ID LSB Register (offset = 20h)

**图 8-14. Register Offset 20h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-16. Bit Descriptions – Language ID LSB Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:0 | langIdLsb | RW | | Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB4020BI-Q1 only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host. |

### 8.6.1.14 Language ID MSB Register (offset = 21h)

**图 8-15. Register Offset 21h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-17. Bit Descriptions – Language ID MSB Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:0 | langIdMsb | RO/RW | | Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB4020BI-Q1 only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States.<br>When customStrings is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host. |

### 8.6.1.15 Serial Number String Length Register (offset = 22h)

**图 8-16. Register Offset 22h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-18. Bit Descriptions – Serial Number String Length Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:6 | RSVD | RO | | Reserved. Read only, returns 0 when read. |
| 5:0 | serNumStringLen | RO/RW | | Serial number string length. The string length in bytes for the serial number string. The default value is 18h indicating that a 24-byte serial number string is supported. The maximum string length is 32 bytes.<br>When customSernum is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host.<br>When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers. |

### 8.6.1.16 Manufacturer String Length Register (offset = 23h)

**图 8-17. Register Offset 23h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-19. Bit Descriptions – Manufacturer String Length Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7 | RSVD | RO | | Reserved. Read only, returns 0 when read. |
| 6:0 | mfgStringLen | RO/RW | | Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes.<br>When customStrings is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host.<br>When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers. |

### 8.6.1.17 Product String Length Register (offset = 24h)

**图 8-18. Register Offset 24h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-20. Bit Descriptions – Product String Length Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7 | RSVD | RO | | Reserved. Read only, returns 0 when read. |
| 6:0 | prodStringLen | RO/RW | | Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes.<br>When customStrings is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host.<br>When the field is non-zero, a product string of prodStringLen bytes is returned at string index 2 from the data contained in the Product String registers. |

### 8.6.1.18 Serial Number Registers (offset = 30h to 4Fh)

**图 8-19. Register Offset 30h to 4Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | x | x | x | x | x | x |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-21. Bit Descriptions – Serial Number Registers**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:0 | serialNumber[n] | RO/RW | | Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is set by TI. When customSernum is 1, these registers may be overwritten by EEPROM contents or by an SMBus host. |

### 8.6.1.19 Manufacturer String Registers (offset = 50h to 8Fh)

**图 8-20. Register Offset 50h to 8Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-22. Bit Descriptions – Manufacturer String Registers**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:0 | mfgStringByte[n] | RO/RW | | Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen.<br>The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0. |

### 8.6.1.20 Product String Registers (offset = 90h to CFh)

**图 8-21. Register Offset 90h to CFh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-23. Bit Descriptions – Product String Byte N Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:0 | prodStringByte[n] | RW | | Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen.<br>The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0. |

### 8.6.1.21 Additional Feature Configuration Register (offset = F0h)

**图 8-22. Register Offset F0h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-24. Bit Descriptions – Additional Feature Configuration Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:1 | RSVD | RO | | Reserved. Read only, returns 0 when read. |
| 0 | RSVD | RW | | Reserved<br>This bit is loaded at the deassertion of reset with the value of the SCL/SMBCLK terminal. |

### 8.6.1.22 Charging Port Control Register (offset = F2h)

**图 8-23. Register Offset F2h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R | R | R | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-25. Bit Descriptions – Charging Port Control Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:4 | RSVD | RO | | Reserved. Read only, returns 0 when read. |
| 3:1 | pwronTime | RW | | Power-On Delay Time. When dsportEcrEn is set, this field sets the delay time from the removal disable of PWRCTL to the enable of PWRCTL when transitioning battery charging modes. For example, when disabling the power on a transition from custom charging mode to Dedicated Charging Port Mode. The nominal timing is defined as follows:<br>TPWRON_EN = (pwronTime + 1) × 200 ms (1)<br>These registers may be overwritten by EEPROM contents or by an SMBus host. |
| 0 | RSVD | RW | | Reserved. This bit is reserved and should not be altered from the default. |

### 8.6.1.23 Device Status and Command Register (offset = F8h)

**图 8-24. Register Offset F8h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R | R | R | R | R | RSU | RCU |

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

**表 8-26. Bit Descriptions – Device Status and Command Register**

| Bit | Field Name | Access | Reset | Description |
|---|---|---|---|---|
| 7:2 | RSVD | R | | Reserved. Read only, returns 0 when read. |
| 1 | smbusRst | RSU | | SMBus interface reset. This bit loads the registers back to their GRSTz values.<br>This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect. |
| 0 | cfgActive | RCU | | Configuration active. This bit indicates that configuration of the TUSB4020BI-Q1 is currently active. The bit is set by hardware when the device enters the $I^2C$ or SMBus mode. The TUSB4020BI-Q1 will not connect on the upstream port while this bit is 1. When in the SMBus mode, this bit must be cleared by the SMBus host to exit the configuration mode and allow the upstream port to connect.<br>The bit is cleared by a writing 1. A write of 0 has no effect. |

# 9 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 9.1 Application Information

The TUSB4020BI-Q1 is a two-port USB 2.0 hub. It provides USB high-speed/full-speed connections on the upstream port and provides USB high-speed, full-speed, or low-speed connections on the downstream port. The TUSB4020BI-Q1 can be used in any application that needs additional USB compliant ports. For example, a specific notebook may only have two downstream USB ports. By using the TUSB4020BI-Q1, the notebook can increase the downstream port count to three.

**图 9-1. Discrete USB Hub Product**

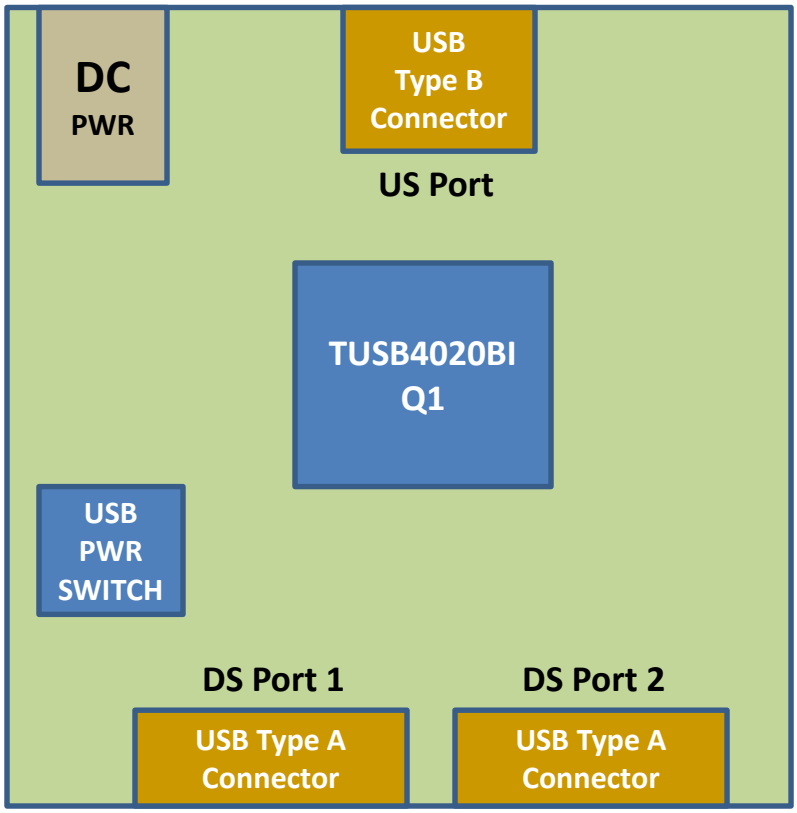



**图 9-2. Discrete USB Hub Product**

### 9.1.1 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12 to 24 pF and frequency stability rating of ±100 PPM or better. To ensure proper startup oscillation condition, TI recommends a maximum crystal equivalent series resistance (ESR) of 50 Ω. A parallel load capacitor should be used if a crystal source is used. The exact load capacitance value used depends on the crystal vendor. Refer to application note *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* for details on how to determine the load capacitance value.

### 9.1.2 Input Clock Requirements

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak-to-peak jitter. XI should be tied to the 1.8-V clock source and XO should be left floating.

## 9.2 Typical Applications

A common application for the TUSB4020BI-Q1 is as a self-powered standalone USB hub product. The product is powered by an external 5-V DC power adapter. In this application using a USB cable, TUSB4020BI-Q1 device's upstream port is plugged into a USB host controller. The downstream ports of the TUSB4020BI-Q1 are exposed to users for connecting USB hard drives, camera, flash drive, and so forth.

### 9.2.1 Upstream Port Implementation

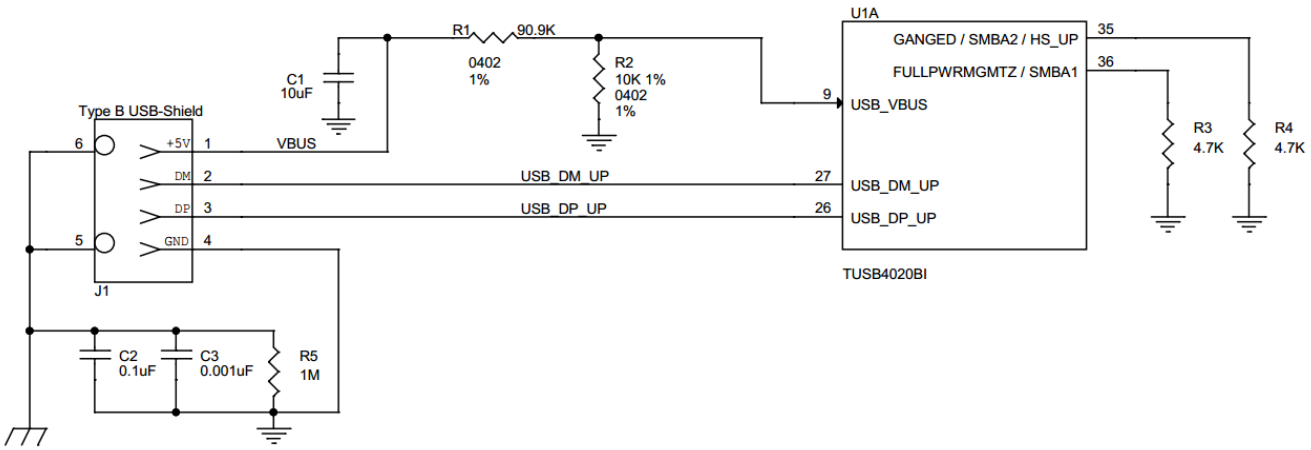



**图 9-3. Upstream Port Implementation Schematic**

#### *9.2.1.1 Design Requirements*

**表 9-1. Input Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| VDD supply | 1.1 V |
| VDD33 supply | 3.3 V |
| Upstream port USB support (HS, FS) | HS, FS |
| Downstream port 1 USB support (HS, FS, LS) | HS, FS, LS |
| Downstream port 2 USB support (HS, FS, LS) | HS, FS, LS |
| Number of removable downstream ports | 2 |
| Number of non-removable downstream ports | 0 |
| Full power management of downstream ports | Yes (FULLPWRMGMTZ = 0) |
| Individual control of downstream port power switch | Yes (GANGED = 0) |
| Power switch enable polarity | Active high (PWRCTL_POL = 0) |
| Battery charge support for downstream port 1 | Yes |
| Battery charge support for downstream port 2 | Yes |
| $I^2C$ EEPROM support | No |
| 24-MHz clock source | Crystal |

### 9.2.1.2 Detailed Design Procedure

The upstream of the TUSB4020BI-Q1 is connected to a USB2 type B connector. This particular example has GANGED terminal and FULLPWRMGMTZ terminal pulled low, which results in individual power support each downstream port. The VBUS signal from the USB2 type B connector is fed through a voltage divider. The purpose of the voltage divider is to make sure the level meets USB_VBUS input requirements.

### 9.2.1.3 Application Curves

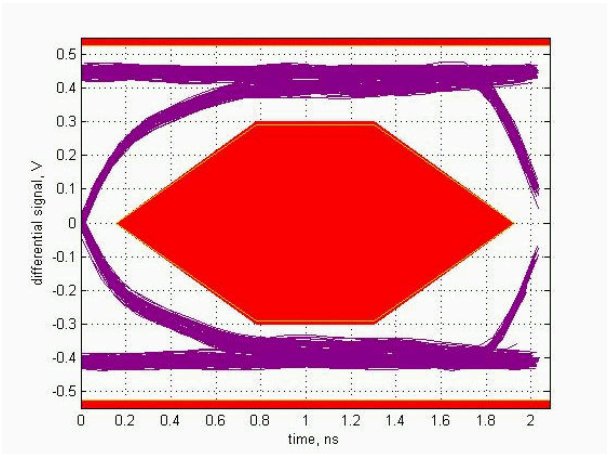



**图 9-4. HighSpeed TX Eye for Downstream Port 1**

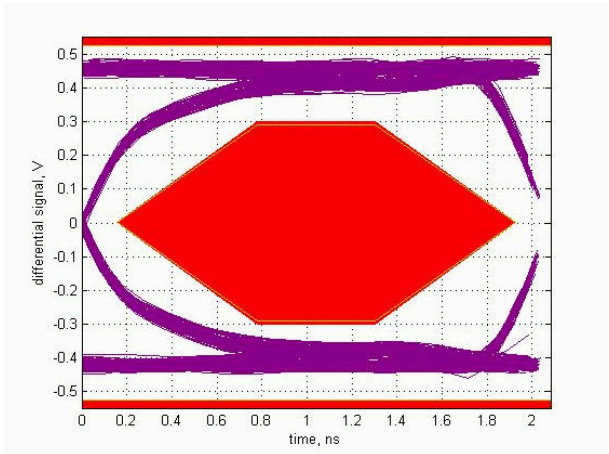



**图 9-5. HighSpeed TX Eye for Downstream Port 2**

### 9.2.2 Downstream Port 1 Implementation

The downstream port 1 of the TUSB4020BI-Q1 is connected to a USB2 type A connector. With BATEN1 terminal pulled up, battery charge support is enabled for port 1. If battery charge support is not needed, then the pullup resistor on BATEN1 should be uninstalled. The PWRCTL_POL is pulled-down, which results in active-high power enable (PWRCTL1 and PWRCTL2) for a USB VBUS power switch.

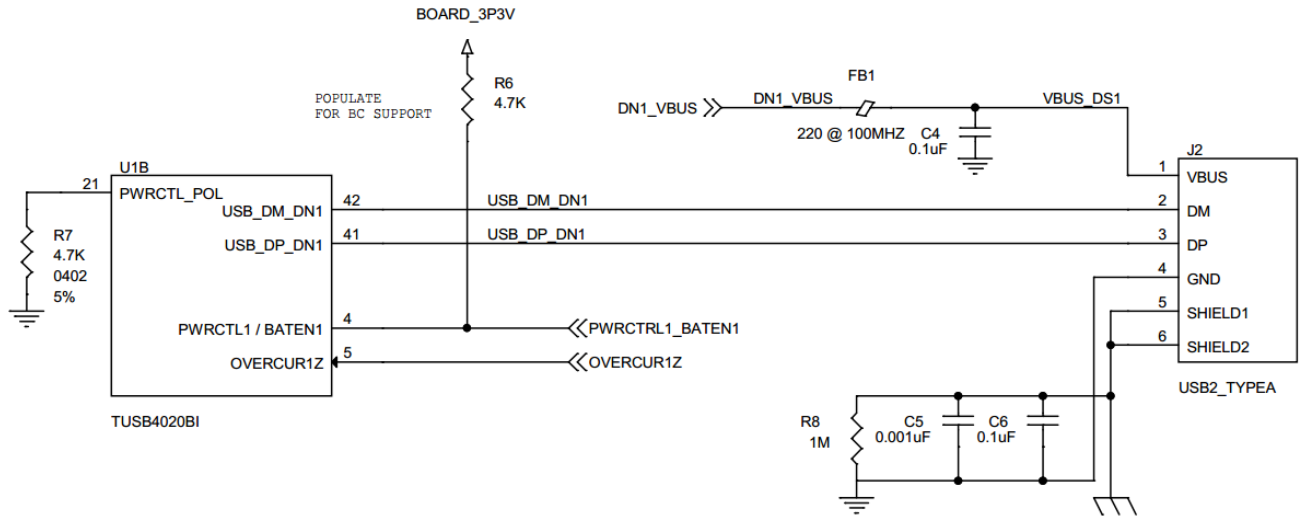



**图 9-6. Downstream Port 1 Implementation Schematic**

### 9.2.3 Downstream Port 2 Implementation

The downstream port 2 of the TUSB4020BI-Q1 is connected to a USB2 type A connector. With BATEN2 terminal pulled up, battery charge support is enabled for port 2. If battery charge support is not needed, then the pullup resistor on BATEN2 should be uninstalled.

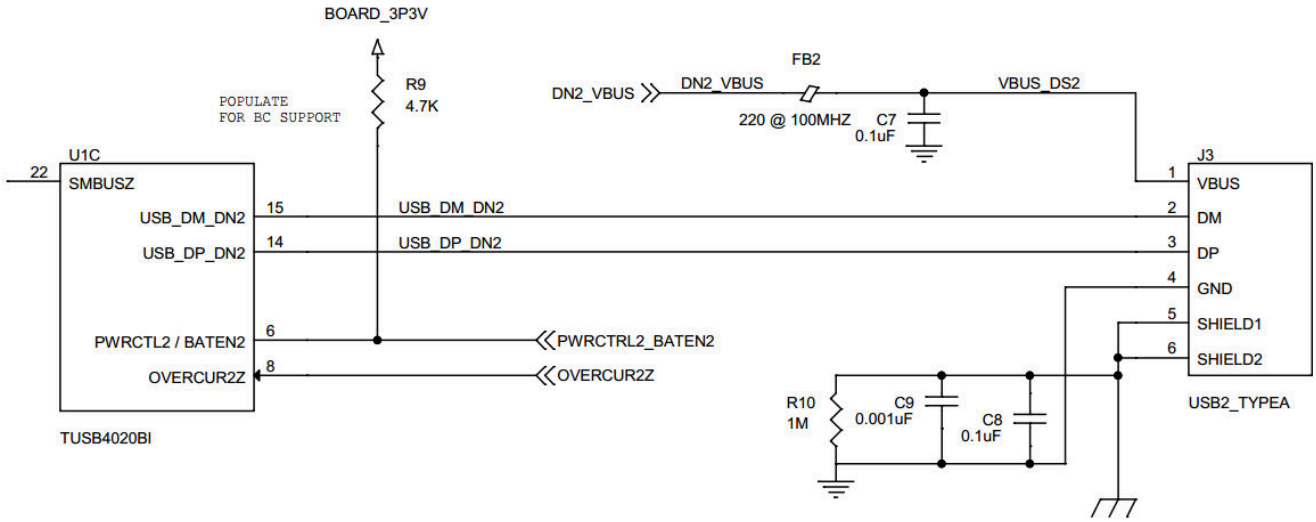



**图 9-7. Downstream Port 2 Implementation Schematic**

### 9.2.4 VBUS Power Switch Implementation

This particular example uses the TI TPS2561 dual-channel precision adjustable current-limited power switch. For details on this power switch or other power switches available from TI, refer to www.ti.com.

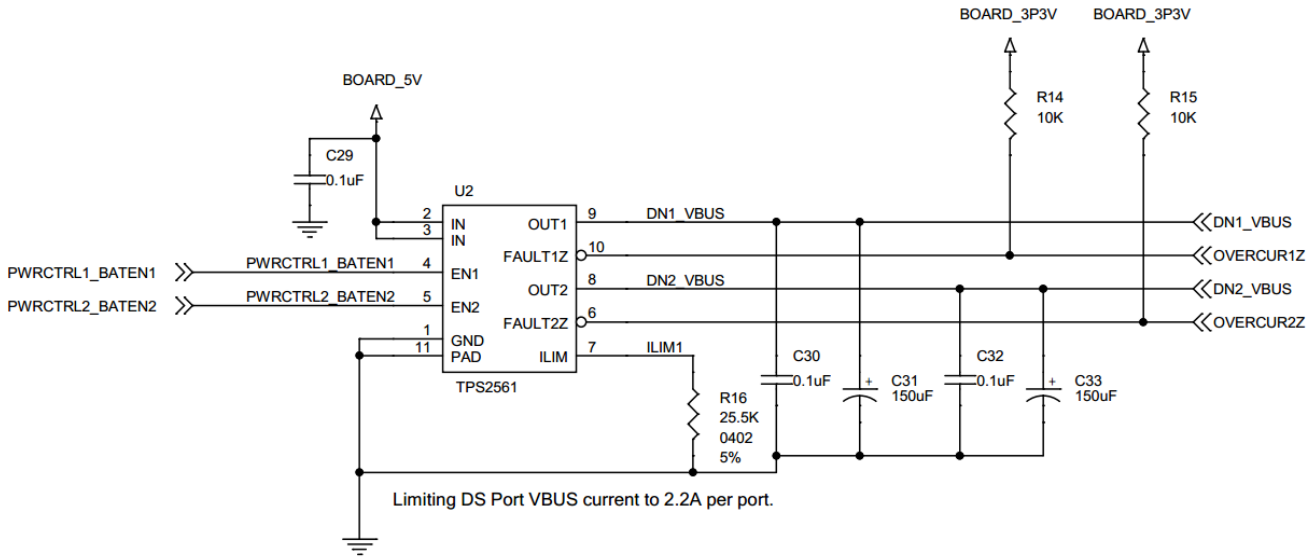



**图 9-8. Power Switch Implementation Schematic**

### 9.2.5 Clock, Reset, and Miscellaneous

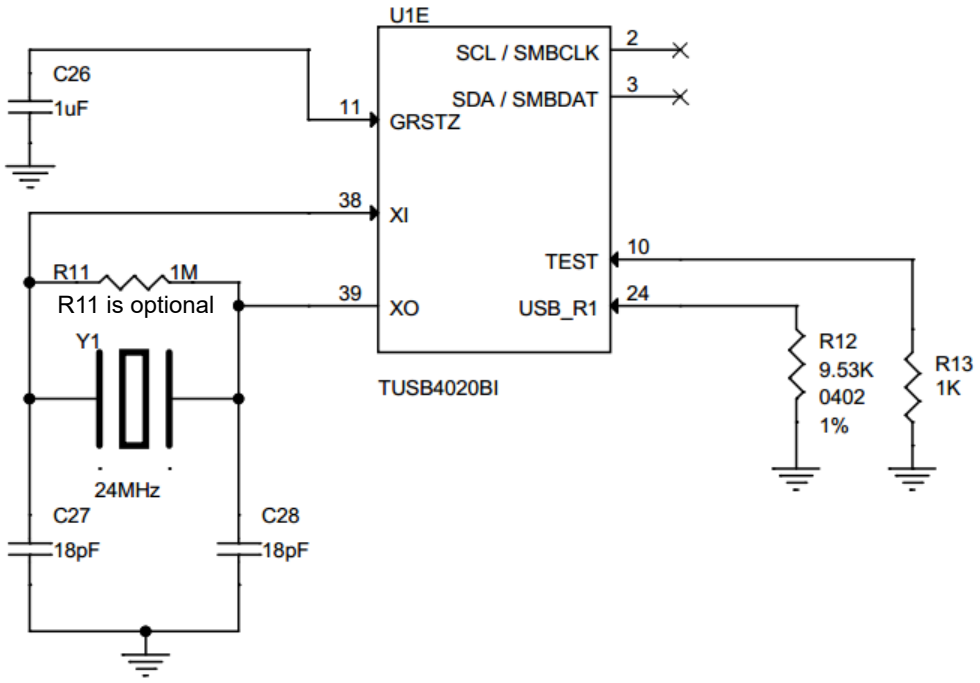



**图 9-9. Clock, Reset, and Miscellaneous Schematic**

### 9.2.6 Power Implementation

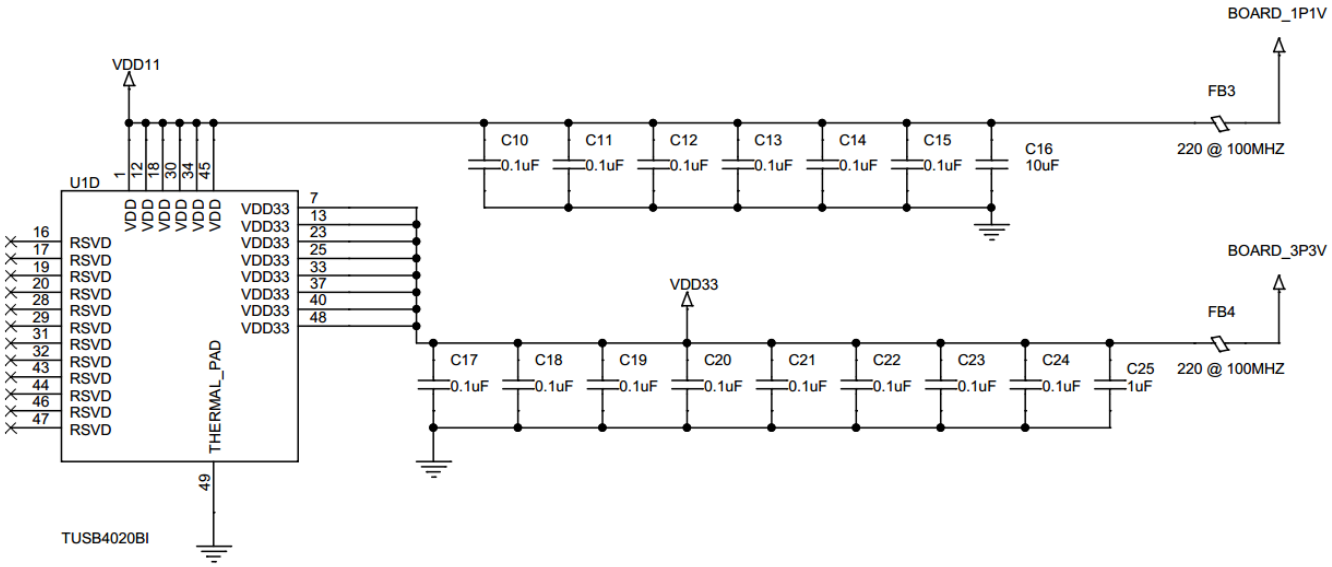



**图 9-10. Power Implementation Schematic**

# 10 Power Supply Recommendations

## 10.1 Power Supply

$V_{DD}$ should be implemented as a single power plane, as should $V_{DD33}$.

- The $V_{DD}$ terminals of the TUSB4020BI-Q1 supply 1.1-V (nominal) power to the core of the TUSB4020BI-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the core power rail can affect the voltage provided to the device due to the high current draw on the power rail. The output of the core voltage regulator may need to be adjusted to account for this or a ferrite bead with low DC resistance (less than 0.05 Ω) can be selected.
- The $V_{DD33}$ terminals of the TUSB4020BI-Q1 supply 3.3-V power rail to the I/O of the TUSB4020BI-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10-µF capacitor or 1-µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB4020BI-Q1 power pins as possible with an optimal grouping of two of differing values per pin.

## 10.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5 V and at least 500 mA per port. Downstream port power switches can be controlled by the TUSB4020BI-Q1 signals. It is possible to leave the downstream port power always enabled.
- Each downstream port's VBUS requires a large bulk low-ESR capacitor of 22 µF or larger to limit in-rush current.
- TI recommends ferrite beads on the VBUS pins of the downstream USB port connections for both ESD and EMI reasons. A 0.1-µF capacitor on the USB connector side of the ferrite provides a low-impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

## 10.3 Ground

TI recommends to use only one board ground plane in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB4020BI-Q1 and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is only implemented near the USB port connectors on a different plane for EMI and ESD purposes.

# 11 Layout

## 11.1 Layout Guidelines

### 11.1.1 Placement

1. A 9.53-kΩ ±1% resistor connected to terminal USB_R1 should be placed as close as possible to the TUSB4020BI-Q1.
2. A 0.1-µF capacitor should be placed as close as possible on each $V_{DD}$ and $V_{DD33}$ power pin.
3. The ESD and EMI protection devices (if used) should also be placed as possible to the USB connector.
4. If a crystal is used, it must be placed as close as possible to the TUSB4020BI-Q1 device's XI and XO terminals.
5. Place voltage regulators as far away as possible from the TUSB4020BI-Q1, crystal, and differential pairs.
6. In general, the large bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators.

### 11.1.2 Package Specific

1. The TUSB4020BI-Q1 package has a 0.5-mm pin pitch.
2. The TUSB4020BI-Q1 package has a 3.6-mm × 3.6-mm thermal pad. This thermal pad must be connected to ground through a system of vias.
3. All vias under device, except for those connected to thermal pad, should be solder masked to avoid potential issues with thermal pad layouts.

### 11.1.3 Differential Pairs

This section describes the layout recommendations for all of the TUSB4020BI-Q1 differential pairs: USB_DP_XX, USB_DM_XX.

- Must be designed with a differential impedance of 90 Ω ±10%.
- To minimize crosstalk, TI recommends to keep high-speed signals away from each other. Each pair should be separated by at least 5× the signal trace width. Separating with ground as depicted in the layout example also helps minimize crosstalk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- Adding test points causes impedance discontinuity, and therefore, negatively impacts signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
- Avoid 90° turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥135°. Taking this action minimizes any length mismatch caused by the bends, and therefore, minimizes the impact bends have on EMI.
- Minimize the trace lengths of the differential pair traces. Eight inches is the maximum recommended trace length for USB 2.0 differential-pair signals. Longer trace lengths require very careful routing to assure proper signal integrity.
- Match the etch lengths of the differential pair traces (that is DP and DM). The USB 2.0 differential pairs should not exceed 50-mils relative trace length difference.
- Minimize the use of vias in the differential-pair paths as much as possible. If this is not practical, ensure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB4020BI-Q1 device.
- Do not place power fuses across the differential-pair traces.

## 11.2 Layout Example

图 11-1 shows an example layout of the upstream port to a USB3 Type B connector. The routing to a USB2 Type B connector will be similar.

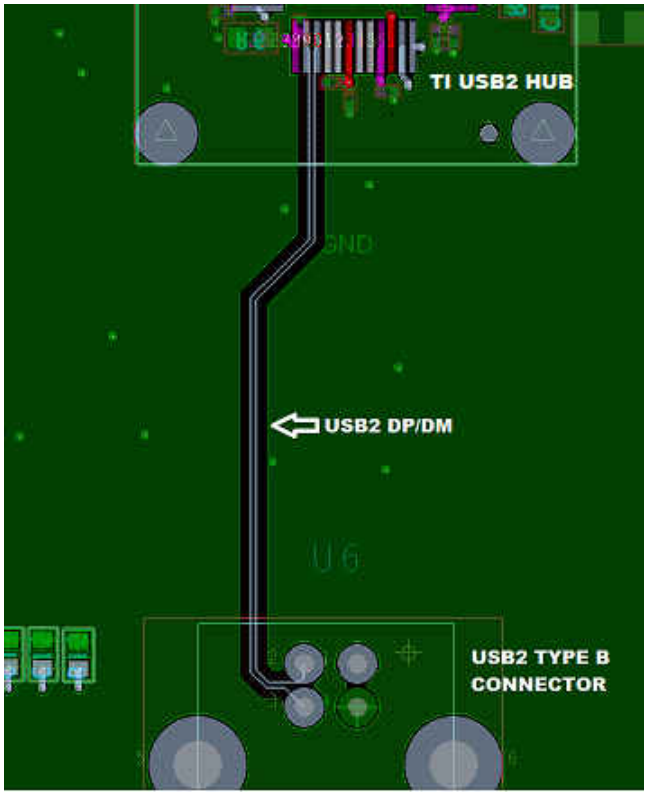



**图 11-1. Upstream Port**

图 11-2 shows an example layout of the Downstream Port to a USB3 Type A connector. The routing to a USB2 Type A connector will be similar.

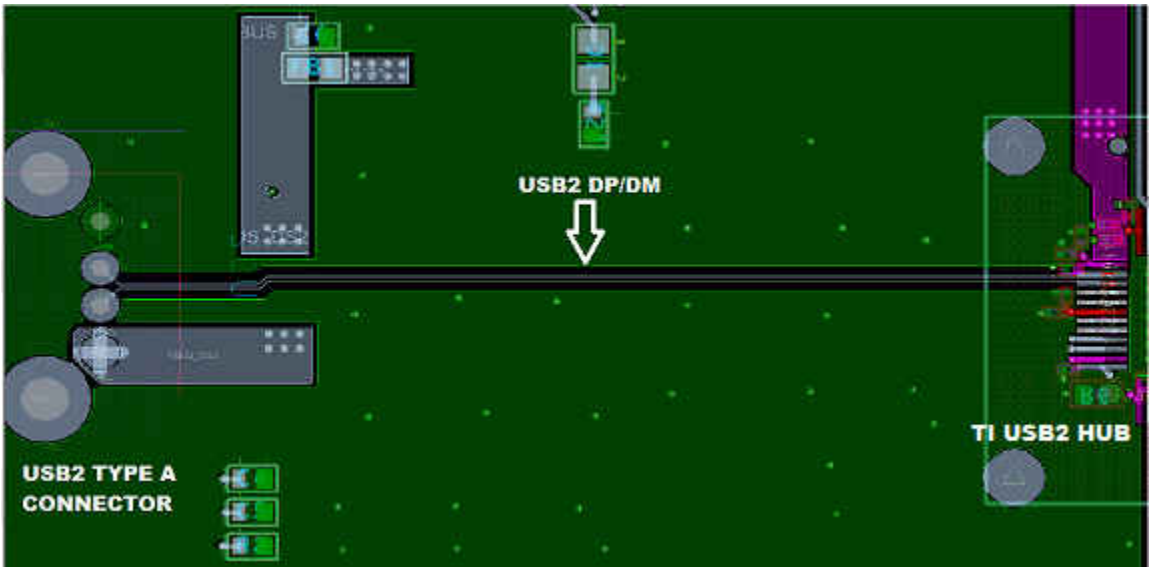



**图 11-2. Downstream Port**

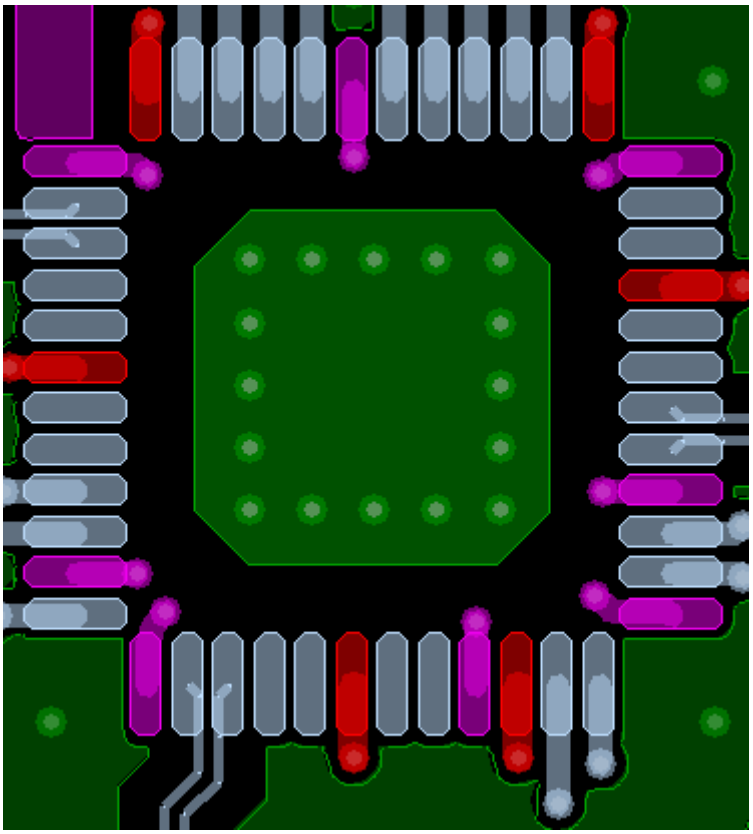


**图 11-3. Thermal Pad**

# 12 Device and Documentation Support

## 12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TUSB4020BIPHPQ1 | ACTIVE | HTQFP | PHP | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T4020BIQ1 | Samples |
| TUSB4020BIPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T4020BIQ1 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF TUSB4020BI-Q1 :**

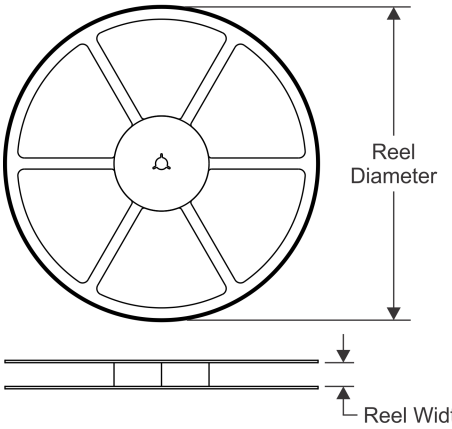
- Catalog : TUSB4020BI

NOTE: Qualified Version Definitions:

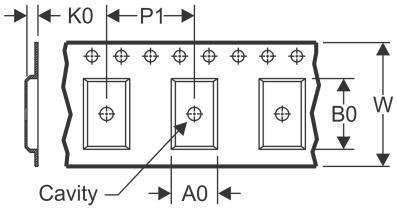
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

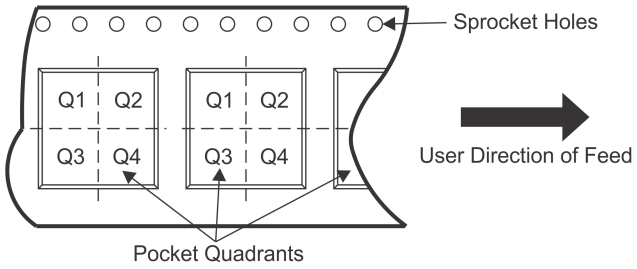



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

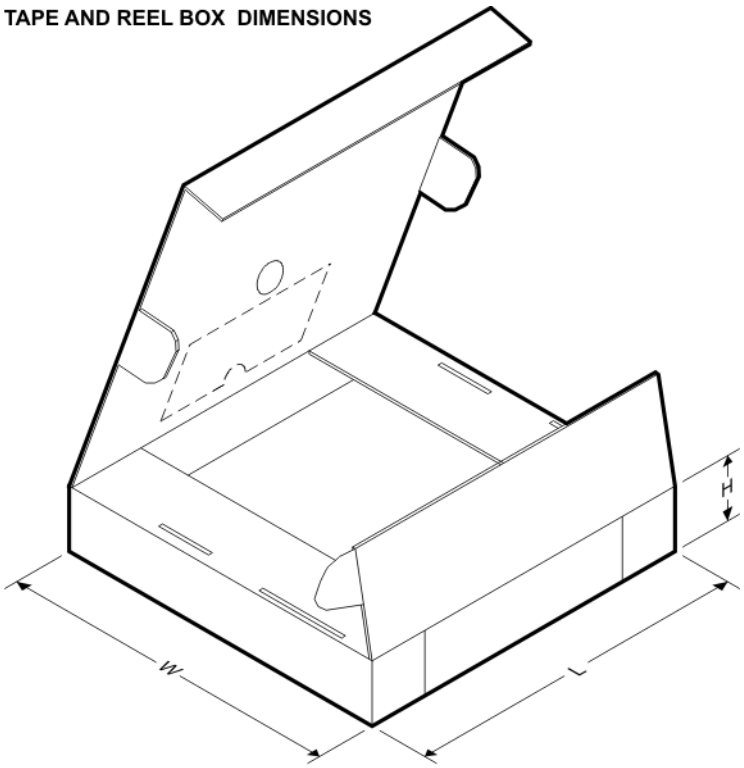
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TUSB4020BIPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

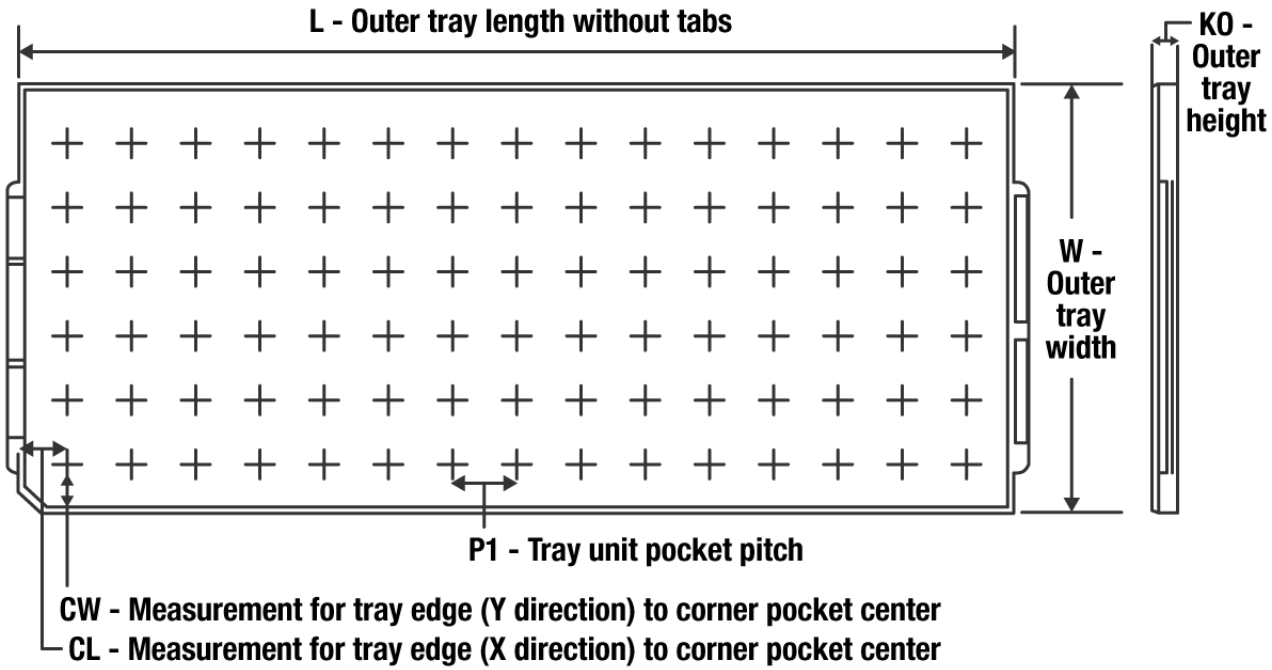
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TUSB4020BIPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TUSB4020BIPHPQ1 | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |

# GENERIC PACKAGE VIEW

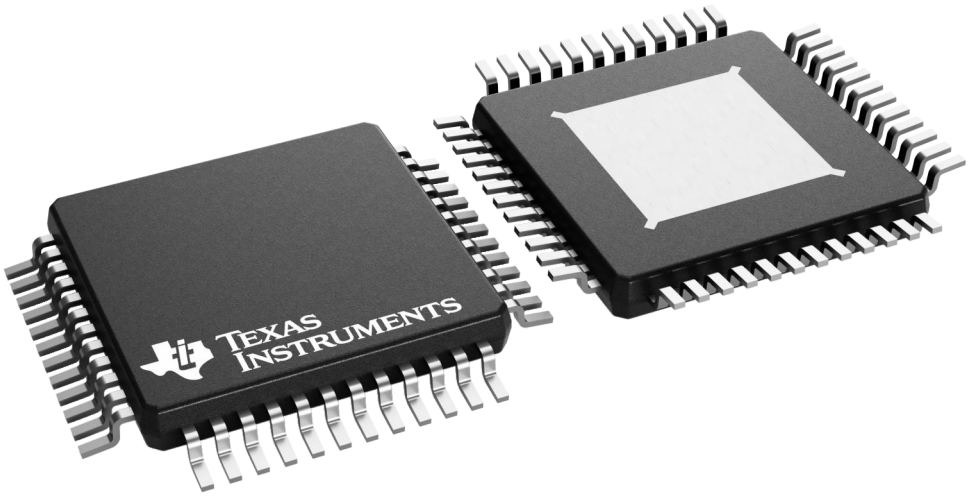
## PHP 48

## TQFP - 1.2 mm max height

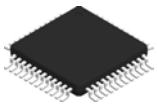
**7 x 7, 0.5 mm pitch**

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



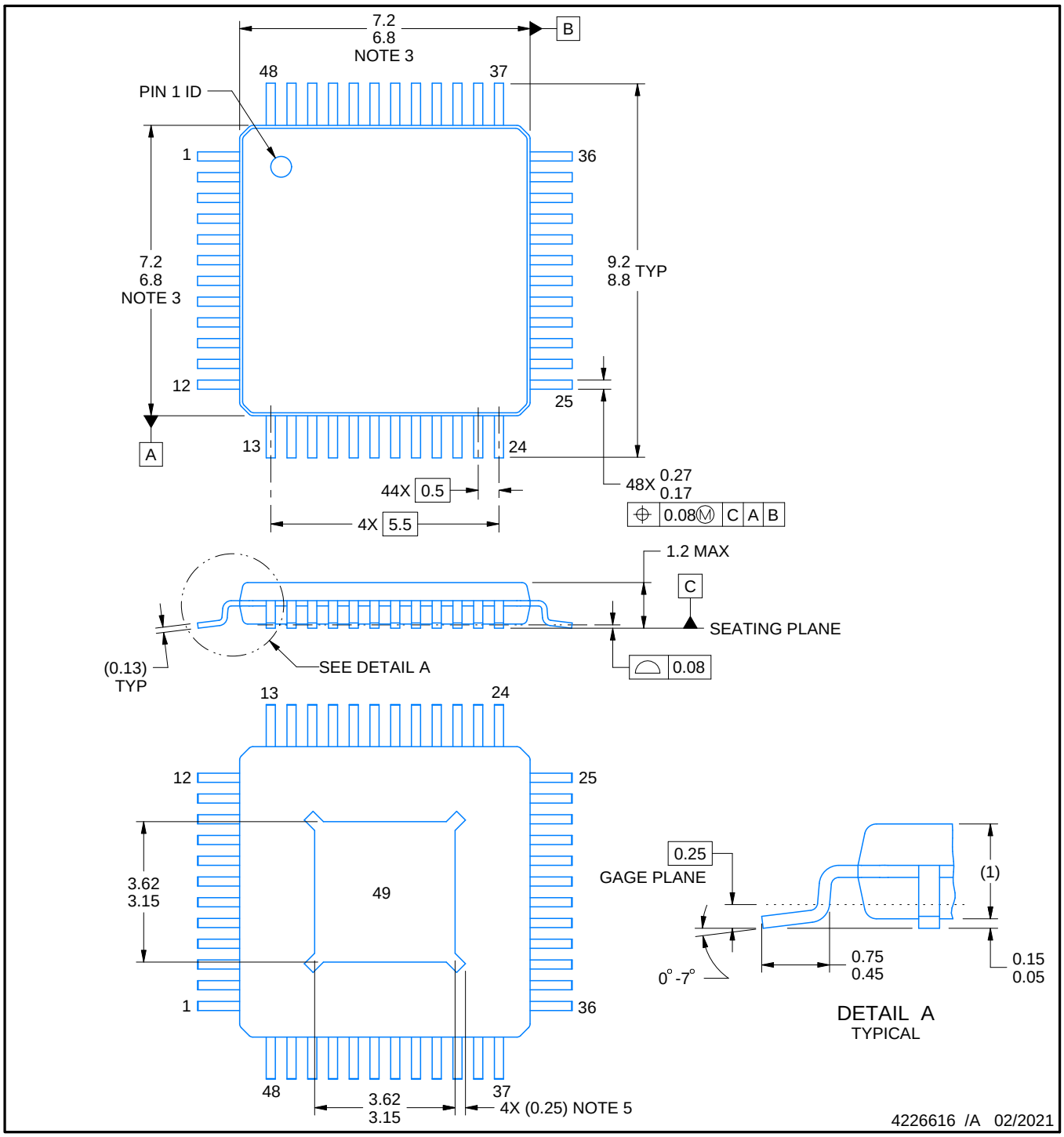

4226443/A



# PACKAGE OUTLINE

## PHP0048E

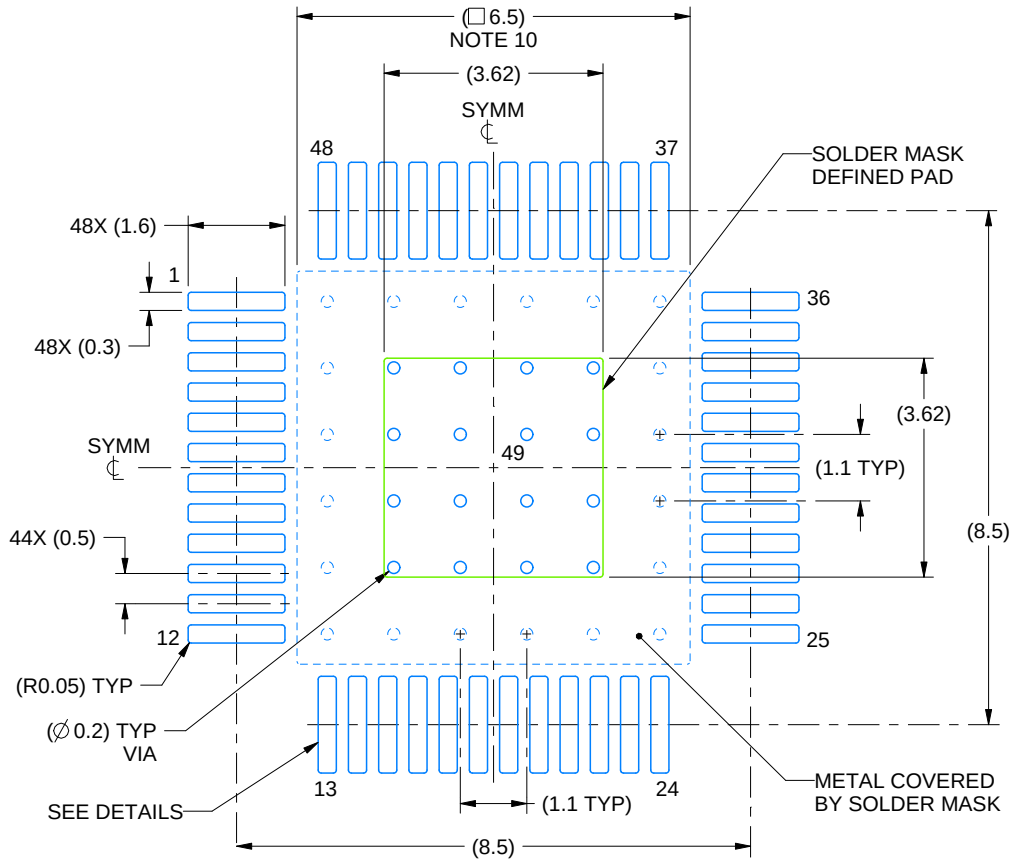
## PowerPAD™ HTQFP - 1.2 mm max height



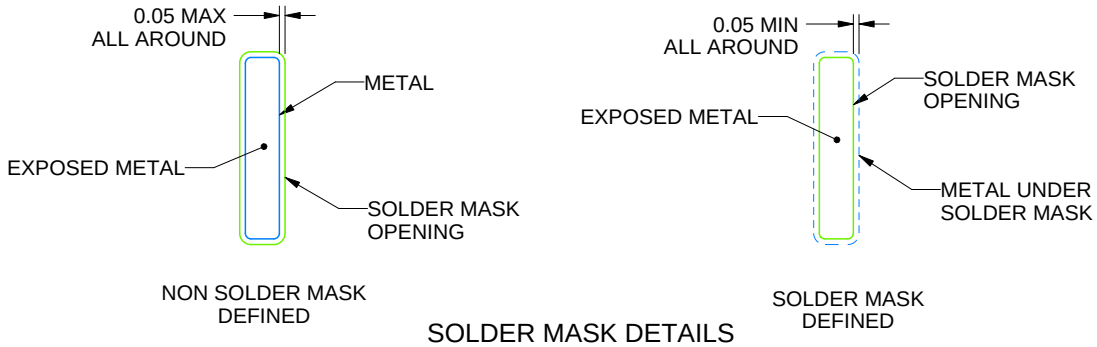

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

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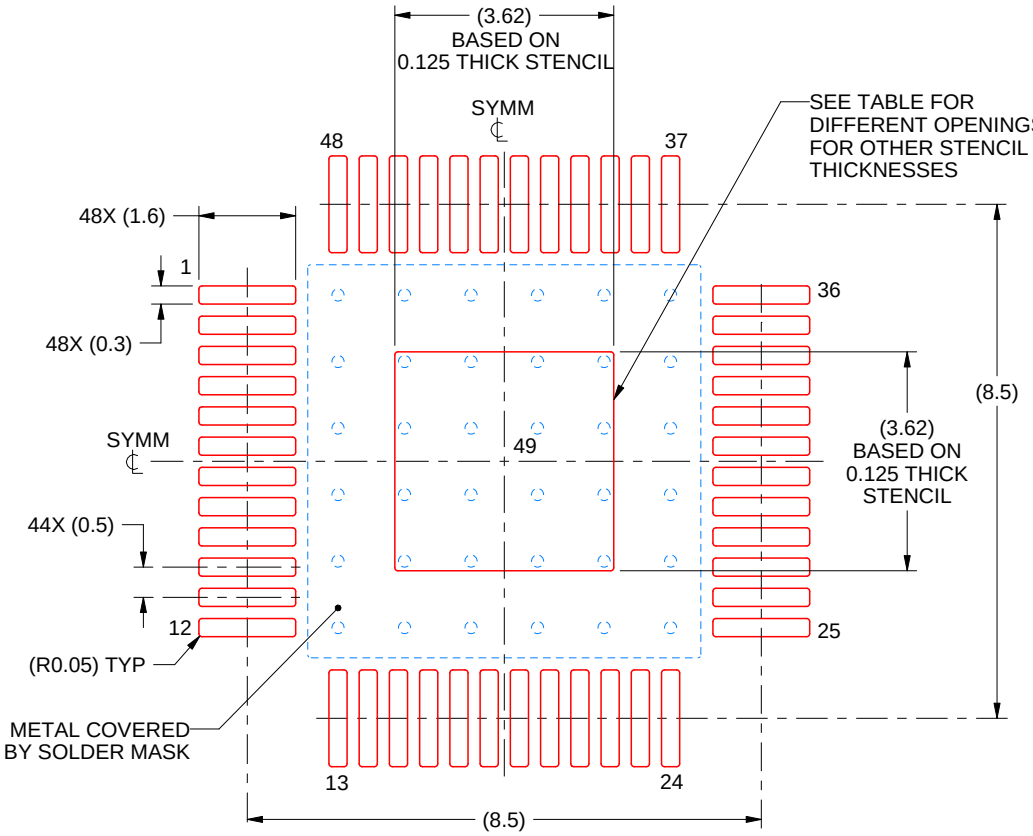
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 4.05 X 4.05 |
| 0.125 | 3.62 x 3.62 (SHOWN) |
| 0.150 | 3.30 x 3.30 |
| 0.175 | 3.06 x 3.06 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# 重要声明和免责声明

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