

CDx4HC86 四路 2 输入异或门

1 特性

- 缓冲输入
- 宽工作电压范围：2V 至 6V
- 宽工作温度范围：-55°C 至 +125°C
- 支持多达 10 个 LSTTL 负载的扇出
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗

2 应用

- 检测输入信号中的相位差
- 创建可选的逆变器/缓冲器

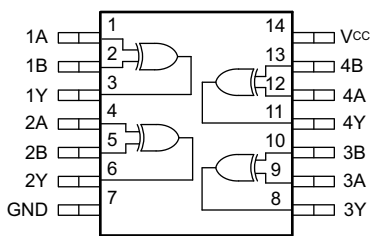
3 说明

此器件包含四个独立双输入异或门。每个逻辑门以正逻辑执行布尔函数 $Y = A \oplus B$ 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
CD74HC86M	SOIC (14)	8.70mm × 3.90mm
CD74HC86E	PDIP (14)	19.30mm × 6.40mm
CD54HC86F	CDIP (14)	21.30mm × 7.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能引脚分配

Table of Contents

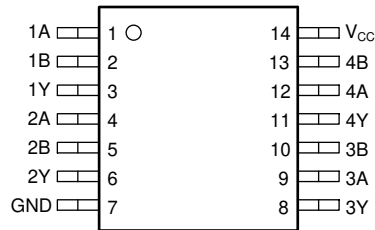
1 特性	1	8.2 Functional Block Diagram.....	8
2 应用	1	8.3 Feature Description.....	8
3 说明	1	8.4 Device Functional Modes.....	9
4 Revision History	2	9 Application and Implementation	10
5 Pin Configuration and Functions	3	9.1 Application Information.....	10
Pin Functions.....	3	9.2 Typical Application.....	10
6 Specifications	4	10 Power Supply Recommendations	12
6.1 Absolute Maximum Ratings.....	4	11 Layout	13
6.2 ESD Ratings.....	4	11.1 Layout Guidelines.....	13
6.3 Recommended Operating Conditions.....	4	11.2 Layout Example.....	13
6.4 Thermal Information.....	5	12 Device and Documentation Support	14
6.5 Electrical Characteristics.....	5	12.1 Documentation Support.....	14
6.6 Switching Characteristics.....	5	12.2 支持资源.....	14
6.7 Operating Characteristics.....	6	12.3 Trademarks.....	14
6.8 Typical Characteristics.....	6	12.4 静电放电警告.....	14
7 Parameter Measurement Information	7	12.5 术语表.....	14
8 Detailed Description	8	13 Mechanical, Packaging, and Orderable Information	14
8.1 Overview.....	8		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (September 2003) to Revision E (June 2021)	Page
• 更新至全新的数据表标准.....	1
• 将 HCT 器件移至单独的数据表 (SCHS410).....	1
• $R_{\theta JA}$ increased for the D package from 86 to 133.6 °C/W and decreased for the N package from 80 to 62.5 °C/W.....	5

5 Pin Configuration and Functions



**D, N, or J Package
14-Pin SOIC, PDIP, or CDIP
Top View**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V _{CC}	14	—	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	- 0.5	7	V	
I _{IK}	Input clamp current ⁽²⁾	V _I < - 0.5 V or V _I > V _{CC} + 0.5 V	±20	mA	
I _{OK}	Output clamp current ⁽²⁾	V _O < - 0.5 V or V _O > V _{CC} + 0.5 V	±20	mA	
I _O	Continuous output current	V _O > - 0.5 V or V _O < V _{CC} + 0.5 V	±25	mA	
	Continuous current through V _{CC} or GND		±50	mA	
T _J	Junction temperature ⁽³⁾		150	°C	
	Lead temperature (soldering 10s)	SOIC - lead tips only	300	°C	
T _{stg}	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 4.5 V	3.15		
		V _{CC} = 6 V	4.2		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 4.5 V		1.35	
		V _{CC} = 6 V		1.8	
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
t _t	Input transition time	V _{CC} = 2 V		1000	ns
		V _{CC} = 4.5 V		500	
		V _{CC} = 6 V		400	
T _A	Operating free-air temperature	- 55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CD74HC86		UNIT
		N (PDIP)	(D SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.5	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.3	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.3	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29.9	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.0	89.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
			25°C			-40°C to 85°C			-55°C to 125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu\text{A}$	2 V	1.9		1.9		1.9		V	
				4.5 V	4.4		4.4		4.4			
				6 V	5.9		5.9		5.9			
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu\text{A}$	2 V		0.1		0.1		0.1	V	
				4.5 V		0.1		0.1		0.1		
				6 V		0.1		0.1		0.1		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 4 \text{ mA}$	4.5 V		0.26		0.33		0.4		
				6 V		0.26		0.33		0.4		
I_I	Input leakage current	$V_I = V_{CC}$ or 0	6 V			± 0.1		± 1		± 1	μA	
						2		20		40		
I_{CC}	Supply current	$V_I = V_{CC}$ or 0	$I_O = 0$	6 V							40	μA
C_i	Input capacitance			5 V							10	pF

6.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			-40°C to 85°C			-55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A or B	Y	$C_L = 50 \text{ pF}$	2 V		120		150		180	ns		
					4.5 V		24		30		36			
					6 V		20		26		31			
		A or B	Y	$C_L = 15 \text{ pF}$	5 V		9							

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			- 40°C to 85°C			- 55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_t	Transition-time	Y	$C_L = 50\text{ pF}$	2 V	75			95			110			ns
				4.5 V	15			19			22			
				6 V	13			16			19			

6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate No load	2 V to 6 V		22		pF

6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$

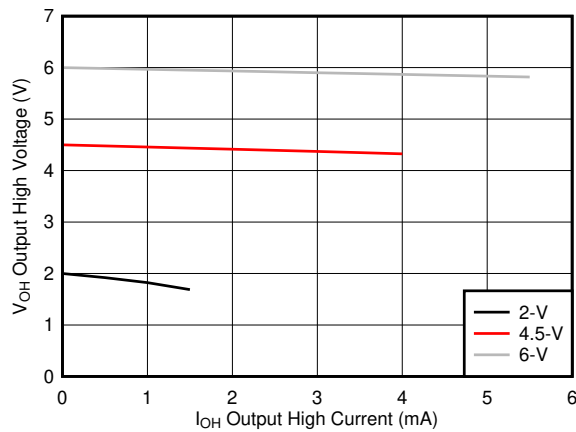


图 6-1. Typical output voltage in the high state (V_{OH})

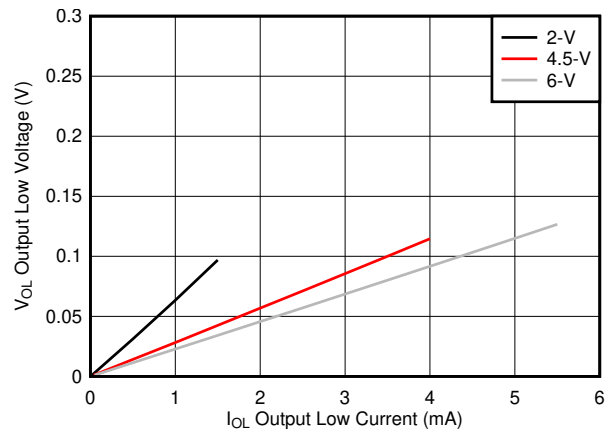
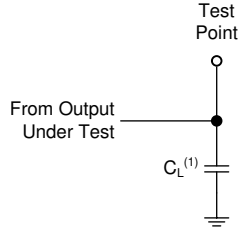


图 6-2. Typical output voltage in the low state (V_{OL})

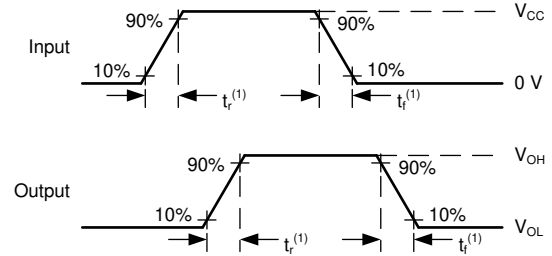
7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.



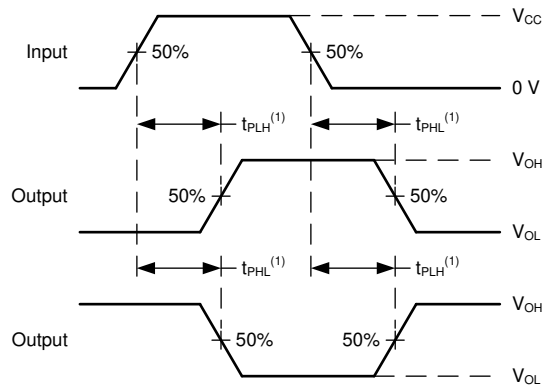
A. $C_L = 50 \text{ pF}$ and includes probe and jig capacitance.

图 7-1. Load Circuit



A. t_t is the greater of t_r and t_f .

图 7-2. Voltage Waveforms Transition Times



A. The maximum between t_{PLH} and t_{PHL} is used for t_{pd} .

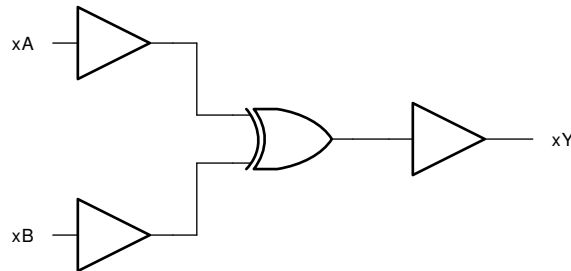
图 7-3. Voltage Waveforms Propagation Delays

8 Detailed Description

8.1 Overview

This device contains four independent 2-input XOR gates. Each gate performs the Boolean function $Y = A \oplus B$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [§ 6.1](#) must be followed at all times.

The CD74HC86 can drive a load with a total capacitance less than or equal to the maximum load listed in the [§ 6.6](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [§ 6.1](#).

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [§ 6.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [§ 6.1](#), and the maximum input leakage current, given in the [§ 6.5](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the [§ 6.3](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 图 8-1.

CAUTION

Voltages beyond the values specified in the 节 6.1 table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

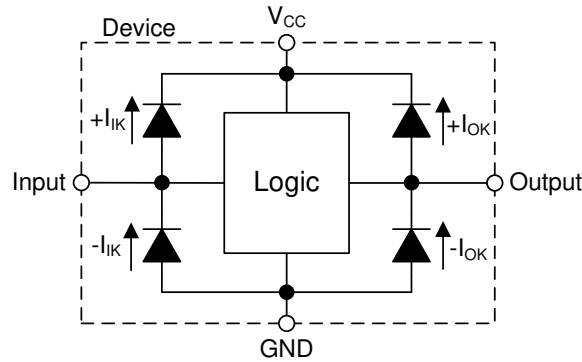


图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

In this application, a 2-input XOR gate is used as a phase difference detector as shown in [图 9-1](#). The remaining three gates can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

The device is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

9.2 Typical Application

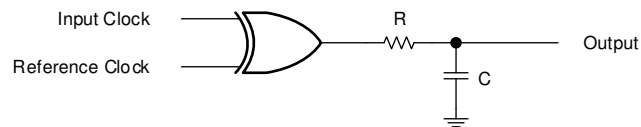


图 9-1. Typical application schematic

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [节 6.3](#). The supply voltage sets the device's electrical characteristics as described in the [节 6.5](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HC86 plus the maximum supply current, I_{CC} , listed in the [节 6.5](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the [节 6.1](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_J(\max)$ listed in the [节 6.1](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [节 6.1](#). These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HC86, as specified in the [节 6.5](#), and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The CD74HC86 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [§ 6.3](#).

Refer to the [§ 8.3](#) for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the [§ 6.5](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [§ 6.5](#).

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to [§ 8.3](#) for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the [§ 11](#).
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HC86 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the [§ 6.1](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

9.2.3 Application Curves

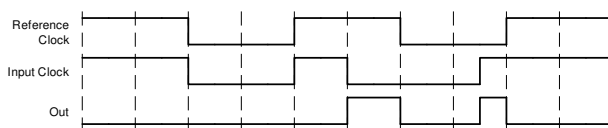


图 9-2. Typical application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [# 6.3](#). Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [图 11-1](#).

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

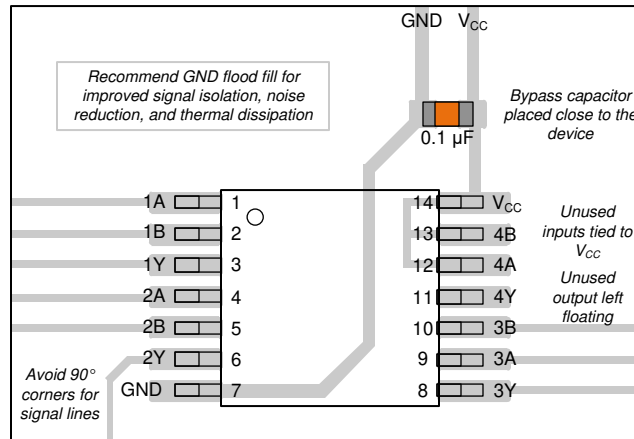


图 11-1. Example layout for the CD74HC86

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

12.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

12.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC86F3A	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8404601CA CD54HC86F3A	Samples
CD74HC86E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC86E	Samples
CD74HC86M	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC86M	Samples
CD74HC86M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC86M	Samples
CD74HC86MT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC86M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

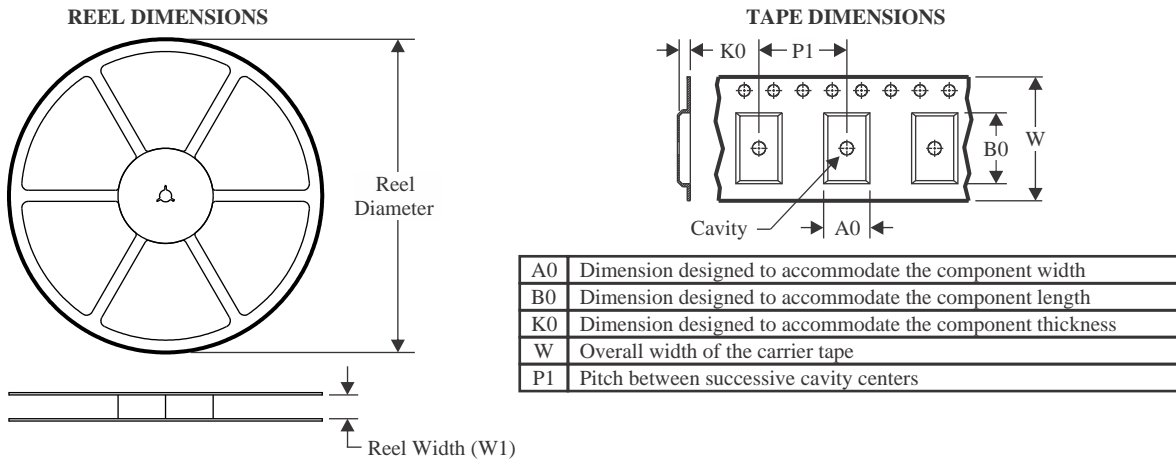
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC86, CD74HC86 :

- Catalog : [CD74HC86](#)
- Military : [CD54HC86](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC86M96	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HC86M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC86MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC86M96	SOIC	D	14	2500	366.0	364.0	50.0
CD74HC86M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC86MT	SOIC	D	14	250	210.0	185.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC86E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC86E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC86M	D	SOIC	14	50	506.6	8	3940	4.32

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

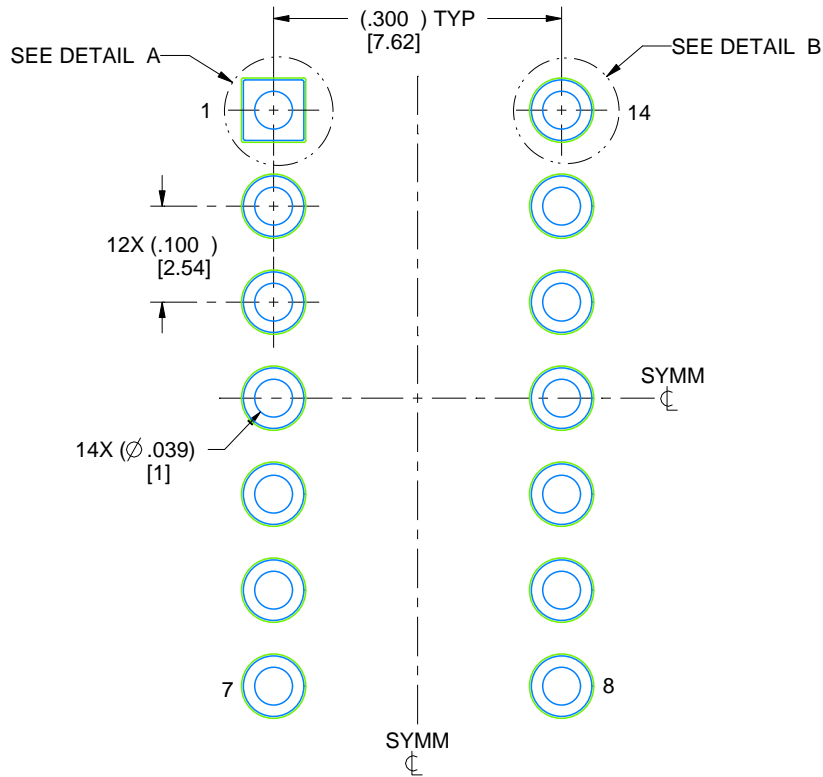
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

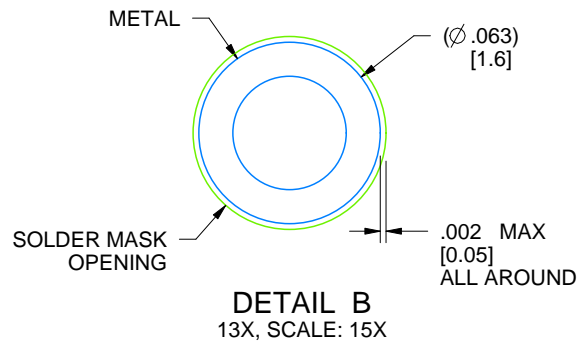
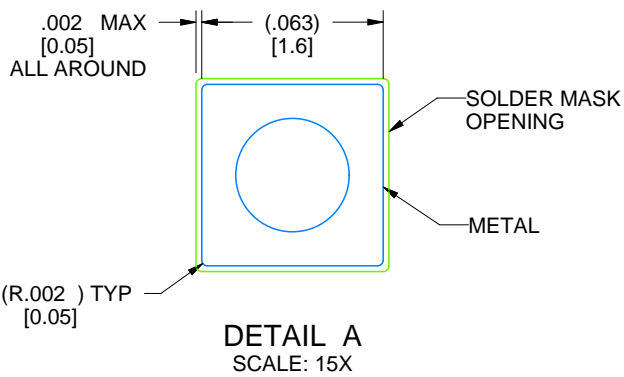
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司