TEXAS INSTRUMENTS
LDC3114-Q1
ZHCSLR1B – DECEMBER 2021 – REVISED DECEMBER 2021

LDC3114-Q1 4 通道混合电感式触控和电感数字转换器

1 特性

- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 的工作环境温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 多种运行模式：
  - 原始数据模式：访问预处理的电感测量数据，从而在 MCU 上实现用于线性检测的先进算法
  - 按钮模式：通过基线跟踪和先进的片上后处理实现按钮按压检测
  - 触控按钮的受力形变测量
- 引脚和寄存器与 LDC2114 兼容
- 稳健的 EMI 性能支持 CISPR 22 和 CISPR 24 合规性
- 四个通道独立运行
- 可配置扫描速率：
  - 0.625SPS 至 160SPS
  - 连续扫描选项
- 先进的按钮按压检测算法：
  - 可调节每个按钮的受力阈值
  - 环境变化补偿
  - 同步按钮按压检测
- 低电流消耗：
  - 一个按钮：在 0.625SPS 下为 6µA
  - 两个按钮：在 20SPS 下为 72µA
- 接口：
  - 支持 1.8V 和 3.3V 电平的 I^2C 和 INTB
  - 按钮每个通道输出 1.8V 逻辑电平

2 应用

- 汽车
  - 触控按钮和压感触控按钮：
    - 方向盘控制
    - 汽车显示模块
    - 汽车音响主机
  - 车门把手模块
  - 动力系统位置传感器
  - 自动变速器

3 说明

LDC3114-Q1 是一款可在各种材料上实现人机界面 (HMI) 触控按钮设计的电感式检测器件，该器件在面板内小型印刷电路板 (PCB) 上安装有线圈，可测量导电目标的小幅偏移。这种技术允许访问表示电感值的原始数据，因此可用于对汽车、消费和工业应用中金属目标的精密线性位置检测。电感式传感解决方案不受湿度或油污和灰尘等非导电污染物的干扰。

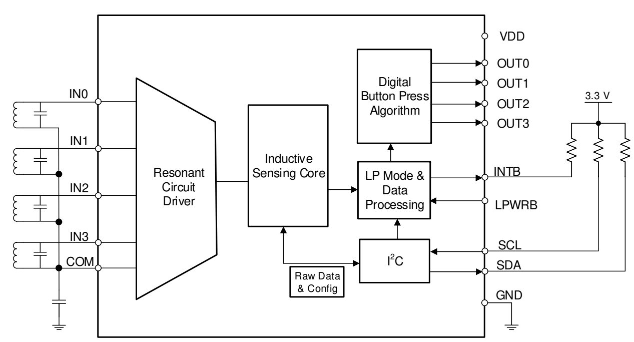
LDC3114-Q1 的按钮模式可自动更正导电目标出现的任何变形。LDC3114-Q1 提供完全匹配的通道，可实现差分和比例式测量，从而对温度和机械漂移等环境和老化条件提供补偿。LDC3114-Q1 还提供了超低功耗模式，适用于电池供电类应用中的开/关按钮或位置传感器。

LDC3114-Q1 可通过 I^2C 接口进行轻松配置。LDC3114-Q1 采用 16 引脚 TSSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LDC3114-Q1	TSSOP (16)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



LDC3114-Q1 简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2021) to Revision B (December 2021)	Page
• Changed the MSBs and LSBs of the four raw data output registers	15

Changes from Revision * (April 2021) to Revision A (December 2021)	Page
• 将数据表状态从“预告信息”更改为：量产数据	1
• Updated 4-ch normal mode high-temp max current limit	4
• Updated 2-ch normal mode high-temp max current limit	4
• Updated low-power mode max current limit	4
• Updated supply current normal power and standby mode curves	7
• Corrected typo for data register address range from 0x05 to 0x09	11
• Changed table title "Button Scan Rate" to "Scan Rate" to make name generic for either button or raw data mode	40
• Removed "button" where appropriate to clarify the difference between "button scan rate" and "raw data scan rate" text	40
• Corrected PCB layout 图 10-1 to have correct device name "LDC3114"	51

5 Pin Configuration and Functions

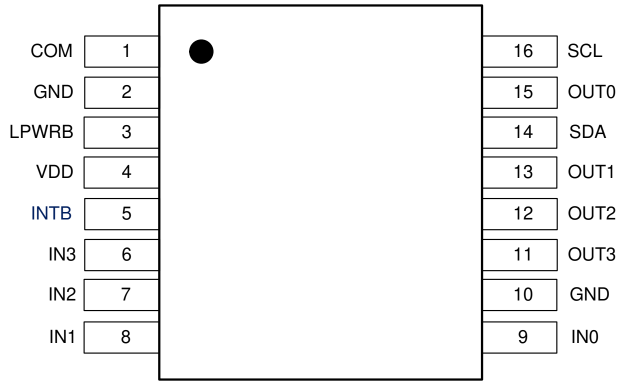

图 5-1. LDC3114-Q1 PW Package 16-Pin TSSOP Top View

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VDD	4	P	Power supply
GND	2 10	G	Ground(2)
INTB	5	O	Interrupt output Polarity can be configured in Register 0x11.
LPWRB	3	I	Normal / Low Power Mode select Set LPWRB to V_{DD} for Normal Power Mode or ground for Low Power Mode.
COM	1	A	Common return current path for all LC resonator sensors A capacitor should be connected from this pin to GND. Refer to *Setting COM Pin Capacitor*.
IN0	9	A	Channel 0 LC sensor input
IN1	8	A	Channel 1 LC sensor input
IN2	7	A	Channel 2 LC sensor input
IN3	6	A	Channel 3 LC sensor input
OUT0	15	O	Channel 0 logic output Polarity can be configured in Register 0x1C.
OUT1	13	O	Channel 1 logic output Polarity can be configured in Register 0x1C.
OUT2	12	O	Channel 2 logic output Polarity can be configured in Register 0x1C.
OUT3	11	O	Channel 3 logic output Polarity can be configured in Register 0x1C.
SCL	16	I	I^2C clock
SDA	14	I/O	I^2C data I^2C address = 0x2A.

(1) I = Input, O = Output, P=Power, G=Ground, A=Analog
(2) Both pins should be connected to the system ground on the PCB.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range unless otherwise noted.[(1)]

		MIN	MAX	UNIT
V_{DD}	Supply voltage		2.2	V
V_I	Voltage on SCL, SDA. INTB	–0.3	3.6	V
	Voltage on any other pin	–0.3	2.2[(2)]	V
T_J	Junction temperature	–40	135	℃
T_{STG}	Storage temperature	–65	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum voltage across any two pins (not including SCL or SDA) is V_{DD} + 0.3 V.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating temperature range unless otherwise noted.

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.71		1.89	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		LDC3114-Q1	UNIT
		TSSOP	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over operating temperature range unless otherwise noted.
Over operating V_{DD} range unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
V_{DD}	Supply voltage		1.71	1.8	1.89	V

Over operating temperature range unless otherwise noted.
Over operating V_{DD} range unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DDNP}	Normal power mode supply current (4 channels)[(1)] [(2)]	4 channels, 40 SPS per channel, 1 ms sampling window per channel, LPWRB = V_{DD} -40℃ ⩽ T_A ⩽ 125℃		0.46	2	mA
	Normal power mode supply current (2 channels)[(1)] [(2)]	2 channels, 40 SPS per channel, 1 ms sampling window per channel, LPWRB = V_{DD} -40℃ ⩽ T_A ⩽ 125℃		0.31	1	mA
I_{DDLP}	Low power mode supply current [(1)] [(2)]	1 channel, 1.25 SPS per channel, 1 ms sampling window per channel, LPWRB = Ground -40℃ ⩽ T_A ⩽ 125℃		10	35	µA
I_{DDSB}	Standby supply current	No button active (EN = 0x00) -40℃ ⩽ T_A ⩽ 125℃		7	22	µA
SENSOR						
$I_{SENSOR, MAX}$	Maximum sensor current drive	Registers SENSOR*n*_CONFIG: RP*n* = 0[(3)]		2.5		mA
$R_{P, MIN}$	Minimum sensor parallel resonant impedance			350		Ω
$R_{P, MAX}$	Maximum sensor parallel resonant impedance			10		kΩ
f_{SENSOR}	Sensor resonant frequency[(4)]		5		30	MHz
$Q_{SENSOR, MIN}$	Minimum sensor quality factor			5		
$Q_{SENSOR, MAX}$	Maximum sensor quality factor			30		
$V_{SENSOR, PP}$	Sensor oscillation peak-to-peak voltage	Measured on the IN*n* [(3)] pins with reference to COM.		0.9		V
C_{IN}	Sensor input pin capacitance			17		pF
CONVERTER						
$SR_{NP, MIN}$	Minimum normal power mode scan rate[(5)]	LPWRB = V_{DD}	7	10	13	SPS
$SR_{NP, MAX}$	Maximum normal power mode scan rate[(5)]	LPWRB = V_{DD}	56	80	104	SPS
$SR_{LP, MIN}$	Minimum low power mode scan rate[(5)]	LPWRB = Ground	0.438	0.625	0.813	SPS
$SR_{LP, MAX}$	Maximum low power mode scan rate[(5)]	LPWRB = Ground	3.5	5	6.5	SPS
f_{REF_CLK}	Internal Reference clock frequency	T_A=25℃		44		MHz
$f_{REF\_CLK\_TC}$	Internal Reference clock frequency variation from T_A=25℃ to over temperature	-40℃ ⩽ T_A ⩽ 125℃		3		%

(1) Sensor configuration: L_{SENSOR} = 0.85 µH, C_{SENSOR} = 58 pF, Q_{SENSOR} = 11, R_P = 0.7 kΩ.
(2) I^2C communication and pull-up resistors current is not included.
(3) The italic *n* is the channel index, *n* = 0, 1, 2, or 3 for LDC3114.
(4) For optimal performance, configure the sensor frequency to be greater than 3 MHz
(5) For typical distribution of the scan rates, refer to 图 6-9.

6.6 Digital Interface

Over operating temperature range unless otherwise noted. Pins: LPWRB, INT_DR, OUT0, OUT1, OUT2, OUT3, and ADDR.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE LEVELS						
V_{IH}	Input high voltage, LPWRB pin		0.8 × V_{DD}			V
V_{IL}	Input low voltage, LPWRB pin				0.2 × V_{DD}	V

Over operating temperature range unless otherwise noted. Pins: LPWRB, INT_DR, OUT0, OUT1, OUT2, OUT3, and ADDR.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage, OUTx pins	I_{SOURCE} = 400 µA	0.8 × V_{DD}			V
V_{OL}	Output low voltage, OUTx pins	I_{SINK} = 400 µA			0.2 × V_{DD}	V
I_L	Digital input leakage current		–500		500	nA
V_{OL_INTB}	Output low voltage, INTB pin	3 mA sink current			0.4	V

6.7 I²C Interface

			MIN	TYP	MAX	UNIT
VOLTAGE LEVELS						
V_{IH_I2C}	Input high voltage		0.7 × V_{DD}			V
V_{IL_I2C}	Input low voltage				0.3 × V_{DD}	V
V_{OL_I2C}	Output low voltage	3 mA sink current			0.2 × V_{DD}	V
HYS_{I2C}	Hysteresis		0.05 × V_{DD}			V
I²C TIMING CHARACTERISTICS						
f_{SCL}	Clock frequency				400	kHz
t_{LOW}	Clock low time		1.3			µs
t_{HIGH}	Clock high time		0.6			µs
$t_{HD;STA}$	Hold time repeated START condition	After this period, the first clock pulse is generated.	0.6			µs
$t_{SU;STA}$	Set-up time for a repeated START condition		0.6			µs
$t_{HD;DAT}$	Data hold time		0			µs
$t_{SU;DAT}$	Data set-up time		100			ns
$t_{SU;STO}$	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{VD;DAT}$	Data valid time				0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time				0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter(1)				50	ns

(1) This parameter is specified by design and/or characterization and is not tested in production.

6.8 Timing Diagram

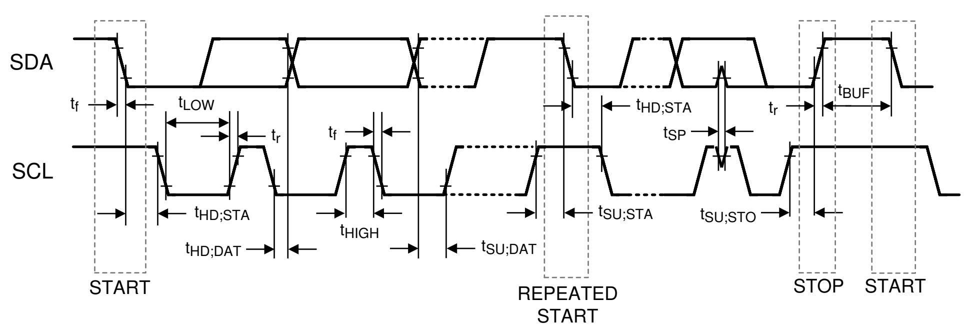

图 6-1. I²C Timing Diagram

6.9 Typical Characteristics

Over recommended operating conditions unless specified otherwise. V_{DD} = 1.8 V, T_J = 25°C. One channel enabled with a button sampling window of 1 ms unless specified otherwise.

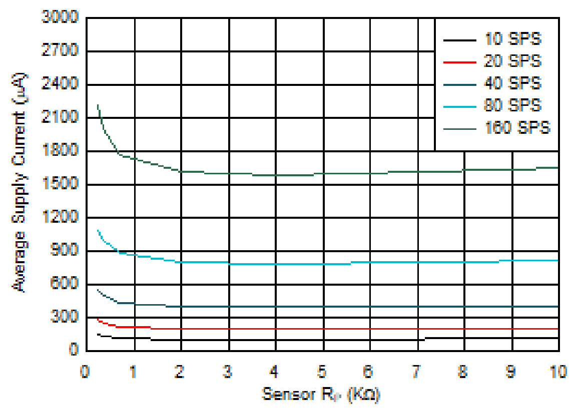

图 6-2. Supply Current vs Sensor R_P for Normal Power Mode. Sensor Frequency = 10 MHz. Sampling Window = 2mS. Four Channels Enabled.

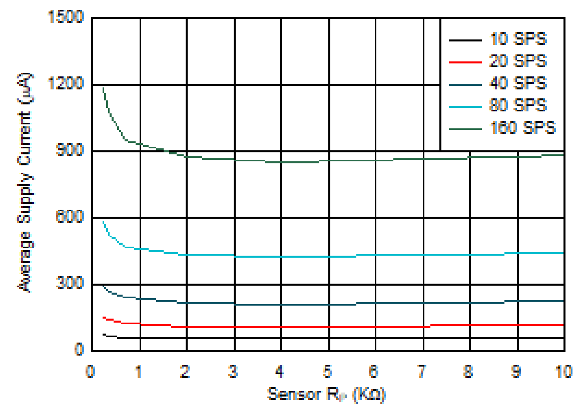

图 6-3. Supply Current vs Sensor R_P for Normal Power Mode. Sensor Frequency = 10 MHz. Sampling Window = 2mS. Two Channels Enabled.

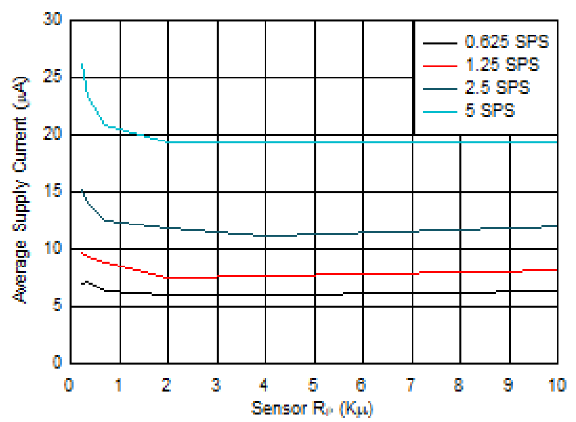

图 6-4. Supply Current vs Sensor R_P for Low Power Mode. Sensor Frequency = 10 MHz.

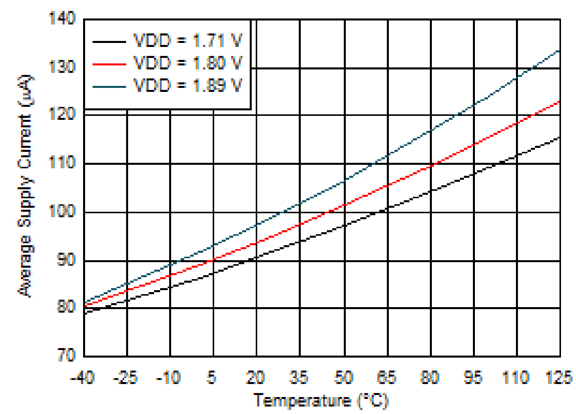

图 6-5. Supply Current vs Temperature. Sensor R_P = 720 Ω, Scan Rate = 40 SPS, Sensor Frequency = 20 MHz.

6.9 Typical Characteristics (continued)

Over recommended operating conditions unless specified otherwise. V_{DD} = 1.8 V, T_J = 25°C. One channel enabled with a button sampling window of 1 ms unless specified otherwise.

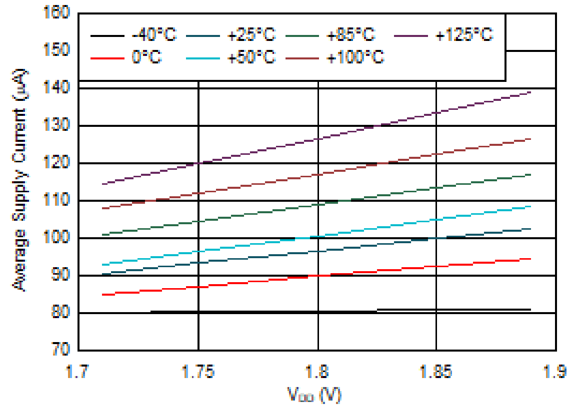

图 6-6. Supply Current vs. V_{DD}. Sensor R_P = 720 Ω, Scan Rate = 40 SPS, Sensor Frequency = 20 MHz.

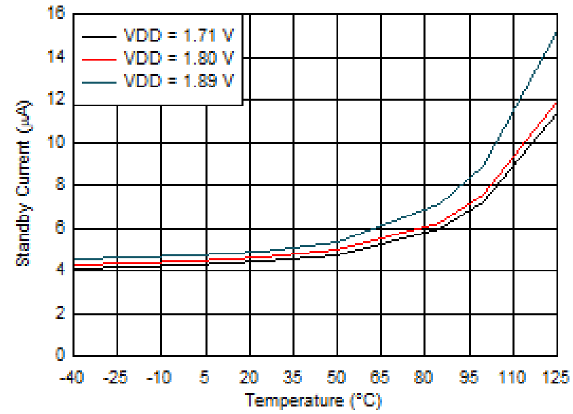

图 6-7. Standby Current vs. Temperature

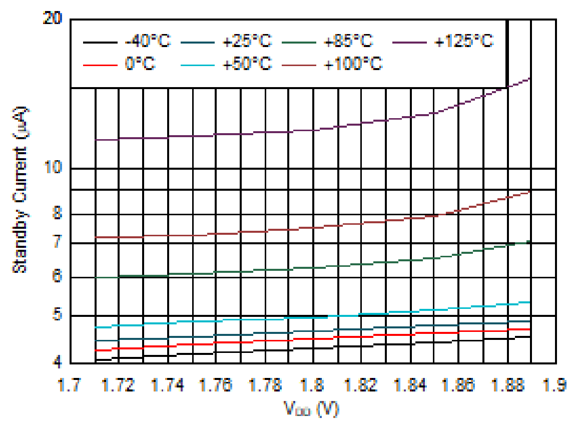

图 6-8. Standby Current vs V_{DD}

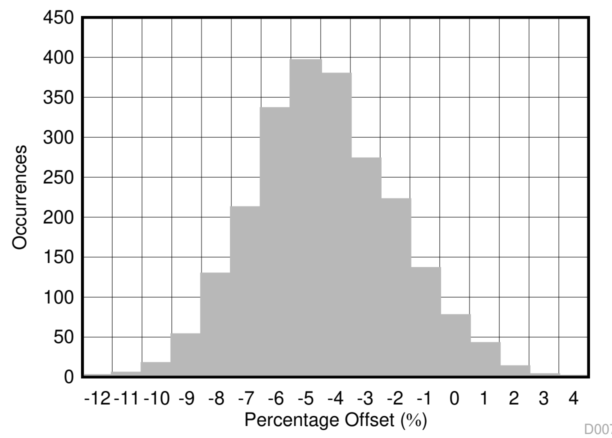

图 6-9. Scan Rate Distribution at 30°C

7 Detailed Description

7.1 Overview

The LDC3114-Q1 is a hybrid multichannel, low-noise, high-resolution inductance-to-digital converter (LDC) optimized for inductive touch applications as well as linear position sensing. Button presses form micro-deflections in the conductive targets which cause frequency shifts in the resonant sensors. The LDC3114-Q1 can measure such frequency shifts and determine when button presses occur. With adjustable sensitivity per input channel, the LDC3114-Q1 can reliably operate with a wide range of physical button structures and materials. The high resolution measurement enables the implementation of force level buttons. The LDC3114-Q1 incorporates customizable post-processing algorithms for enhanced robustness.

The LDC3114-Q1 additionally implements a raw data access mode. The MCU can read directly the data representing the effective inductance of the sensor and implement further post processing. In this mode, additional post processing features such as baseline tracking and algorithms for false button detection are ignored. This mode is useful for linear or rotary position sensing with inductive sensors while having excellent EMI performance across wide range of applications. This mode can also be used to measure the micro-deflection for button-like applications as well.

The LDC3114-Q1 can operate in an ultra-low power mode for optimal battery life, or can be toggled into a higher scan rate for more responsive button press detection for game play or other low latency applications. The LDC3114-Q1 is operational from –40°C to +125°C with a 1.8 V ± 5% power supply voltage.

The LDC3114-Q1 is configured through 400-kHz I^2C. Button presses can be reported through the I^2C interface or with configurable polarity dedicated push-pull outputs. Besides the LC resonant sensors, the only external components necessary for operation are supply bypassing capacitors and a COM pin capacitor to ground.

7.2 Functional Block Diagram

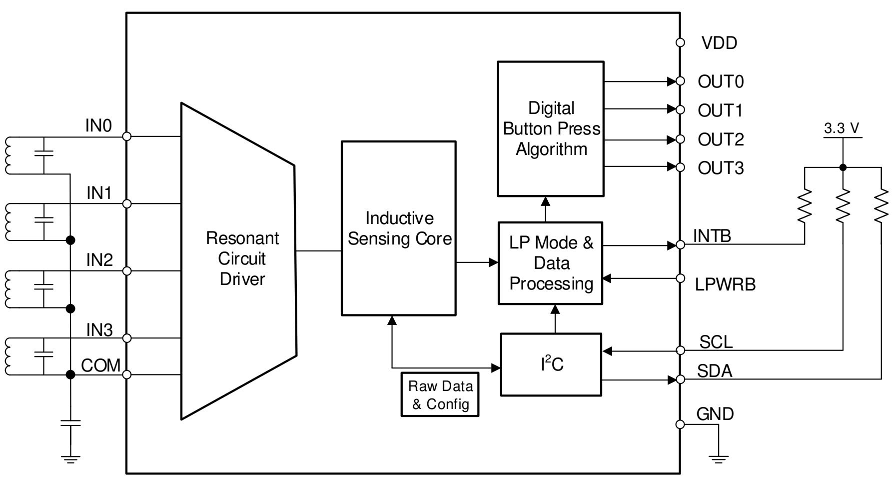

图 7-1. Block Diagram of LDC3114-Q1

7.3 Feature Description

7.3.1 Multimode Operation

LDC3114-Q1 offers two main modes of operations: raw data access mode and button algorithm mode which is controlled by the *BTN_ALG_EN* field in *Register INTPOL Address 0x11*. 图 7-2 shows conceptually how these two modes are implemented.

Raw data access mode allows an external MCU to extract data from the signal after the inductance-to-digital converter from registers through I^2C (see *Raw Data Output*). There is no further processing on this raw data such as baseline tracking, integrated button algorithms and button thresholding. This mode gives MCU full control over the measured raw data to implement algorithms for linear position sensing, rotational encoder applications, metal presence/deflection applications, smart button algorithms and for multimodal sensor fusion applications.

The second mode is button algorithm mode. Here further processing with parameters defined by the user (see *Baseline Tracking* and *Integrated Button Algorithms*) is done on the data and a button thresholding as defined by the user is applied. The processed data are available in separate registers to be read by I^2C and any button press detection is indicated on the OUTx pins (see *Button Output Interfaces*) This mode is used to implement button press functionality and can also be used to implement the measurement of force applied for button press along with detection to implement multilevel button press.

For register settings that are applicable to button mode versus raw access data mode are clearly identified in the descriptions of the registers (see *Register Maps*).

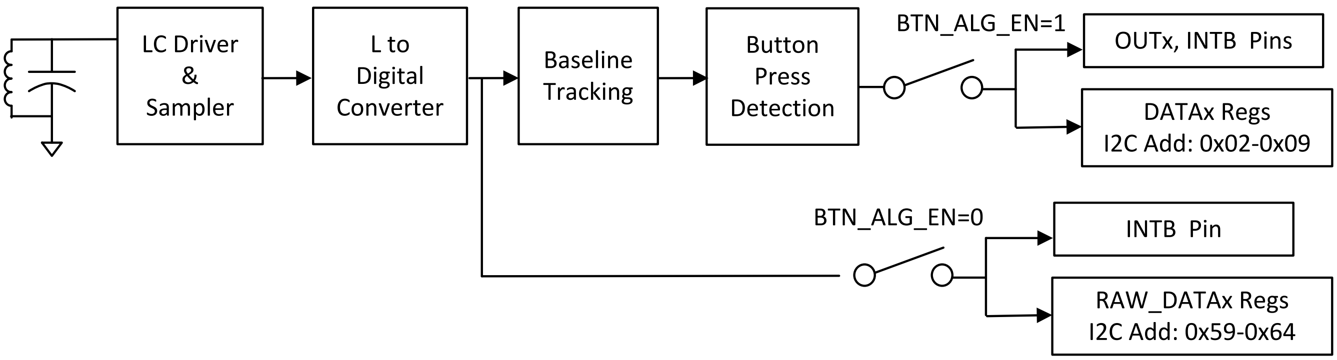

图 7-2. Multimode Operation in LDC3114-Q1

7.3.2 Multichannel and Single-Channel Operation

The LDC3114-Q1 provides four independent sensing channels. In the following sections, some parameters, such as DATA*n* and SENSOR*n*_CONFIG, contain a channel index *n*.

Any of the four channels available in the LDC3114-Q1 can be independently enabled by setting the EN*n* and LPEN*n* (*n* = 0, 1, 2, or 3) bit fields in *Register EN (Address 0x0C)*. The low-power-enable bit LPEN*n* only takes effect if the corresponding EN*n* bit is also set. If only one channel is set active, the LDC3114-Q1 periodically samples the single active channel at the configured scan rate. When several channels are set active, the LDC3114-Q1 operates in multichannel mode, and the device sequentially samples the active channels at the configured scan rate. Each channel of the LDC3114-Q1 can be independently enabled in Low Power Mode and Normal Power Mode.

7.3.3 Raw Data Output

Raw data mode is enabled by setting *BTN_ALG_EN=0x0* field in *Register INTPOL Address 0x11*. 图 7-2 shows that this operation will extract data directly from the output of the inductance-to-digital converter.

The data is read from the I^2C interface of the LDC3114-Q1. The *DATA_RDY* field in *Register OUT (Address 0x01)* indicates when new data is available for reading. In the raw data mode, the INTB pin also assserted when new data is available and can be used by the MCU as an interrupt. The raw data can be extracted by reading, the output RAW_DATA*n*_*x* registers (*n* = 0, 1, 2, or 3, for each channel, *x*= 1, 2, or 3 splitting 24-bit data over 3 8-bit register fields). 方程式 1 shows the relationship between 24-bit data and the sensor frequency.

$$f_{SENSOR} = \frac{30 \times W \times f_{REF\_CLK}}{raw\_data} \quad (1)$$

where:

- f_{sensor} is the instantaneous frequency of the inductive sensor
- f_{REF_CLK} is the internal reference clock frequency as specified in *Electrical Characteristics*
- raw_data is the decimal representation of 24-bit binary data read from the RAW_DATAn_x for a particular channel

- W calculated in 方程式 2 (see *Programming Button or Raw Data Sampling Window* for details):

$$W = 128 \times (1 + SENCYn) \times 2^{LCDIV} \quad (2)$$

7.3.4 Button Output Interfaces

Button events may be reported by using two methods. The first method is to monitor the OUT*n* pins (*n* = 0, 1, 2, or 3), which are push-pull outputs and can be used as interrupts to a microcontroller. The polarities of these pins are programmable through *Register OPOL_DPOL (Address 0x1C)*. Any button press or error condition is also reported by the open-drain pin, INTB. The INTB pin polarity is configurable through *Register INTPOL (Address 0x11)*. Any assertion of INTB is cleared upon reading *Register STATUS (Address 0x00)*. Each push-pull output must be assigned to a dedicated general-purpose input pin on the microcontroller to avoid potential current fights.

The second method is through the I^2C interface. The *Register OUT (Address 0x01)* contains the fields OUT0, OUT1, OUT2, and OUT3, which indicate when a button press has been detected. For more advanced button press measurements, the output DATA*n* registers (*n* = 0, 1, 2, or 3, *Register DATA0_LSB - Address 0x02*), which are 12-bit two's complements, can be retrieved for all active buttons, and processed on a microcontroller. A valid button push is represented by a positive value. The polarity is configurable in *Register OPOL_DPOL (Address 0x1C)*. The DATA*n* values can be used to implement multilevel buttons, where the data value is correlated to the amount of force applied to the button.

7.3.5 Programmable Button Sensitivity

The GAIN*n* registers (Addresses *0x0E*, *0x10*, *0x12*, and *0x14*) enable sensitivity enhancement of individual buttons to ensure consistent behavior of different mechanical structures. The sensitivity has a 64-level gain factor for a normalized gain between 1 and 232. Each gain step increases the gain by an average of 9%.

The gain required for an application is primarily determined by the mechanical rigidity of each individual button. The individual gain steps are listed in the *Gain Table*.

7.3.6 Baseline Tracking

The LDC3114-Q1 incorporates a baseline tracking algorithm to automatically compensate for any slow change in the sensor output caused by environmental variations, such as temperature drift. The baseline tracking is configured independently for Normal Power Mode and Low Power Mode. For more information, refer to *Tracking Baseline*.

备注

The baseline tracking feature is applicable only for button algorithm functionality and cannot be bypassed. To disable baseline tracking, LDC3114-Q1 must be used in raw data access mode. See *Multimode Operation* for details.

7.3.7 Integrated Button Algorithms

The LDC3114-Q1 features several algorithms that can mitigate false button detections due to mechanical non-idealities. The algorithms look for correlated button responses, such as similar or opposite responses between two neighboring buttons, to determine if there is any undesirable mechanical crosstalk. For more information, refer to *Mitigating False Button Detections*.

7.3.8 I^2C Interface

The LDC3114-Q1 features an I^2C Interface that can be used to program the internal registers and read channel data. Before reading the OUT (Address 0x01) or channel DATA*n* (*n* = 0, 1, 2 or 3, Addresses 0x02 through 0x09) registers for button press data or raw channel data, RAW_DATAn_x (*n* = 0, 1, 2, or 3, for each channel, *x*= 1, 2, or 3 splitting 24-bit data over 3 8-bit register fields), the user should always read *Register STATUS (Address 0x00)* first to lock the data. The LDC3114-Q1 supports burst mode with auto-incrementing register addresses. The LDC3114-Q1 has a fixed I^2C address of 0x2A.

For the write sequence, there is a special handshake process that has to take place to ensure data integrity. The sequence of register writes is:

- Set CONFIG_MODE (*Register RESET, Address 0x0A*) bit = 1 to start the register write session.
- Poll for RDY_TO_WRITE (*Register STATUS, Address 0x00*) bit = 1.
- Perform I²C write to configure registers.
- Set CONFIG_MODE (*Register RESET, Address 0x0A*) bit = 0 to terminate the register write session.

After CONFIG_MODE is de-asserted, the new scan cycle will start in less than 1 ms. 图 7-3 shows the waveform of the above process.

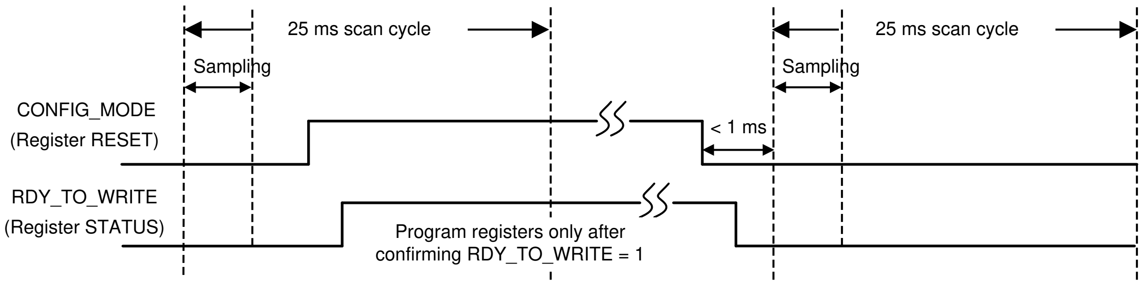

图 7-3. Timing Diagram Representing the States of the CONFIG_MODE and RDY_TO_WRITE Bits for an I²C Write Handshake

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备注

The I²C interface pin, the SDA, the SCL, and the INTB pins are all open-drain and 3.3-V compatible. These pins can be used to connect to an MCU which is supplied by 3.3-V supply without requiring voltage level translation between LDC3114-Q1 and the MCU.

7.3.8.1 I²C Interface Specifications

The maximum speed of the I²C interface is 400 kHz. This sequence uses the standard I²C 7-bit target address followed by an 8-bit pointer to set the register address. For both write and read, the address pointer will auto-increment as long as the controller acknowledges.

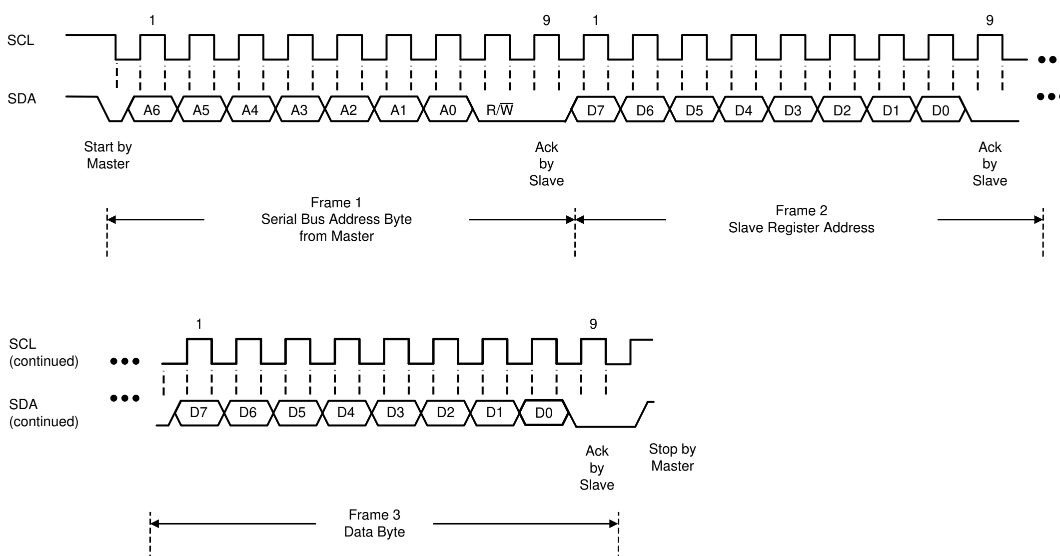


图 7-4. I²C Sequence of Writing a Single Register

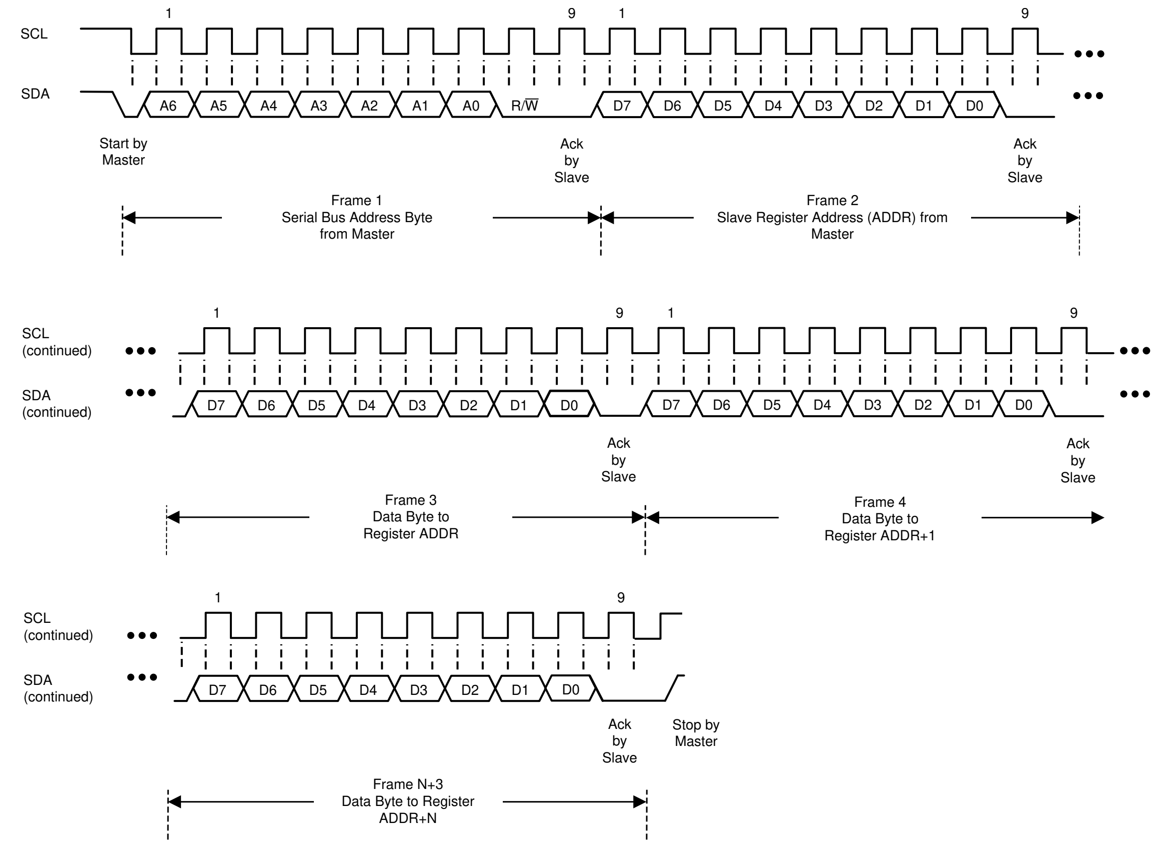


图 7-5. I^{2}C Sequence of Writing Consecutive Registers

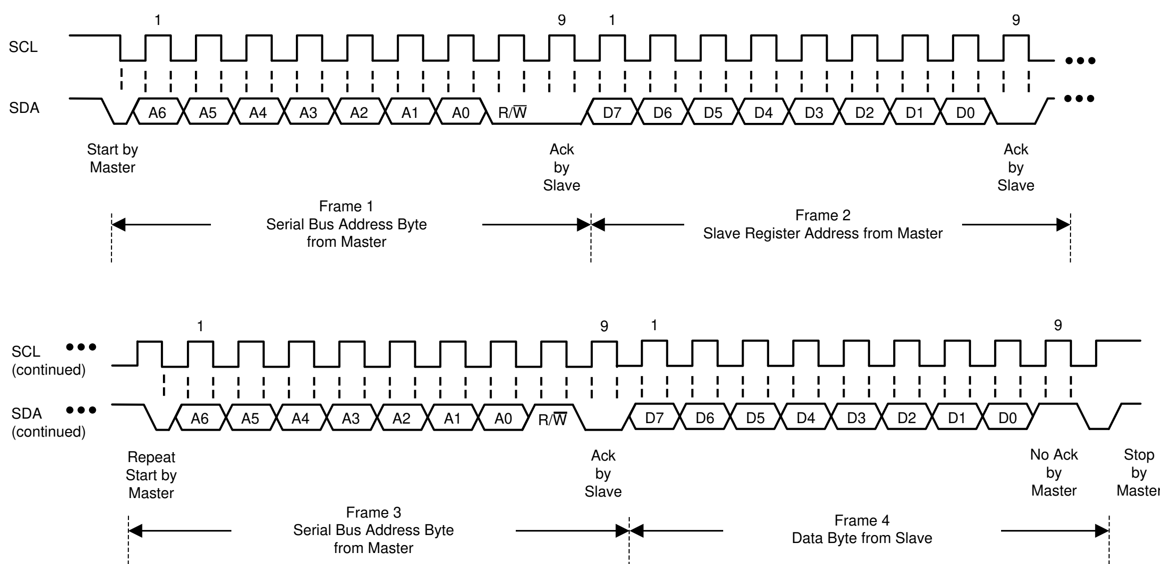


图 7-6. I^{2}C Sequence of Reading a Single Register

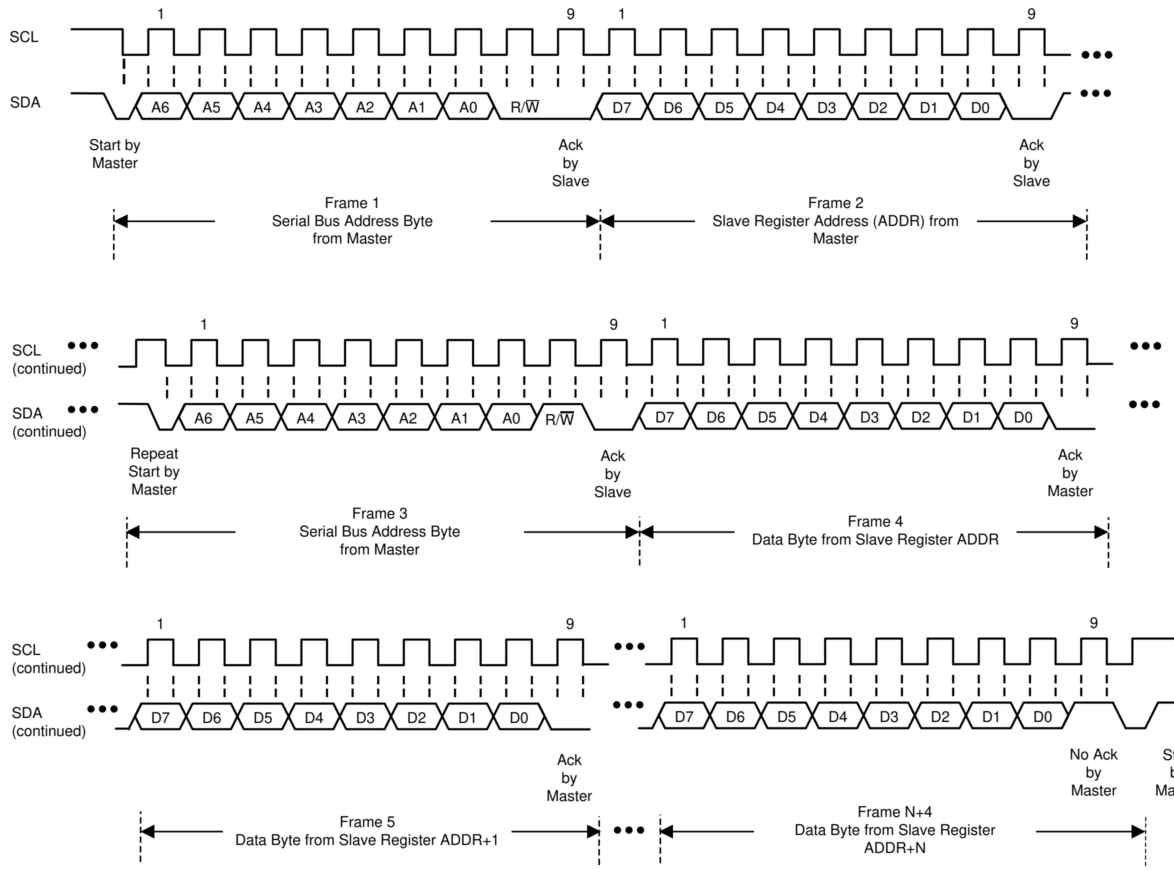


图 7-7. I²C Sequence of Reading Consecutive Registers

7.3.8.2 I²C Bus Control

The LDC3114-Q1 cannot drive the I²C clock (SCL), that is the device does not support clock stretching. In the unlikely event where the SCL is stuck LOW, power cycle any device that is holding the SCL to activate its internal Power-On Reset (POR) circuit. If the LDC is connected to the same power supply as that device, there will be about 66-ms setup time before the LDC becomes active again. For more information, refer to *Defining Power-On Timing*. If the data line (SDA) is stuck LOW, the I²C controller should send nine clock pulses. The device that is holding the bus LOW should release the bus sometime within those nine clocks. If not, then power cycle to clear the bus.

The LDC3114-Q1 has built-in monitors to check that the device is currently working. In the unlikely event of a device fault, the device state will be reset internally, and all the registers will be reset with default settings. For system robustness, TI recommends to check the value of a modified register periodically to monitor the device status and reload the register settings, if needed.

7.4 Device Functional Modes

The LDC3114-Q1 supports two power modes of operation: a Normal Power Mode for active sampling at 10, 20, 40, or 80 SPS, and a Low Power Mode for reduced current consumption at 0.625, 1.25, 2.5, or 5 SPS. The device can also be configured in Normal Power Mode for additional faster sampling rate of 160 SPS or for a continuous sampling rate. Refer to *Configuring Button or Raw Data Scan Rate* for details.

7.4.1 Normal Power Mode

When the LPWRB input pin is set to V_{DD}, all enabled channels operate in Normal Power Mode. Each channel can be enabled independently through *Register EN (Address 0x0C)*. For the electrical specification of Normal Power Mode Scan Rate, refer to the *Electrical Characteristics* table.

7.4.2 Low Power Mode

When the LPWRB input pin is set to ground, only the low-power-enabled channels are active. Each channel can be enabled independently to operate in Low Power Mode through *Register EN (Address 0x0C)*. For a channel to operate in the Low Power Mode, both the LPEN*n* and EN*n* bits (*n* is the channel index) must be set to 1. The Low Power Mode allows for energy-saving monitoring of button activity. In this mode, the device is in an inactive power-saving state for the majority of the time. Lower scan rates correspond to lower current consumption. In addition, the individual button sampling window should be set to the lowest effective setting (this is system dependent, but typically 0.8 ms to 1 ms). For the electrical specification of the configurable Low Power Mode Scan Rate, refer to the *Electrical Characteristics* table.

If a channel is operational in both Low Power Mode and Normal Power Mode, TI recommends to toggle the LPWRB pin only after the button associated with that channel is released.

The Low Power Mode is also applicable for raw data access mode.

7.4.3 Configuration Mode

Before configuring any register settings, the device must be put into the configuration mode first. Setting CONFIG_MODE = 1 through *Register RESET (Address 0x0A)* stops data conversion and holds the device in configuration mode. Any device configuration changes can then be made. The current consumption in this mode is typically 0.3 mA. After all changes have been written, set CONFIG_MODE = 0 for normal operation. Refer to *I^2C Interface* for more information.

7.5 Register Maps

7.5.1 LDC3114 Registers

LDC3114 Registers lists the memory-mapped registers for the LDC3114 registers. All register offset addresses not listed in LDC3114 Registers should be considered as reserved locations and the register contents should not be modified.

表 7-1. LDC3114 Registers

Offset	Acronym	Register Name	Section
0h	STATUS	Device status	节 7.5.1.1
1h	OUT	Channel output logic states	节 7.5.1.2
2h	DATA0_LSB	The lower 8 bits of the Button 0 data (Two's complement	节 7.5.1.3
3h	DATA0_MSB	The upper 4 bits of the Button 0 data (Two's complement)	节 7.5.1.4
4h	DATA1_LSB	The lower 8 bits of the Button 1 data (Two's complement)	节 7.5.1.5
5h	DATA1_MSB	The upper 4 bits of the Button 1 data (Two's complement)	节 7.5.1.6
6h	DATA2_LSB	The lower 8 bits of the Button 2 data (Two's complement)	节 7.5.1.7
7h	DATA2_MSB	The upper 4 bits of the Button 2 data (Two's complement)	节 7.5.1.8
8h	DATA3_LSB	The lower 8 bits of the Button 3 data (Two's complement)	节 7.5.1.9
9h	DATA3_MSB	The upper 4 bits of the Button 3 data (Two's complement)	节 7.5.1.10
Ah	RESET	Reset device and register configurations	节 7.5.1.11
Ch	EN	Enable channels and low power modes	节 7.5.1.12
Dh	NP_SCAN_RATE	Normal Power Mode scan rate	节 7.5.1.13
Eh	GAIN0	Gain for Channel 0 sensitivity adjustment for button algorithm	节 7.5.1.14
Fh	LP_SCAN_RATE	Low Power Mode scan rate	节 7.5.1.15

表 7-1. LDC3114 Registers (continued)

Offset	Acronym	Register Name	Section
10h	GAIN1	Gain for Channel 1 sensitivity adjustment for button algorithm	节 7.5.1.16
11h	INTPOL	Interrupt polarity	节 7.5.1.17
12h	GAIN2	Gain for Channel 2 sensitivity adjustment for button algorithm	节 7.5.1.18
13h	LP_BASE_INC	Low power base increment for button algorithm	节 7.5.1.19
14h	GAIN3	Gain for Channel 3 sensitivity adjustment for button algorithm	节 7.5.1.20
15h	NP_BASE_INC	Normal power base increment for button algorithm	节 7.5.1.21
16h	BTPAUSE_MAXWIN	Baseline tracking pause and Max-win for button algorithm	节 7.5.1.22
17h	LC_DIVIDER	LC oscillation frequency divider	节 7.5.1.23
18h	HYST	Hysteresis for threshold for button algorithm	节 7.5.1.24
19h	TWIST	Anti-twist for button algorithm	节 7.5.1.25
1Ah	COMMON_DEFORM	Anti-common and anti-deformation for button algorithm	节 7.5.1.26
1Ch	OPOL_DPOL	Output polarity for button data and output	节 7.5.1.27
1Eh	CNTSC	Counter scale	节 7.5.1.28
20h	SENSOR0_CONFIG	Sensor 0 cycle count, frequency, RP range	节 7.5.1.29
22h	SENSOR1_CONFIG	Sensor 1 cycle count, frequency, RP range	节 7.5.1.30
24h	SENSOR2_CONFIG	Sensor 2 cycle count, frequency, RP range	节 7.5.1.31
25h	FTF0	Sensor 0 fast tracking factor for button algorithm	节 7.5.1.32
26h	SENSOR3_CONFIG	Sensor3 cycle count, frequency, RP range	节 7.5.1.33
28h	FTF1_2	Sensors 1 and 2 fast tracking factors for button algorithm	节 7.5.1.34
2Bh	FTF3	Sensor 3 fast tracking factor for button algorithm	节 7.5.1.35
59h	RAW_DATA0_3	Sensor 0 pre-processed raw data	节 7.5.1.36
5Ah	RAW_DATA0_2	Sensor 0 pre-processed raw data	节 7.5.1.37
5Bh	RAW_DATA0_1	Sensor 0 pre-processed raw data	节 7.5.1.38
5Ch	RAW_DATA1_3	Sensor 1 pre-processed raw data	节 7.5.1.39
5Dh	RAW_DATA1_2	Sensor 1 pre-processed raw data	节 7.5.1.40
5Eh	RAW_DATA1_1	Sensor 1 pre-processed raw data	节 7.5.1.41
5Fh	RAW_DATA2_3	Sensor 2 pre-processed raw data	节 7.5.1.42
60h	RAW_DATA2_2	Sensor 2 pre-processed raw data	节 7.5.1.43
61h	RAW_DATA2_1	Sensor 2 pre-processed raw data	节 7.5.1.44
62h	RAW_DATA3_3	Sensor 3 pre-processed raw data	节 7.5.1.45
63h	RAW_DATA3_2	Sensor 3 pre-processed raw data	节 7.5.1.46
64h	RAW_DATA3_1	Sensor 3 pre-processed raw data	节 7.5.1.47
FCh	MANUFACTURER_ID_LSB	Manufacturer ID lower byte	节 7.5.1.48
FDh	MANUFACTURER_ID_MSB	Manufacturer ID upper byte	节 7.5.1.49
FEh	DEVICE_ID_LSB	Device ID lower byte	节 7.5.1.50
FFh	DEVICE_ID_MSB	Device ID upper byte	节 7.5.1.51

Complex bit access types are encoded to fit into small table cells. LDC3114 Access Type Codes shows the codes that are used for access types in this section.

表 7-2. LDC3114 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

7.5.1.1 STATUS Register (Offset = 0h) [Reset = 40h]

STATUS is shown in STATUS Register Field Descriptions.

Return to the LDC3114 Registers.

Device status

表 7-3. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_STATUS	R	0h	**Output Status** Logic OR of output OUTx bits. This field is cleared by reading this register.
6	CHIP_READY	R	1h	**Chip Ready Status** 0h = Chip not ready after internal reset 1h = Chip ready after internal reset
5	RDY_TO_WRITE	R	0h	**Ready to Write** Indicates if registers are ready to be written. See I2C Interface section for more information. 0h = Registers not ready 1h = Registers ready
4	MAXOUT	R	0h	**Maximum Output Code** Indicates if any channel button output data reaches the maximum value (+0x7FF or -0x800). Cleared by a read of the status register. 0h = No maximum output code 1h = Maximum output code
3	FSM_WD	R	0h	**Finite-State Machine Watchdog Error** Reports an error has occurred and conversions have been halted. Cleared by a read of the status register. 0h = No error in finite-state machine 1h = Error in finite-state machine
2	LC_WD	R	0h	**LC Sensor Watchdog Error** Reports an error when any LC oscillator fails to start. Cleared by a read of the status register. 0h = No error in LC oscillator initialization 1h = Error in LC oscillator initialization
1	TIMEOUT	R	0h	**Button Timeout** Reports when any button is asserted for more than 50 seconds. Cleared by a read of the status register. When DIS_BTN_TO is set, no timeout is asserted 0h = no timeout error 1h = timeout error

表 7-3. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	REGISTER_FLAG	R	0h	**Register Integrity Flag** Reports if any register's value has an unexpected change. Cleared by a read of the status register. 0h = No unexpected register change 1h = Unexpected register change

7.5.1.2 OUT Register (Offset = 1h) [Reset = 00h]

OUT is shown in OUT Register Field Descriptions.

Return to the LDC3114 Registers.

Channel output logic states

表 7-4. OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	DATA_RDY	R	0h	Output Logic State for pre-processed data capture for any enabled channel. Bit cleared on read. 0h = Data Capture in progress 1h = New Data available
3	OUT3	R	0h	**Button output output Logic State for Channel 3** 0h = No button press detected on Channel 3 1h = Button press detected on Channel 3
2	OUT2	R	0h	**Button output Logic State for Channel 2** 0h = No button press detected on Channel 2 1h = Button press detected on Channel 2
1	OUT1	R	0h	**Button output Logic State for Channel 1** 0h = No button press detected on Channel 1 1h = Button press detected on Channel 1
0	OUT0	R	0h	**Button output Logic State for Channel 0** 0h = No button press detected on Channel 0 1h = Button press detected on Channel 0.

7.5.1.3 DATA0_LSB Register (Offset = 2h) [Reset = 00h]

DATA0_LSB is shown in DATA0_LSB Register Field Descriptions.

Return to the LDC3114 Registers.

The lower 8 bits of the Button 0 data (Two's complement

表 7-5. DATA0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA0[7:0]	R	0h	The lower 8 bits of Channel 0 button data (Two's complement).

7.5.1.4 DATA0_MSB Register (Offset = 3h) [Reset = 00h]

DATA0_MSB is shown in DATA0_MSB Register Field Descriptions.

Return to the LDC3114 Registers.

The upper 4 bits of the Button 0 data (Two's complement)

表 7-6. DATA0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	DATA0[11:8]	R	0h	The upper 4 bits of Channel 0 button data (Two's complement).

7.5.1.5 DATA1_LSB Register (Offset = 4h) [Reset = 00h]

DATA1_LSB is shown in DATA1_LSB Register Field Descriptions.

Return to the LDC3114 Registers.

The lower 8 bits of the Button 1 data (Two's complement)

表 7-7. DATA1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA1[7:0]	R	0h	The lower 8 bits of Channel 1 button data (Two's complement).

7.5.1.6 DATA1_MSB Register (Offset = 5h) [Reset = 00h]

DATA1_MSB is shown in DATA1_MSB Register Field Descriptions.

Return to the LDC3114 Registers.

The upper 4 bits of the Button 1 data (Two's complement)

表 7-8. DATA1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	DATA1[11:8]	R	0h	The upper 4 bits of Channel 1 button data (Two's complement).

7.5.1.7 DATA2_LSB Register (Offset = 6h) [Reset = 00h]

DATA2_LSB is shown in DATA2_LSB Register Field Descriptions.

Return to the LDC3114 Registers.

The lower 8 bits of the Button 2 data (Two's complement)

表 7-9. DATA2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA2[7:0]	R	0h	The lower 8 bits of Channel 2 button data (Two's complement).

7.5.1.8 DATA2_MSB Register (Offset = 7h) [Reset = 00h]

DATA2_MSB is shown in DATA2_MSB Register Field Descriptions.

Return to the LDC3114 Registers.

The upper 4 bits of the Button 2 data (Two's complement)

表 7-10. DATA2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	DATA2[11:8]	R	0h	The upper 4 bits of Channel 2 button data (Two's complement).

7.5.1.9 DATA3_LSB Register (Offset = 8h) [Reset = 00h]

DATA3_LSB is shown in DATA3_LSB Register Field Descriptions.

Return to the LDC3114 Registers.

The lower 8 bits of the Button 3 data (Two's complement)

表 7-11. DATA3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA3[7:0]	R	0h	The lower 8 bits of Channel 3 button data (Two's complement).

7.5.1.10 DATA3_MSB Register (Offset = 9h) [Reset = 00h]

DATA3_MSB is shown in DATA3_MSB Register Field Descriptions.

Return to the LDC3114 Registers.

The upper 4 bits of the Button 3 data (Two's complement)

表 7-12. DATA3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	DATA3[11:8]	R	0h	The upper 4 bits of Channel 3 button data (Two's complement).

7.5.1.11 RESET Register (Offset = Ah) [Reset = 00h]

RESET is shown in RESET Register Field Descriptions.

Return to the LDC3114 Registers.

Reset device and register configurations

表 7-13. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	Reserved
4	FULL_RESET	R/W	0h	**Device Reset** 0h = Normal operation 1h = Resets the device and register configurations. All registers will be returned to default values. Normal operation will not resume until STATUS:CHIP_READY = 1.
3-1	RESERVED	R/W	0h	Reserved
0	CONFIG_MODE	R/W	0h	**Configuration Mode** Any device configuration changes should be made with this bit set to 1. After all configuration changes have been written, set this bit to 0 for normal operation. 0h = Normal operation 1h = Holds the device in configuration mode (no data conversion), but maintains current register configurations.

7.5.1.12 EN Register (Offset = Ch) [Reset = 1Fh]

EN is shown in EN Register Field Descriptions.

Return to the LDC3114 Registers.

Enable channels and low power modes

表 7-14. EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LPEN3	R/W	0h	**Channel 3 Low-Power-Enable** 0h = Disable Channel 3 in Low Power Mode 1h = Enable Channel 3 in Low Power Mode. EN3 must also be set to 1.
6	LPEN2	R/W	0h	**Channel 2 Low-Power-Enable** 0h = Disable Channel 2 in Low Power Mode 1h = Enable Channel 2 in Low Power Mode. EN2 must also be set to 1.
5	LPEN1	R/W	0h	**Channel 1 Low-Power-Enable** 0h = Disable Channel 1 in Low Power Mode 1h = Enable Channel 1 in Low Power Mode. EN1 must also be set to 1.
4	LPEN0	R/W	1h	**Channel 0 Low-Power-Enable** 0h = Disable Channel 0 in Low Power Mode 1h = Enable Channel 0 in Low Power Mode. EN0 must also be set to 1.
3	EN3	R/W	1h	**Channel 3 Enable** 0h = Disable Channel 2 1h = Enable Channel 2
2	EN2	R/W	1h	**Channel 2 Enable** 0h = Disable Channel 2 1h = Enable Channel 2
1	EN1	R/W	1h	**Channel 1 Enable** 0h = Disable Channel 1 1h = Enable Channel 1
0	EN0	R/W	1h	**Channel 0 Enable** 0h = Disable Channel 0 1h = Enable Channel 0

7.5.1.13 NP_SCAN_RATE Register (Offset = Dh) [Reset = 01h]

NP_SCAN_RATE is shown in NP_SCAN_RATE Register Field Descriptions.

Return to the LDC3114 Registers.

Normal Power Mode scan rate

表 7-15. NP_SCAN_RATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved
3	NPFSR	R/W	0h	Normal Power Mode Fast Scan Rate of 160SPS. When set, this bit will override setting in NPSR only and not NPCS.
2	NPCS	R/W	0h	Continuous key scan in Normal Power mode When set, the scan cycle is continuous without delay in the Normal Power mode. The base increment value is fixed. This bit has no effect if the chip is in Low Power mode. This bit will override the setting in NPSR and NPFSR registers.

表 7-15. NP_SCAN_RATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	NPSR	R/W	1h	**Normal Power Mode Scan Rate** Refer to Configuring Button Scan Rate section for more information. 0h = 80 SPS 1h = 40 SPS (Default) 2h = 20 SPS 3h = 10 SPS

7.5.1.14 GAIN0 Register (Offset = Eh) [Reset = 28h]

GAIN0 is shown in GAIN0 Register Field Descriptions.

Return to the LDC3114 Registers.

Gain for Channel 0 sensitivity adjustment for button algorithm

表 7-16. GAIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5-0	GAIN0	R/W	28h	**Gain for Button Data for Channel 0** Refer to the Gain Table for detailed configuration.

7.5.1.15 LP_SCAN_RATE Register (Offset = Fh) [Reset = 10h]

LP_SCAN_RATE is shown in LP_SCAN_RATE Register Field Descriptions.

Return to the LDC3114 Registers.

Low Power Mode scan rate

表 7-17. LP_SCAN_RATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	4h	Reserved
1-0	LPSR	R/W	0h	**Low Power Mode Scan Rate** Refer to Configuring Button Scan Rate section for more information. 0h = 5 SPS 1h = 2.5 SPS 2h = 1.25 SPS (Default) 3h = 0.625 SPS

7.5.1.16 GAIN1 Register (Offset = 10h) [Reset = 28h]

GAIN1 is shown in GAIN1 Register Field Descriptions.

Return to the LDC3114 Registers.

Gain for Channel 1 sensitivity adjustment for button algorithm

表 7-18. GAIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5-0	GAIN1	R/W	28h	**Gain for Button Data for Channel 1** Refer to the Gain Table for detailed configuration.

7.5.1.17 INTPOL Register (Offset = 11h) [Reset = 18h]

INTPOL is shown in INTPOL Register Field Descriptions.

Return to the LDC3114 Registers.

Interrupt polarity

表 7-19. INTPOL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	Reserved
4	BTSRT_EN	R/W	1h	**Enable reset of button algorithm baseline tracking value** When this bit is not set, during transition between normal power mode to low power mode and back to normal power mode **only baseline tracking value** for enabled channels not reset. Other values in the button algorithm for calculating button press are reset even if this bit is not set. 0h = Disable Button Algorithm Restart 1h = Enable Button Algorithm Restart
3	BTN_ALG_EN	R/W	1h	**Enable button press detection algorithm to assert events on OUT_x pins** When disabled, raw pre-processed data can be accessed via RAW_DATAx registers. When disabled, interrupt on INTB pin is asserted when pre-processed data capture is complete after active window period completion for any of the enabled channels or for error events. When disabled, events on OUT_x pins pins are ignored to assert interrupt on INTB pin 0h = Disable Button Algorithm 1h = Enable Button Algorithm
2	INTPOL	R/W	0h	**Interrupt Polarity** 0h = Set INTB pin polarity to active low 1h = Set INTB pin polarity to active high.
1	DIS_BTN_TO	R/W	0h	Disable Button time-out if if button pressed for more than 50s. 0h = Enable Button Timeout 1h = Disable Button Timeout
0	DIS_BTB_MO	R/W	0h	Disable setting MAXOUT bit if button algorithm generates codes outside maximum range. 0h = Enable MAXOUT check 1h = Disable MAXOUT check

7.5.1.18 GAIN2 Register (Offset = 12h) [Reset = 28h]

GAIN2 is shown in GAIN2 Register Field Descriptions.

Return to the LDC3114 Registers.

Gain for Channel 2 sensitivity adjustment for button algorithm

表 7-20. GAIN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5-0	GAIN2	R/W	28h	**Gain for Button Data for Channel 2** Refer to the Gain Table for detailed configuration.

7.5.1.19 LP_BASE_INC Register (Offset = 13h) [Reset = 05h]

LP_BASE_INC is shown in LP_BASE_INC Register Field Descriptions.

Return to the LDC3114 Registers.

Low power base increment for button algorithm

表 7-21. LP_BASE_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2-0	LPBI	R/W	5h	**Baseline Tracking Increment for button algorithm in Low Power Mode**

7.5.1.20 GAIN3 Register (Offset = 14h) [Reset = 28h]

GAIN3 is shown in GAIN3 Register Field Descriptions.

Return to the LDC3114 Registers.

Gain for Channel 3 sensitivity adjustment for button algorithm

表 7-22. GAIN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5-0	GAIN3	R/W	28h	**Gain for Button Data for Channel 3** Refer to the Gain Table for detailed configuration.

7.5.1.21 NP_BASE_INC Register (Offset = 15h) [Reset = 03h]

NP_BASE_INC is shown in NP_BASE_INC Register Field Descriptions.

Return to the LDC3114 Registers.

Normal power base increment for button algorithm

表 7-23. NP_BASE_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2-0	NPBI	R/W	3h	**Baseline Tracking Increment in Normal Power Mode for button algorithm** Refer to Tracking Baseline section for more information.

7.5.1.22 BTPAUSE_MAXWIN Register (Offset = 16h) [Reset = 00h]

BTPAUSE_MAXWIN is shown in BTPAUSE_MAXWIN Register Field Descriptions.

Return to the LDC3114 Registers.

Baseline tracking pause and Max-win for button algorithm

表 7-24. BTPAUSE_MAXWIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BTPAUSE3	R/W	0h	**Baseline Tracking Pause for Channel 3** Pauses baseline tracking for button algorithm for Channel 3 when OUT3 is asserted. Refer to Tracking Baseline section for more information. 0h = Normal baseline tracking for Channel 1 regardless of OUT3 status. 1h = Pauses baseline tracking for Channel 1 when OUT3 is asserted.

表 7-24. BTPAUSE_MAXWIN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BTPAUSE2	R/W	0h	**Baseline Tracking Pause for Channel 2** Pauses baseline tracking for button algorithm for Channel 2 when OUT2 is asserted. Refer to Tracking Baseline section for more information. 0h = Normal baseline tracking for Channel 1 regardless of OUT2 status. 1h = Pauses baseline tracking for Channel 1 when OUT2 is asserted.
5	BTPAUSE1	R/W	0h	**Baseline Tracking Pause for Channel 1** Pauses baseline tracking for button algorithm for Channel 1 when OUT1 is asserted. Refer to Tracking Baseline section for more information. 0h = Normal baseline tracking for Channel 1 regardless of OUT1 status. 1h = Pauses baseline tracking for Channel 1 when OUT1 is asserted.
4	BTPAUSE0	R/W	0h	**Baseline Tracking Pause for Channel 0** Pauses baseline tracking for button algorithm for Channel 0 when OUT0 is asserted. Refer to Tracking Baseline section for more information. 0h = Normal baseline tracking for Channel 0 regardless of OUT0 status. 1h = Pauses baseline tracking for Channel 0 when OUT0 is asserted.
3	MAXWIN3	R/W	0h	**Max-Win Button Algorithm Setting for Channel 3** Refer to Resolving Simultaneous Button Presses (Max-Win) section for more information. 0h = Exclude Channel 3 from the max-win group 1h = Include Channel 3 in the max-win group
2	MAXWIN2	R/W	0h	**Max-Win Button Algorithm Setting for Channel 2** Refer to Resolving Simultaneous Button Presses (Max-Win) section for more information. 0h = Exclude Channel 2 from the max-win group 1h = Include Channel 2 in the max-win group
1	MAXWIN1	R/W	0h	**Max-Win Button Algorithm Setting for Channel 1** Refer to Resolving Simultaneous Button Presses (Max-Win) section for more information. 0h = Exclude Channel 1 from the max-win group 1h = Include Channel 1 in the max-win group
0	MAXWIN0	R/W	0h	**Max-Win Button Algorithm Setting for Channel 0** Refer to Resolving Simultaneous Button Presses (Max-Win) section for more information. 0h = Exclude Channel 0 from the max-win group 1h = Include Channel 0 in the max-win group

7.5.1.23 LC_DIVIDER Register (Offset = 17h) [Reset = 03h]

LC_DIVIDER is shown in LC_DIVIDER Register Field Descriptions.

Return to the LDC3114 Registers.

LC oscillation frequency divider

表 7-25. LC_DIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved

表 7-25. LC_DIVIDER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LCDIV	R/W	3h	**LC Oscillation Frequency Divider** The frequency divider sets the button sampling window in conjunction with SENCYCn

7.5.1.24 HYST Register (Offset = 18h) [Reset = 08h]

HYST is shown in HYST Register Field Descriptions.

Return to the LDC3114 Registers.

Hysteresis for threshold for button algorithm

表 7-26. HYST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved
3-0	HYST	R/W	8h	**Hysteresis** Defines the hysteresis for button triggering threshold. Hysteresis = HYST ´ 4 Refer to Setting Button Triggering Threshold section for more information.

7.5.1.25 TWIST Register (Offset = 19h) [Reset = 00h]

TWIST is shown in TWIST Register Field Descriptions.

Return to the LDC3114 Registers.

Anti-twist for button algorithm

表 7-27. TWIST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2-0	ANTITWIST	R/W	0h	**Anti-Twist** When set to 0, the anti-twist for button algorithm is not enabled. When greater than 0, all buttons are enabled for the anti-twist button algorithm. The validation of all buttons is void if any button 's BTN_DATA is negative by a threshold. Anti-twist Threshold = ANTITWIST × 4. Refer to Overcoming Case Twisting (Anti-Twist) section for more information.

7.5.1.26 COMMON_DEFORM Register (Offset = 1Ah) [Reset = 00h]

COMMON_DEFORM is shown in COMMON_DEFORM Register Field Descriptions.

Return to the LDC3114 Registers.

Anti-common and anti-deformation for button algorithm

表 7-28. COMMON_DEFORM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ANTICOM3	R/W	0h	**Anti-Common Button Algorithm Setting for Channel 3** Refer to Eliminating Common-Mode Change (Anti-Common) section for more information. 0h = Exclude Channel 3 from the anti-common group. 1h = Include Channel 3 in the anti-common group.

表 7-28. COMMON_DEFORM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ANTICOM2	R/W	0h	**Anti-Common Button Algorithm Setting for Channel 2** Refer to Eliminating Common-Mode Change (Anti-Common) section for more information. 0h = Exclude Channel 2 from the anti-common group. 1h = Include Channel 2 in the anti-common group.
5	ANTICOM1	R/W	0h	**Anti-Common Button Algorithm Setting for Channel 1** Refer to Eliminating Common-Mode Change (Anti-Common) section for more information. 0h = Exclude Channel 1 from the anti-common group. 1h = Include Channel 1 in the anti-common group.
4	ANTICOM0	R/W	0h	**Anti-Common Button Algorithm Setting for Channel 0** Refer to Eliminating Common-Mode Change (Anti-Common) section for more information. 0h = Exclude Channel 0 from the anti-common group. 1h = Include Channel 0 in the anti-common group.
3	ANTIDFORM3	R/W	0h	**Anti-Deform Button Algorithm Setting for Channel 3** Refer to Mitigating Metal Deformation (Anti-Deform) section for more information. 0h = Exclude Channel 3 from the anti-deform group. 1h = Include Channel 3 in the anti-deform group.
2	ANTIDFORM2	R/W	0h	**Anti-Deform Button Algorithm Setting for Channel 2** Refer to Mitigating Metal Deformation (Anti-Deform) section for more information. 0h = Exclude Channel 2 from the anti-deform group. 1h = Include Channel 2 in the anti-deform group.
1	ANTIDFORM1	R/W	0h	**Anti-Deform Button Algorithm Setting for Channel 1** Refer to Mitigating Metal Deformation (Anti-Deform) section for more information. 0h = Exclude Channel 1 from the anti-deform group. 1h = Include Channel 1 in the anti-deform group.
0	ANTIDFORM0	R/W	0h	**Anti-Deform Button Algorithm Setting for Channel 0** Refer to Mitigating Metal Deformation (Anti-Deform) section for more information. 0h = Exclude Channel 0 from the anti-deform group. 1h = Include Channel 0 in the anti-deform group.

7.5.1.27 OPOL_DPOL Register (Offset = 1Ch) [Reset = 0Fh]

OPOL_DPOL is shown in OPOL_DPOL Register Field Descriptions.

Return to the LDC3114 Registers.

Output polarity for button data and output

表 7-29. OPOL_DPOL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OPOL3	R/W	0h	**Button Output Polarity for OUT3 Pin** 0h = Active low (Default) 1h = Active high
6	OPOL2	R/W	0h	**Button Output Polarity for OUT2 Pin** 0h = Active low (Default) 1h = Active high
5	OPOL1	R/W	0h	**Button Output Polarity for OUT1 Pin** 0h = Active low (Default) 1h = Active high

表 7-29. OPOL_DPOL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	OPOL0	R/W	0h	**Button Output Polarity for OUT0 Pin** 0h = Active low (Default) 1h = Active high
3	DPOL3	R/W	1h	**Processed Button Algorithm Data Polarity for Channel 3** 0h = BTN_DATA3 decreases as fSENSOR3 increases 1h = DATA3 increases as fSENSOR3 increases.
2	DPOL2	R/W	1h	**Processed Button Algorithm Data Polarity for Channel 2** 0h = BTN_DATA2 decreases as fSENSOR2 increases 1h = DATA2 increases as fSENSOR2 increases.
1	DPOL1	R/W	1h	**Processed Button Algorithm Data Polarity for Channel 1** 0h = BTN_DATA1 decreases as fSENSOR1 increases 1h = DATA1 increases as fSENSOR1 increases.
0	DPOL0	R/W	1h	**Processed Button Algorithm Data Polarity for Channel 0** 0h = BTN_DATA0 decreases as fSENSOR0 increases 1h = DATA0 increases as fSENSOR0 increases.

7.5.1.28 CNTSC Register (Offset = 1Eh) [Reset = 55h]

CNTSC is shown in CNTSC Register Field Descriptions.

Return to the LDC3114 Registers.

Counter scale

表 7-30. CNTSC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CNTSC3	R/W	1h	**Counter Scale for Channel 3** Refer to Scaling Frequency Counter Output section for more information. 0h = CNTSC3 is 0 1h = CNTSC3 is 1 2h = CNTSC3 is 2 3h = CNTSC3 is 3
5-4	CNTSC2	R/W	1h	**Counter Scale for Channel 2** Refer to Scaling Frequency Counter Output section for more information. 0h = CNTSC2 is 0 1h = CNTSC2 is 1 2h = CNTSC2 is 2 3h = CNTSC2 is 3
3-2	CNTSC1	R/W	1h	**Counter Scale for Channel 1** Refer to Scaling Frequency Counter Output section for more information. 0h = CNTSC1 is 0 1h = CNTSC1 is 1 2h = CNTSC1 is 2 3h = CNTSC1 is 3

表 7-30. CNTSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	CNTSC0	R/W	1h	**Counter Scale for Channel 0** Refer to Scaling Frequency Counter Output section for more information. 0h = CNTSC0 is 0 1h = CNTSC0 is 1 2h = CNTSC0 is 2 3h = CNTSC0 is 3

7.5.1.29 SENSOR0_CONFIG Register (Offset = 20h) [Reset = 04h]

SENSOR0_CONFIG is shown in SENSOR0_CONFIG Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 0 cycle count, frequency, RP range

表 7-31. SENSOR0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RP0	R/W	0h	**Channel 0 Sensor Rp Range Select** Set based on the actual sensor Rp physical parameter. Refer to Designing Sensor Parameters section for more information. 0h = 50 Ω ≤ Rp ≤ 4 kΩ (Default) 1h = 800 Ω ≤ Rp ≤ 10 kΩ
6-5	FREQ0	R/W	0h	**Channel 0 Sensor Frequency Range Select** Refer to Designing Sensor Parameterssection for more information. 0h = 1 MHz to 3.3 MHz 1h = 3.3 MHz to 10 MHz 2h = 10 MHz to 30 MHz 3h = Reserved
4-0	SENCYC0	R/W	4h	**Channel 0 Sensor Cycle Count** SENCYC0 sets the Channel 0 button sampling window in conjunction with LCDIV. Refer to Programming Button Sampling Window section for more information.

7.5.1.30 SENSOR1_CONFIG Register (Offset = 22h) [Reset = 04h]

SENSOR1_CONFIG is shown in SENSOR1_CONFIG Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 1 cycle count, frequency, RP range

表 7-32. SENSOR1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RP1	R/W	0h	**Channel 1 Sensor Rp Range Select** Set based on the actual sensor Rp physical parameter. Refer to Designing Sensor Parameters section for more information. 0h = 50 Ω ≤ Rp ≤ 4 kΩ (Default) 1h = 800 Ω ≤ Rp ≤ 10 kΩ
6-5	FREQ1	R/W	0h	**Channel 1 Sensor Frequency Range Select** Refer to Designing Sensor Parameterssection for more information. 0h = 1 MHz to 3.3 MHz 1h = 3.3 MHz to 10 MHz 2h = 10 MHz to 30 MHz 3h = Reserved

表 7-32. SENSOR1_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	SENCYC1	R/W	4h	**Channel 1 Sensor Cycle Count** SENCYC1 sets the Channel 1 button sampling window in conjunction with LCDIV. Refer to Programming Button Sampling Window section for more information.

7.5.1.31 SENSOR2_CONFIG Register (Offset = 24h) [Reset = 04h]

SENSOR2_CONFIG is shown in SENSOR2_CONFIG Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 2 cycle count, frequency, RP range

表 7-33. SENSOR2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RP2	R/W	0h	**Channel 2 Sensor Rp Range Select** Set based on the actual sensor Rp physical parameter. Refer to Designing Sensor Parameters section for more information. 0h = 50 Ω ≤ Rp ≤ 4 kΩ (Default) 1h = 800 Ω ≤ Rp ≤ 10 kΩ
6-5	FREQ2	R/W	0h	**Channel 2 Sensor Frequency Range Select** Refer to Designing Sensor Parameterssection for more information. 0h = 1 MHz to 3.3 MHz 1h = 3.3 MHz to 10 MHz 2h = 10 MHz to 30 MHz 3h = Reserved
4-0	SENCYC2	R/W	4h	**Channel 2 Sensor Cycle Count** SENCYC2 sets the Channel 2 button sampling window in conjunction with LCDIV. Refer to Programming Button Sampling Window section for more information.

7.5.1.32 FTF0 Register (Offset = 25h) [Reset = DAh]

FTF0 is shown in FTF0 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 0 fast tracking factor for button algorithm

表 7-34. FTF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	1Bh	Reserved
2-1	FTF0	R/W	1h	**Fast Tracking Factor for Channel 0** Defines baseline tracking for button algorithm speed for negative values of DATA0. Refer to Tracking Baseline section for more information. 0h = FTF0 is 0 1h = FTF0 is 1 2h = FTF0 is 2 3h = FTF0 is 3
0	RESERVED	R/W	0h	Reserved

7.5.1.33 SENSOR3_CONFIG Register (Offset = 26h) [Reset = 04h]

SENSOR3_CONFIG is shown in SENSOR3_CONFIG Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor3 cycle count, frequency, RP range

表 7-35. SENSOR3_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RP3	R/W	0h	**Channel 3 Sensor Rp Range Select** Set based on the actual sensor Rp physical parameter. Refer to Designing Sensor Parameters section for more information. 0h = 50 Ω ≤ Rp ≤ 4 kΩ (Default) 1h = 800 Ω ≤ Rp ≤ 10 kΩ
6-5	FREQ3	R/W	0h	**Channel 3 Sensor Frequency Range Select** Refer to Designing Sensor Parameters section for more information. 0h = 1 MHz to 3.3 MHz 1h = 3.3 MHz to 10 MHz 2h = 10 MHz to 30 MHz 3h = Reserved
4-0	SENCYC3	R/W	4h	**Channel 3 Sensor Cycle Count** SENCYC3 sets the Channel 3 button sampling window in conjunction with LCDIV. Refer to Programming Button Sampling Window section for more information.

7.5.1.34 FTF1_2 Register (Offset = 28h) [Reset = 50h]

FTF1_2 is shown in FTF1_2 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensors 1 and 2 fast tracking factors for button algorithm

表 7-36. FTF1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FTF2	R/W	1h	**Fast Tracking Factor for Channel 2** Defines baseline tracking for button algorithm speed for negative values of DATA2. Refer to Tracking Baseline section for more information. 0h = FTF2 is 0 1h = FTF2 is 1 2h = FTF2 is 2 3h = FTF2 is 3
5-4	FTF1	R/W	1h	**Fast Tracking Factor for Channel 0** Defines baseline tracking for button algorithm speed for negative values of DATA1. Refer to Tracking Baseline section for more information. 0h = FTF1 is 0 1h = FTF1 is 1 2h = FTF1 is 2 3h = FTF1 is 3
3-0	RESERVED	R/W	0h	Reserved

7.5.1.35 FTF3 Register (Offset = 2Bh) [Reset = 01h]

FTF3 is shown in FTF3 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 3 fast tracking factor for button algorithm

表 7-37. FTF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	Reserved
1-0	FTF3	R/W	1h	**Fast Tracking Factor for Channel 3** Defines baseline tracking for button algorithm speed for negative values of DATA3. Refer to Tracking Baseline section for more information. 0h = FTF3 is 0 1h = FTF3 is 1 2h = FTF3 is 2 3h = FTF3 is 3

7.5.1.36 RAW_DATA0_3 Register (Offset = 59h) [Reset = 00h]

RAW_DATA0_3 is shown in RAW_DATA0_3 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 0 pre-processed raw data

表 7-38. RAW_DATA0_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA0[7:0]	R	0h	Sensor 0 pre-processed raw data

7.5.1.37 RAW_DATA0_2 Register (Offset = 5Ah) [Reset = 00h]

RAW_DATA0_2 is shown in RAW_DATA0_2 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 0 pre-processed raw data

表 7-39. RAW_DATA0_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA0[15:8]	R	0h	Sensor 0 pre-processed raw data

7.5.1.38 RAW_DATA0_1 Register (Offset = 5Bh) [Reset = 00h]

RAW_DATA0_1 is shown in RAW_DATA0_1 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 0 pre-processed raw data

表 7-40. RAW_DATA0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA0[23:16]	R	0h	Sensor 0 pre-processed raw data

7.5.1.39 RAW_DATA1_3 Register (Offset = 5Ch) [Reset = 00h]

RAW_DATA1_3 is shown in RAW_DATA1_3 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 1 pre-processed raw data

表 7-41. RAW_DATA1_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA1[7:0]	R	0h	Sensor 1 pre-processed raw data

7.5.1.40 RAW_DATA1_2 Register (Offset = 5Dh) [Reset = 00h]

RAW_DATA1_2 is shown in RAW_DATA1_2 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 1 pre-processed raw data

表 7-42. RAW_DATA1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA1[15:8]	R	0h	Sensor 1 pre-processed raw data

7.5.1.41 RAW_DATA1_1 Register (Offset = 5Eh) [Reset = 00h]

RAW_DATA1_1 is shown in RAW_DATA1_1 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 1 pre-processed raw data

表 7-43. RAW_DATA1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA1[23:16]	R	0h	Sensor 1 pre-processed raw data

7.5.1.42 RAW_DATA2_3 Register (Offset = 5Fh) [Reset = 00h]

RAW_DATA2_3 is shown in RAW_DATA2_3 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 2 pre-processed raw data

表 7-44. RAW_DATA2_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA2[7:0]	R	0h	Sensor 2 pre-processed raw data

7.5.1.43 RAW_DATA2_2 Register (Offset = 60h) [Reset = 00h]

RAW_DATA2_2 is shown in RAW_DATA2_2 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 2 pre-processed raw data

表 7-45. RAW_DATA2_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA2[15:8]	R	0h	Sensor 2 pre-processed raw data

7.5.1.44 RAW_DATA2_1 Register (Offset = 61h) [Reset = 00h]

RAW_DATA2_1 is shown in RAW_DATA2_1 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 2 pre-processed raw data

表 7-46. RAW_DATA2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA2[23:16]	R	0h	Sensor 2 pre-processed raw data

7.5.1.45 RAW_DATA3_3 Register (Offset = 62h) [Reset = 00h]

RAW_DATA3_3 is shown in RAW_DATA3_3 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 3 pre-processed raw data

表 7-47. RAW_DATA3_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA3[7:0]	R	0h	Sensor 3 pre-processed raw data

7.5.1.46 RAW_DATA3_2 Register (Offset = 63h) [Reset = 00h]

RAW_DATA3_2 is shown in RAW_DATA3_2 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 3 pre-processed raw data

表 7-48. RAW_DATA3_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA3[15:8]	R	0h	Sensor 3 pre-processed raw data

7.5.1.47 RAW_DATA3_1 Register (Offset = 64h) [Reset = 00h]

RAW_DATA3_1 is shown in RAW_DATA3_1 Register Field Descriptions.

Return to the LDC3114 Registers.

Sensor 3 pre-processed raw data

表 7-49. RAW_DATA3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAW_DATA3[23:16]	R	0h	Sensor 3 pre-processed raw data

7.5.1.48 MANUFACTURER_ID_LSB Register (Offset = FCh) [Reset = 49h]

MANUFACTURER_ID_LSB is shown in MANUFACTURER_ID_LSB Register Field Descriptions.

Return to the LDC3114 Registers.

Manufacturer ID lower byte

表 7-50. MANUFACTURER_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MANUFACTURER_ID_[7:0]	R	49h	**Manufacturer ID [7:0]**

7.5.1.49 MANUFACTURER_ID_MSB Register (Offset = FDh) [Reset = 54h]

MANUFACTURER_ID_MSB is shown in MANUFACTURER_ID_MSB Register Field Descriptions.

Return to the LDC3114 Registers.

Manufacturer ID upper byte

表 7-51. MANUFACTURER_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MANUFACTURER_ID_[15:8]	R	54h	**Manufacturer ID [15:8]**

7.5.1.50 DEVICE_ID_LSB Register (Offset = FEh) [Reset = 00h]

DEVICE_ID_LSB is shown in DEVICE_ID_LSB Register Field Descriptions.

Return to the LDC3114 Registers.

Device ID lower byte

表 7-52. DEVICE_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID_[7:0]	R	0h	**Device ID [7:0]**

7.5.1.51 DEVICE_ID_MSB Register (Offset = FFh) [Reset = 40h]

DEVICE_ID_MSB is shown in DEVICE_ID_MSB Register Field Descriptions.

Return to the LDC3114 Registers.

Device ID upper byte

表 7-53. DEVICE_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID_[15:8]	R	40h	**Device ID [15:8]**

7.5.2 Gain Table for Registers GAIN0, GAIN1, GAIN2, and GAIN3

表 7-54. GAIN*n* Bit Values in Decimal and Corresponding Normalized Gain Factors

BIT VALUE IN DECIMAL	NORMALIZED GAIN FACTOR	BIT VALUE IN DECIMAL	NORMALIZED GAIN FACTOR
0	1.0	32	16
1	1.0625	33	17
2	1.1875	34	19
3	1.3125	35	21
4	1.4375	36	23
5	1.5625	37	25
6	1.6875	38	27
7	1.8125	39	29
8	2.0	40	32
9	2.125	41	34
10	2.375	42	38
11	2.625	43	42
12	2.875	44	46
13	3.125	45	50
14	3.375	46	54
15	3.625	47	58
16	4.0	48	64
17	4.25	49	68
18	4.75	50	76
19	5.25	51	84
20	5.75	52	92
21	6.25	53	100
22	6.75	54	108
23	7.25	55	116
24	8.0	56	128
25	8.5	57	136
26	9.5	58	152
27	10.5	59	168
28	11.5	60	184
29	12.5	61	200
30	13.5	62	216
31	14.5	63	232

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The LDC3114-Q1 supports multiple buttons. Each button can be configured in various ways for optimal operation.

8.1.1 Theory of Operation

An AC current flowing through an inductor will generate an AC magnetic field. If a conductive material, such as a metal object, is in close proximity to the inductor, the magnetic field will induce circulating eddy currents on the surface of the conductor. The eddy currents are a function of the distance, size, and composition of the conductor. If the conductor is deflected toward the inductor as shown in 图 8-1, more eddy currents will be generated.

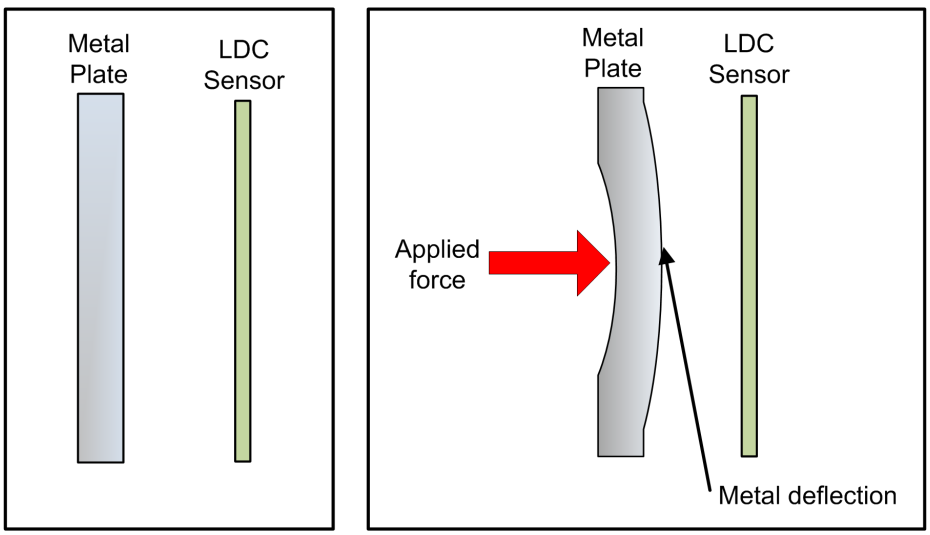


图 8-1. Metal Deflection

The eddy currents create their own magnetic field, which opposes the original field generated by the inductor. This effect reduces the effective inductance of the system, resulting in an increase in sensor frequency. 图 8-2 shows the inductance and frequency response of an example sensor with a diameter of 14 mm. As the sensitivity of an inductive sensor increases with closer targets, the conductive plate should be placed quite close to the sensor—typically 10% of the sensor diameter for circular coils. For rectangular or race-track-shaped coils, the target to sensor distance should typically be less than 10% of the shorter side of the coil.

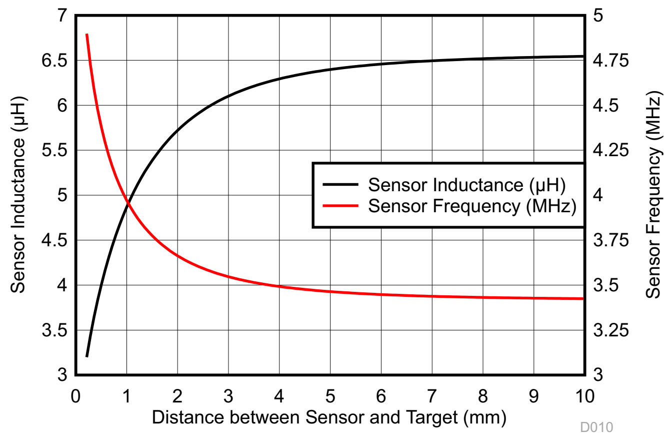


图 8-2. Sensor Inductance and Frequency vs. Target Distance. Sensor Diameter = 14 mm

The output DATA*n* registers (Addresses 0x02 through 0x09) of the LDC3114-Q1 contain the processed values of the changes in sensor frequencies.

8.1.2 Designing Sensor Parameters

图 8-3 shows that each inductive touch button uses an LC resonator sensor, where L is the inductor, C is the capacitor, and R_S is the AC series resistance of the sensor at the frequency of operation. The key parameters of the LC sensor include frequency, effective parallel resistance R_P, and quality factor Q. These parameters must be within the ranges as specified in the *Sensor* section of the *Electrical Characteristics* table. Note that the effective R_P and Q changes when the conductive target is in place.

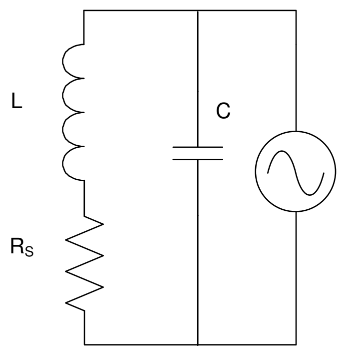


图 8-3. LC Resonator

The LC sensor frequency defined in 方程式 3 must be between 1 MHz and 30 MHz. For optimal performance, configure the sensor frequency to be greater than 3 MHz.

$$f_{SENSOR} = \frac{1}{2\pi\sqrt{LC}} \tag{3}$$

The sensor quality factor defined in 方程式 4 must be between 5 and 30.

$$Q_{SENSOR} = \frac{1}{R_S}\sqrt{\frac{L}{C}} \tag{4}$$

The series resistance defined in 方程式 5 can be represented as an equivalent parallel resistance, R_P.

$$R_P = \frac{L}{R_S C} \tag{5}$$

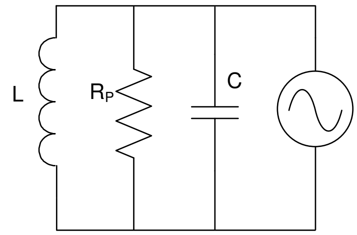


图 8-4. Equivalent Parallel Circuit

R_P can be viewed as the load on the sensor driver. This load corresponds to the current drive required to maintain the oscillation amplitude. R_P must be between 350 Ω and 10 kΩ.

In summary, the LDC3114-Q1 requires that the sensor parameters are within the following ranges when the conductive target is present:

- $1\ \text{MHz} \leqslant f_{SENSOR} \leqslant 30\ \text{MHz}$
- $5 \leqslant Q \leqslant 30$
- $350\ \Omega \leqslant R_P \leqslant 10\ \text{k}\Omega$

8.1.3 Setting COM Pin Capacitor

The COM pin requires a bypass capacitor to ground. The capacitor should be a low-ESL, low-ESR type. C_{COM} must be sized so that the following relationship is valid for all channels.

$$100 \times C_{SENSORn} / Q_{SENSORn} < C_{COM} < 1250 \times C_{SENSORn} / Q_{SENSORn} \quad (6)$$

The value of $Q_{SENSORn}$ when the sensor is at the minimum target distance should be used. The maximum acceptable value for C_{COM} is 20 nF. The C_{COM} range for a particular sensor configuration can be obtained with the Spiral_Inductor_Designer tab of the *LDC Calculations Tool*.

8.1.4 Defining Power-On Timing

The low power architecture of the LDC3114-Q1 makes it possible for the device to be active all the time. When not being used, the LDC3114-Q1 can operate in Low Power Mode with a single standby power button, which typically consumes less than 10 µA. If additional power-saving is desired, or in the rare event where a power-on reset becomes necessary (see *I²C Interface*), the output data will become ready after 50-ms start-up time, about 1-ms optional register loading time, and two sampling windows for all active channels. 图 8-5 shows the power-on timing of the LDC3114-Q1.

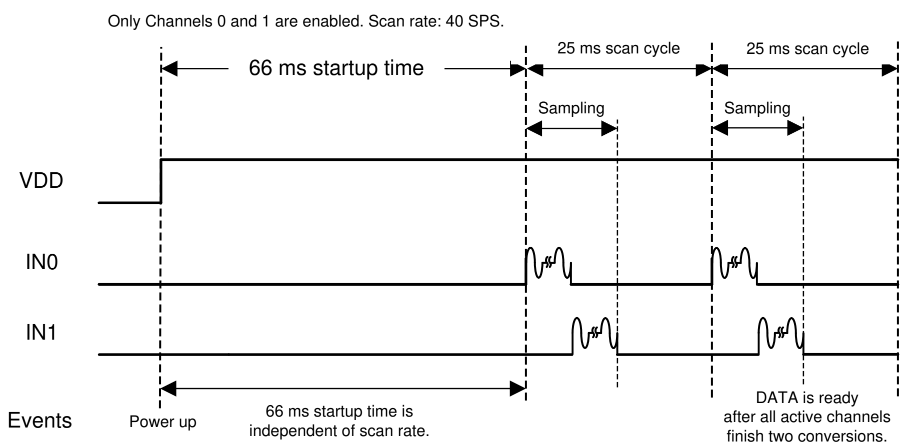


图 8-5. Power-On Timing

8.1.5 Configuring Button or Raw Data Scan Rate

The LDC3114-Q1 periodically samples all active channels at the selected scan rate. The device can operate at eight different scan rates to meet various power consumption requirements, where a lower scan rate achieves lower power consumption.

In Normal Power Mode, the scan rate can be programmed to 80, 40, 20, or 10 SPS through *Register NP_SCAN_RATE (Address 0x0D)*. Additionally through NPFSR bit field in the same register 160 SPS rate can be enabled which overrides the setting of *NPSR* but not the *NPCS* bit fields. The *NPCS* bit field allows to set the part in continuous sampling mode in Normal Power Mode only. When *NPCS* is set then the settings for NPSR and NPFSR are ignored.

In Low Power Mode, the scan rate can be programmed to 5, 2.5, 1.25, or 0.625 SPS through *Register LP_SCAN_RATE (Address 0x0F)*. The mode is selected by setting the LPWRB pin to VDD (Normal Power) or ground (Low Power). In either mode, each button can be independently enabled through a bit in *Register EN (Address 0x0C)*. 图 6-9 shows the typical distribution of the scan rates.

表 8-1. Scan Rates

SCAN RATE (SPS)	LPSR (0x0F) SETTING	NPSR (0x0D) SETTING	NPCS (0x0D) SETTING	NPFSR (0x0D) SETTING	LPWRB PIN SETTING
0.625	b11	Not Applicable	Not Applicable	Not Applicable	Ground
1.25	b10	Not Applicable	Not Applicable	Not Applicable	Ground
2.5	b01	Not Applicable	Not Applicable	Not Applicable	Ground
5	b00	Not Applicable	Not Applicable	Not Applicable	Ground
10	Not Applicable	b11	b0	b0	V_{DD}
20	Not Applicable	b10	b0	b0	V_{DD}
40	Not Applicable	b01	b0	b0	V_{DD}
80	Not Applicable	b00	b0	b0	V_{DD}
160	Not Applicable	Not Applicable	b0	b1	V_{DD}
Continuous	Not Applicable	Not Applicable	b1	Not Applicable	V_{DD}

8.1.6 Programming Button or Raw Data Sampling Window

The sampling window is the actual duration per scan cycle for active data sampling of the sensor frequency. It is programmed with the exponential parameter, LCDIV, in *Register LC_DIVIDER (Address 0x17)*, and the individual linear sensor cycle counter SENCYC*n* (*n* = 0, 1, 2, or 3) in Registers SENSOR*n*_CONFIG (*n* = 0, 1, 2, or 3, Addresses *0x20*, *0x22*, *0x24*, *0x26*). For most touch button applications, the button sampling window should be set to between 1 ms and 8 ms. For sampling rate of 160 SPS, the window has to be less than 6.25 ms. For continuous sampling, the data becomes available at the configured sampling window period rate. The recommended minimum sensor conversion time is 1 ms. Longer conversion time can be used to achieve better signal-to-noise ratio, if needed. The active channels in 图 8-6 will sample sequentially if multiple channels are enabled.

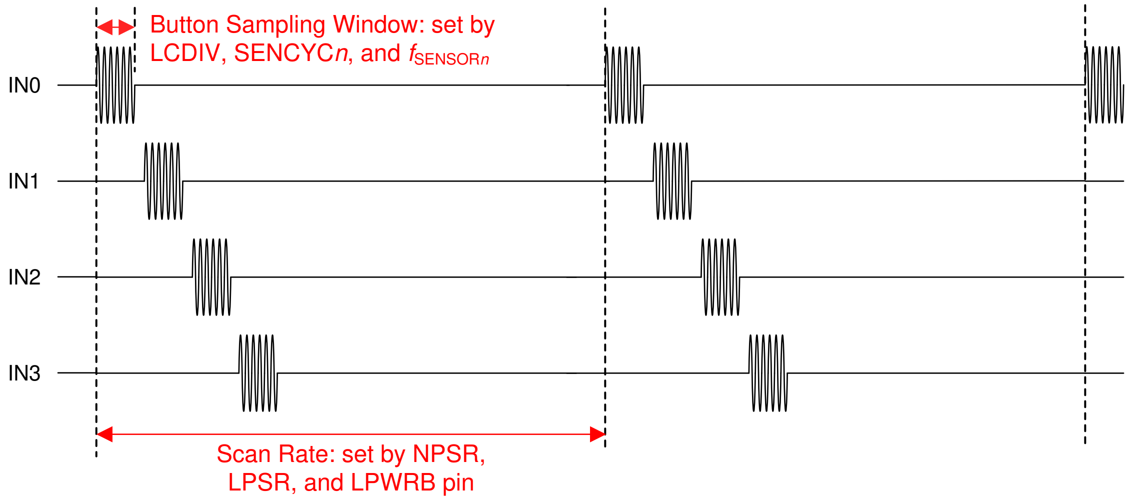


图 8-6. Configurable Scan Rate and Sampling Window

The LDC3114-Q1 is designed to work with LC resonator sensors with oscillation frequencies ranging from 1 MHz to 30 MHz. 方程式 7 calculates the exact definition of the sampling window.

$$\text{Button Sampling Window} = \frac{\text{Number of Sensor Oscillation Cycles}}{\text{Sensor Frequency}}$$

$$t_{SAMPLE} = \frac{128 \times (SENCYCn + 1) \times 2^{LCDIV}}{f_{SENSORn}}, n = 0, 1, 2, \text{ or } 3 \quad (7)$$

where:

- t_{SAMPLE} is the sampling window in µs
- SENCYC*n* and LCDIV are the linear and exponential scalers that set the number of sensor oscillation cycles
- $f_{SENSORn}$ is the sensor frequency in MHz

In 方程式 7, LCDIV (0 to 7, default 3) is the exponential LC divider that sets the approximate ranges for all channels, and SENCYC*n* (0 to 31, default 4) is the linear sensor cycle scaler that fine-tunes each individual channel. Together they set the number of sensor oscillation cycles used to determine the sampling window.

For example, if the LC sensor frequency is 9.2 MHz, and it is desirable to get 1-ms sampling window, then this can be achieved by setting SENCYC*n* = 17 and LCDIV = 2.

Alternatively, from the sampling window and sensor frequency, the LCDIV can be read off from LCDIV as a Function of Sensor Frequency and Button Sampling Window 图 8-7. For example, 1-ms sampling window and 9.2-MHz sensor frequency intersect in the region closest to where LCDIV = 2. Then SENCYC*n* can be calculated accordingly.

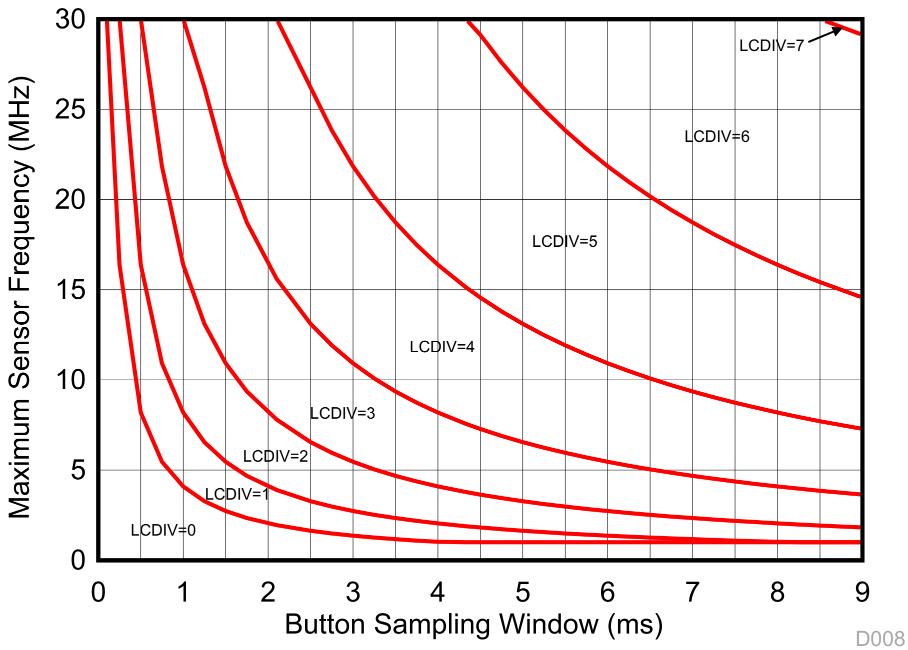


图 8-7. LCDIV as a Function of Sensor Frequency and Button Sampling Window

8.1.7 Scaling Frequency Counter Output

The LDC3114-Q1 requires this internal frequency counter scaler to be set based on the button sampling window to avoid data overflow. Use 方程式 8 to set the scaler in *Register CNTSC (Address 0x1E)*:

$$\text{CNTSC}n = \text{LCDIV} + \text{ceiling}\left(\log_2 \frac{0.0861 \times (\text{SENCYC}n + 1)}{f_{\text{SENSOR}n}}\right), (n = 0, 1, 2, \text{ or } 3) \quad (8)$$

where:

- CNTSC*n* is the internal frequency counter scaler
- SENCYC*n* and LCDIV are the linear and exponential scalers that set the number of sensor oscillation cycles
- $f_{\text{SENSOR}n}$ is the sensor frequency in MHz

8.1.8 Setting Button Triggering Threshold

Every material shows some hysteresis when the material deforms then returns to the original state. The amount of hysteresis is a function of material properties and physical parameters, such as size and thickness. This feature modifies the hysteresis of the button signal threshold according to different materials and various button shapes and sizes. Hysteresis can be programmed in *Register HYST (Address 0x18)*. By default, the button triggering hysteresis is set to 32. The nominal button triggering threshold is 128. With hysteresis, the effective on-threshold is 128 + 32 = 160. This means if the DATA*n* (*n* = 0, 1, 2, or 3) reaches 160, the LDC3114-Q1 considers that as a button press. When the DATA*n* decreases to 128 – 32 = 96, the LDC considers the button to be released.

$$\text{Threshold}_{\text{ON}} = 128 + \text{Hysteresis} \quad (9)$$

$$\text{Threshold}_{\text{OFF}} = 128 - \text{Hysteresis} \quad (10)$$

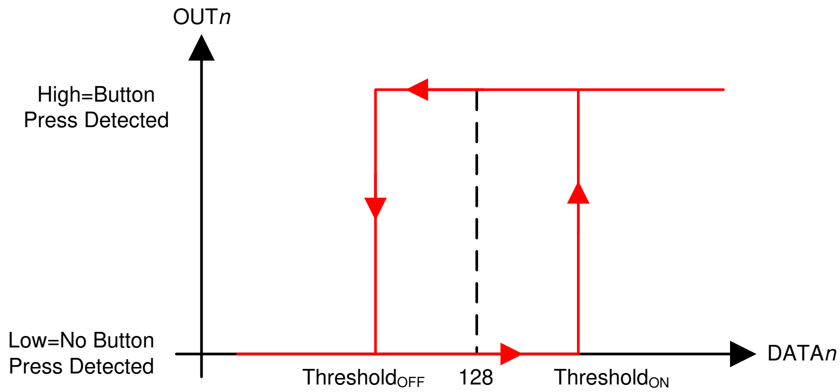


图 8-8. Button Triggering Threshold with Hysteresis. Output Polarity: Active High

8.1.9 Tracking Baseline

The LDC3114-Q1 automatically tracks slow changes in the baseline signal and compensates for environmental drifts and variations. The baseline tracking is only applicable for the button algorithm mode and not for raw data access mode. See *Multimode Operation* for details. In Normal Power Mode, use 方程式 11 to determine the effective baseline increment per scan cycle ($BINC_{NP}$):

$$BINC_{NP} = \frac{2^{NPBI}}{72} \tag{11}$$

where:

- NPBI is the Normal Power Baseline Increment index that can be configured in *Register NP_BASE_INC (Address 0x15)*

In Low Power Mode, use 方程式 12 to determine the effective baseline increment per scan cycle ($BINC_{LP}$):

$$BINC_{LP} = \frac{2^{LPBI}}{9} \tag{12}$$

where:

- LPBI the Low Power Baseline Increment index that can be configured in *Register LP_BASE_INC (Address 0x13)*

As a result of baseline tracking, a button press with a constant force only lasts for a finite amount of time. 方程式 13 defines the duration of a button press ($DATAn > Threshold_{ON}$).

$$\text{Duration of Button Press} = \frac{DATA\mathit{n} - Threshold_{OFF}}{BINC} \tag{13}$$

where:

- Duration of Button Press is the number of scan cycles that the channel is asserted
- DATA*n* is the button signal at the beginning of a press
- BINC is the baseline increment per scan cycle

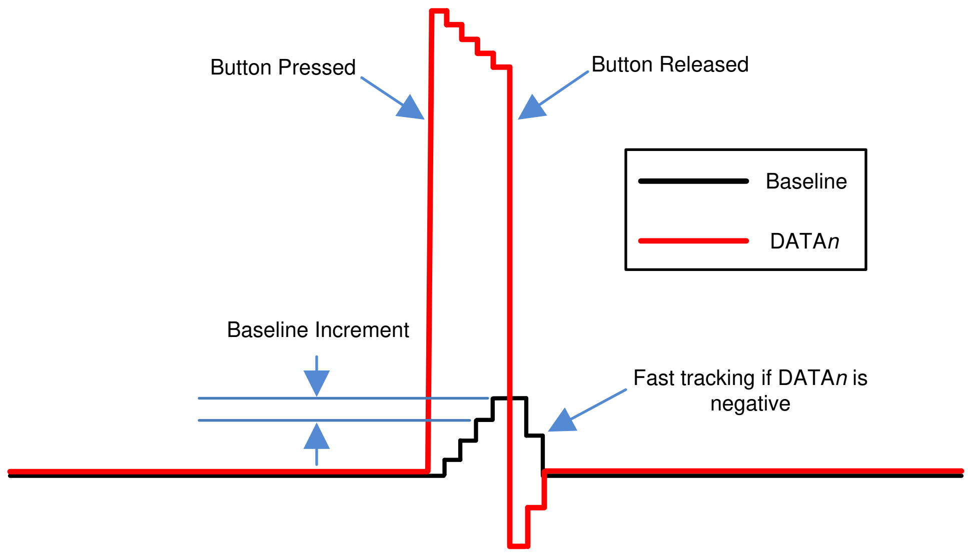


图 8-9. Baseline Tracking in the Presence of a Button Press

The baseline tracking for a particular channel can be paused when the channel output is asserted. This is achieved by setting the corresponding BTPAUSE bit in *Register BTPAUSE_MAXWIN (Address 0x16)* to b1.

If DATA*n* is negative, the tracking speed will be scaled by the fast tracking factor as specified in *Registers FTF0 (Address 0x25)* , *FTF1_2 (Address 0x28)*, or *FTF3 (Address 0x2B)*. 表 8-2 shows the scaling factors for various FTF*n* settings.

$$\text{BINC (DATA}n < 0) = \text{Fast\_Tracking\_Factor\_}n \times \text{BINC (DATA}n > 0) \tag{14}$$

表 8-2. Fast Tracking Factor Settings

FTF*n* Setting	Fast Tracking Factor
b00	1
b01	4
b10	8
b11	16

备注
When the continuous sampling rate using NPCS bit is set, the baseline tracking increment is a fixed value.

8.1.10 Mitigating False Button Detections

The LDC3114-Q1 offers several algorithms that can mitigate false button detections due to mechanical non-idealities associated with groups of buttons. These are listed below.

8.1.10.1 Eliminating Common-Mode Change (Anti-Common)

This algorithm eliminates false detection when a user presses the middle of two or more buttons, which could lead to a common-mode response on multiple buttons. All the buttons can be individually enabled to have this feature by programming *Register COMMON_DEFORM (Address 0x1A)*.

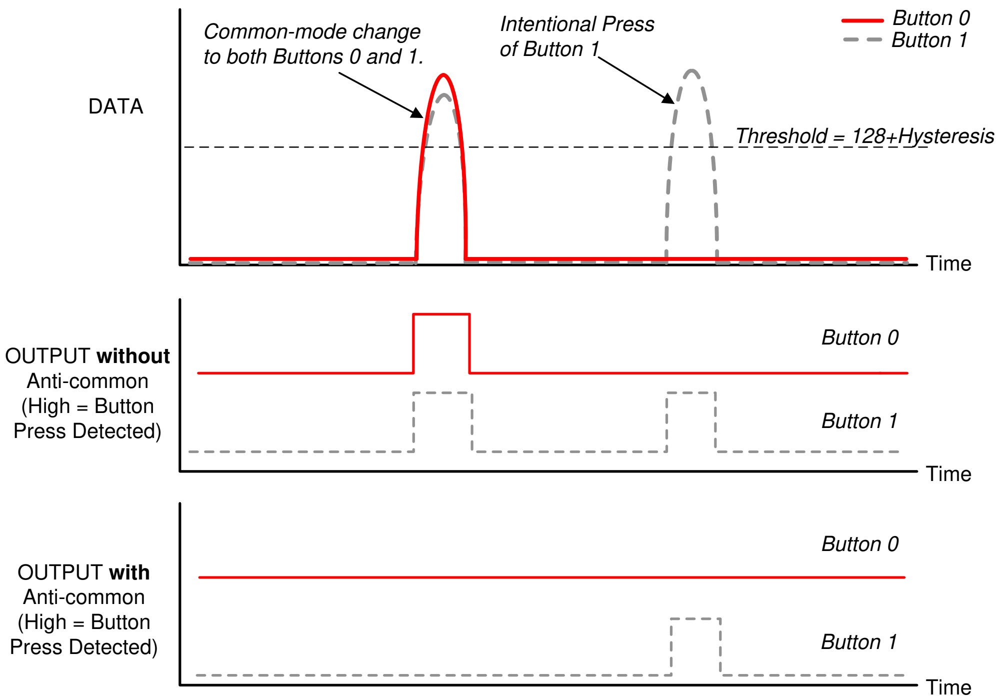


图 8-10. Illustration of the Anti-Common Feature

8.1.10.2 Resolving Simultaneous Button Presses (Max-Win)

This algorithm enables the system to select the button pressed with maximum force when multiple buttons are pressed at the same time. This could happen when two buttons are physically very close to each other, and pressing one causes a residual reaction on the other. Buttons can be individually enabled to join the “max-win” group by configuring *Register BTPAUSE_MAXWIN (Address 0x16)*.

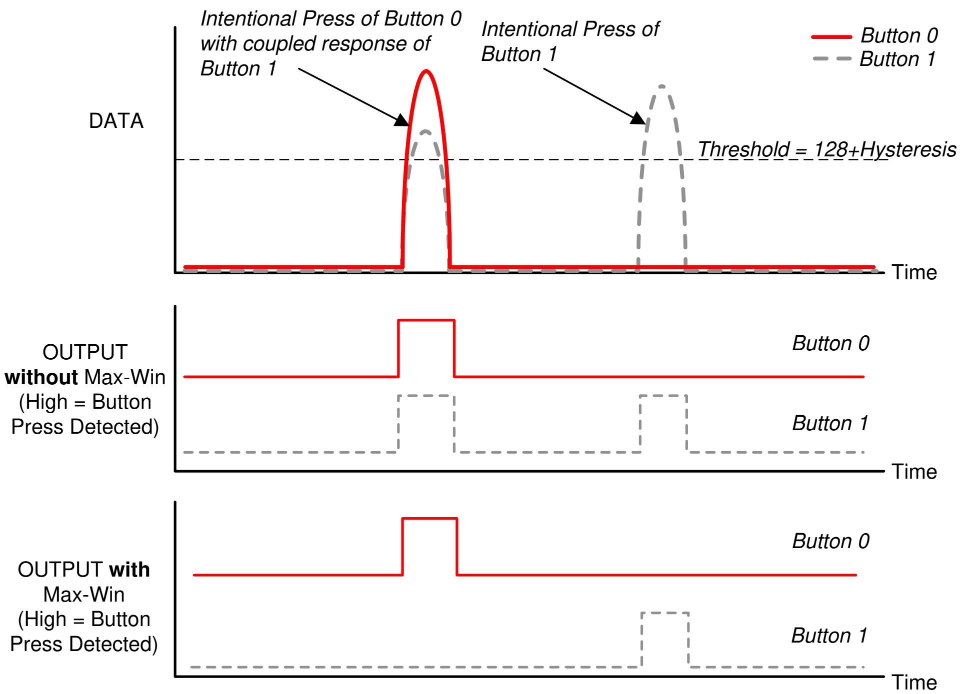


图 8-11. Illustration of the Max-Win Feature

8.1.10.3 Overcoming Case Twisting (Anti-Twist)

The anti-twist algorithm reduces the likelihood of false detection when the case is twisted, which could cause unintended mechanical activation of the buttons, or an opposite reaction in two adjacent buttons. When this algorithm is enabled, detection of button presses is suppressed if any button’s output data is negative by a configurable threshold. The anti-twist algorithm can be enabled by configuring *Register TWIST (Address 0x19)*.

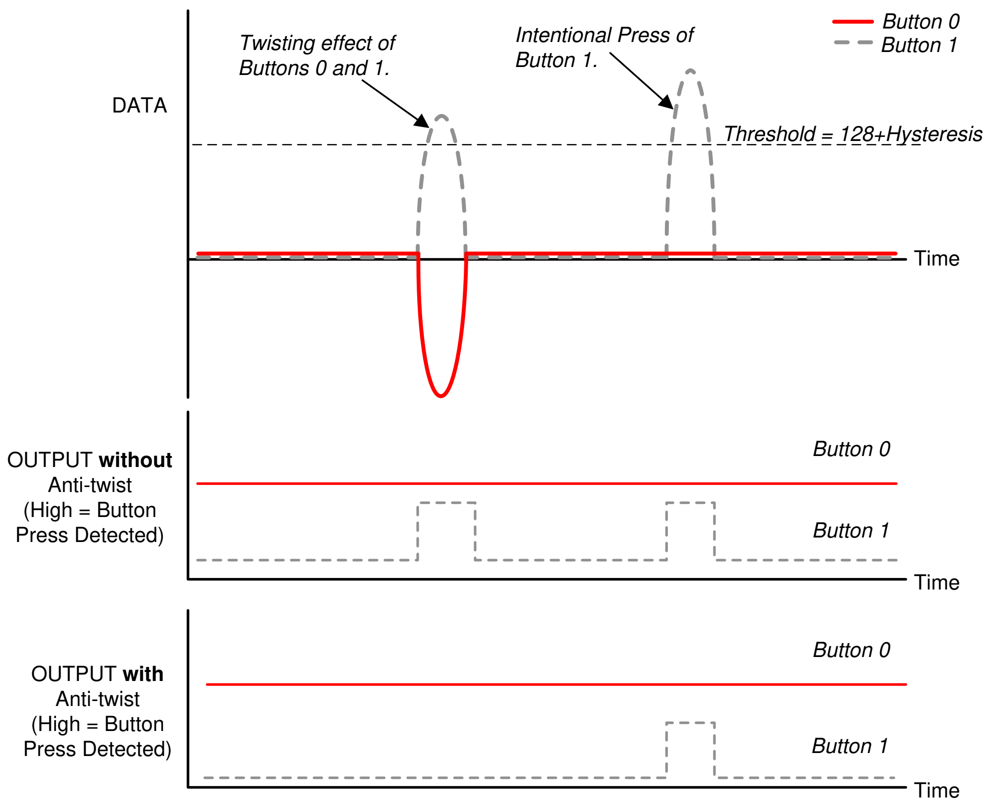


图 8-12. Illustration of the Anti-Twist Feature

8.1.10.4 Mitigating Metal Deformation (Anti-Deform)

This function filters changes due to metal deformation in the vicinity of one or more buttons. Such metal deformation can be accidentally caused by pressing a neighboring button that does not have sufficient mechanical isolation. The user can specify which buttons to join the anti-deform group by configuring *Register COMMON_DEFORM (Address 0x1A)*.

8.1.11 Reporting Interrupts for Button Presses, Raw Data Ready and Error Conditions

INTB, the LDC3114-Q1 interrupt pin, is asserted when a button press or an error condition occurs. The default polarity is active low and can be configured through *Register INTPOL (Address 0x11)*.

图 8-13 shows the LDC3114-Q1 response to a single button press on Channel 0. At the end of the button sampling window following a press of Button 0, the OUT0 pin and INTB pin are asserted. The OUT_STATUS bit changes from 0 to 1, and remains so until a read of the STATUS register clears it. The OUT*n* (*n* = 0, 1, 2, or 3) and INTB pins are asserted until the end of the button sampling window following the release of the button.

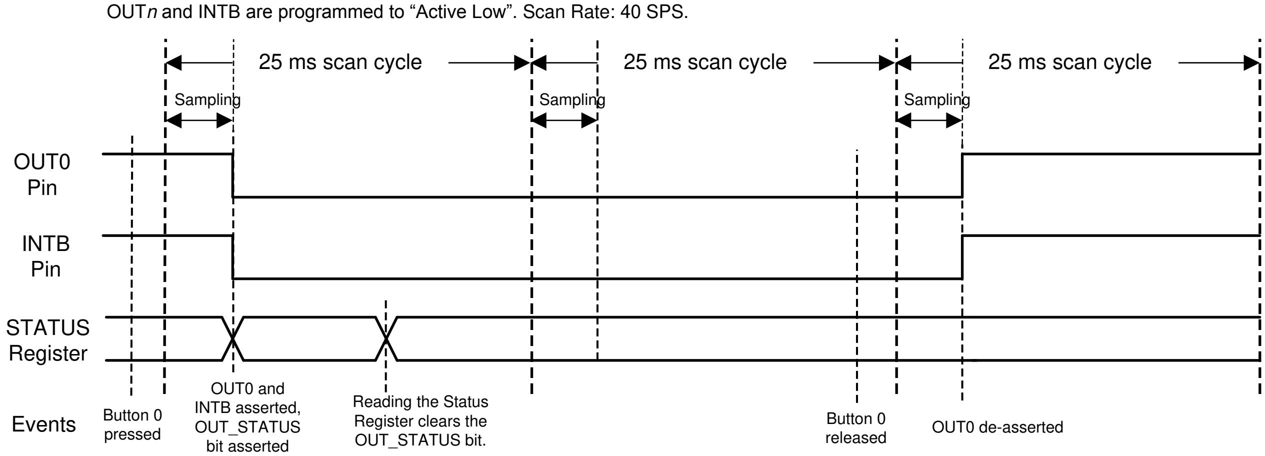


图 8-13. Timing Diagram of a Single Button Press

图 8-14 shows the LDC3114-Q1 response to multiple button presses. In this example, after Button 0 is pressed, the OUT0 pin is asserted. After that, Button 1 is also pressed, following which Button 0 is released. The OUT0 pin is de-asserted and OUT1 pin asserted at the end of the next button sampling window. The INTB pin remains continuously asserted as long as at least one of the buttons is pressed. The OUT_STATUS bit only changes from 0 to 1 after the first button assertion.

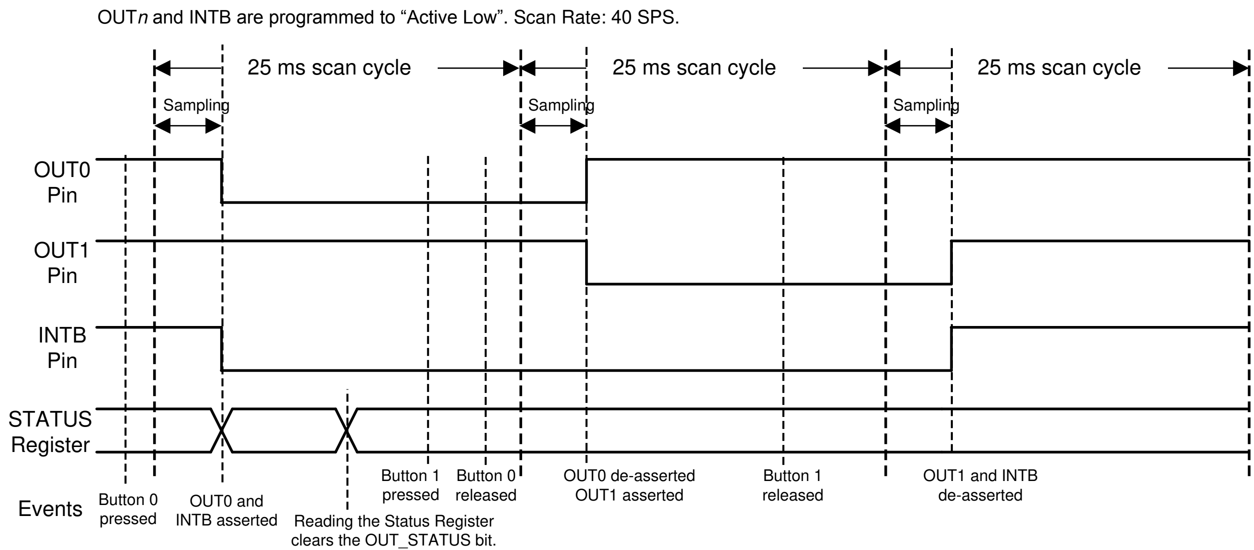


图 8-14. Timing Diagram of Multiple Button Presses

The INTB pin also reports any error event. If an error occurs, the INTB pin is asserted and the error is reported in the STATUS register (Address 0x00). Refer to the *Register Maps* section for possible error events.

For Raw data access mode, the OUTx pins are not used and INTB pin along with error is also used to assert when the sampling cycle is complete and data is available for all channels.

8.1.12 Estimating Supply Current

When the LDC3114-Q1 is active (in either Normal Power Mode or Low Power Mode), use 方程式 15 to determine the current:

$$I_{ACTIVEn} = 1.6 + \frac{12}{1 + 16 \times R_{Pn}{}^{1.21}} + 0.011 \times f_{SENSORn} \tag{15}$$

where

- $I_{ACTIVEn}$ is the supply current in mA during active sampling
- R_{Pn} is the sensor parallel resonant impedance in kΩ
- $f_{SENSORn}$ is the sensor frequency in MHz
- n is the channel index, that is, n = 0, 1, 2, or 3 for LDC3114-Q1

The LDC3114-Q1 is only actively sampling the enabled channels during a fraction of the scan window. 方程式 16 determines the average supply current:

$$I_{DD} = \frac{1}{t_{SCAN}} \times \left(\sum_{n} I_{ACTIVEn} \times t_{SAMPLEn} \right) + 0.005 \tag{16}$$

where

- I_{DD} is the average supply current in mA
- t_{SCAN} is the scan window (set by the scan rate) in ms
- $I_{ACTIVEn}$ is the supply current when the device is active as defined by 方程式 15
- t_{SAMPLE} is the button sampling window in ms

8.2 Typical Application

8.2.1 Touch Button Design

The low power architecture of LDC3114-Q1 makes them suitable for driving button sensors in consumer electronics, such as mobile phones. Most mobile phones today have three buttons along the edges, namely the power button, volume up, and volume down.

On a typical smartphone, the two volume buttons are next to each other, so they may be susceptible to false detections such as simultaneous button presses. To prevent such mis-triggers, they can be grouped together to take advantage of the various features that mitigate false detections as explained in *Mitigating False Button Detections*. For example, if Max-win is applied to the two volume buttons, only the one with the greater force will be triggered.

The inductive touch solution does not require any mechanical cutouts at the button locations. This can support reduced manufacturing cost for the phone case and enhance the case resistance to moisture, dust, and dirt. This is a great advantage compared to mechanical buttons in the market today.

图 8-15 shows a typical touch button application.

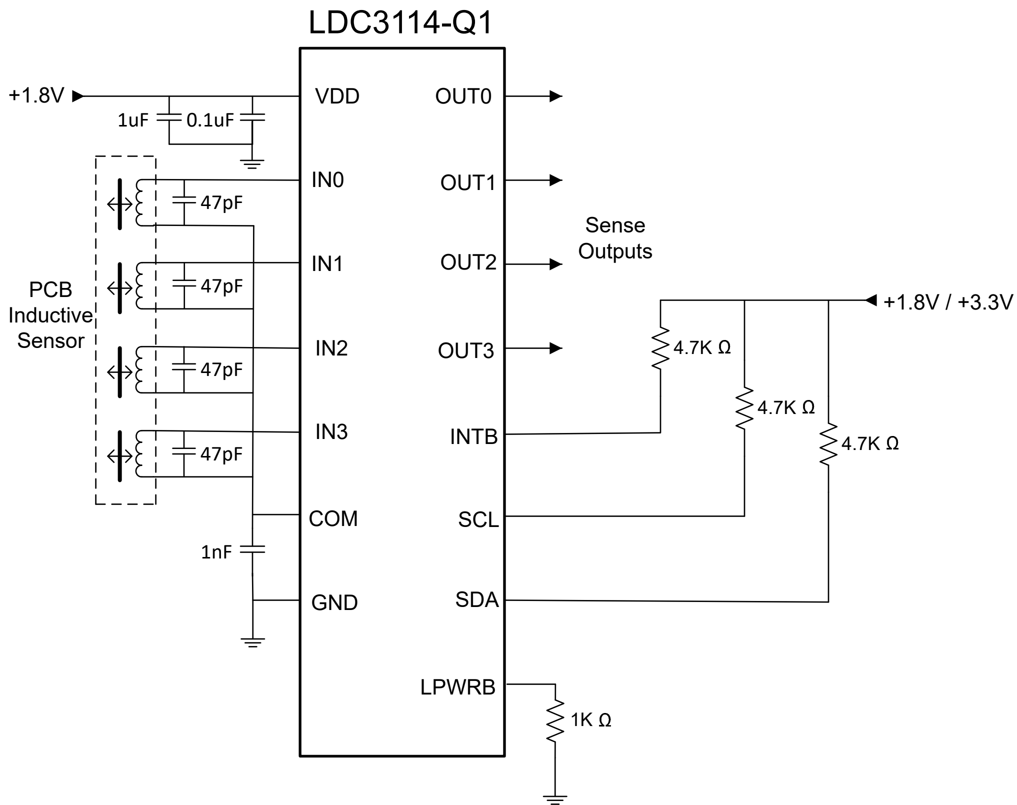


图 8-15. Application Schematic

8.2.1.1 Design Requirements

The sensor parameters, including frequency, R_P, and Q factor have to be within the design space of the LDC3114-Q1 as specified in the *Electrical Characteristics* table.

8.2.1.2 Detailed Design Procedure

The LDC3114-Q1 is a multichannel device. The italic *n* in the parameters below refers to the channel index:

1. Select system-based options:
   - Select Normal or Low Power Mode of operation by setting the LPWRB pin to V_{DD} or ground, respectively. Configure the enable bits for all channels in *Register EN (Address 0x0C)*.
   - Select the polarities of OUT*n* and INTB pins by configuring *Register OPOL_DPOL (Address 0x1C)* and *Register INTPOL (Address 0x11)*.
   - Configure the sensor frequency setting in Registers SENSOR*n*_CONFIG (Addresses *0x20*, *0x22*, *0x24*, *0x26*).
2. Choose the sampling rate (80, 40, 20, 10, 5, 2.5, 1.25, or 0.625 SPS) based on system power consumption requirement, and configure *Register NP_SCAN_RATE (Address 0x0D)* or *Register LP_SCAN_RATE (Address 0x0F)*.
3. Choose the button sampling window based on power consumption and noise requirements (recommended: 1 ms to 8 ms). While a longer button sampling window provides better noise performance, 1 ms is typically sufficient for most applications. Set SENCYC*n* and LCDIV in Registers SENSOR*n*_CONFIG (Addresses *0x20*, *0x22*, *0x24*, *0x26*) and *Register LC_DIVIDER (Address 0x17)* in the following steps:
   - Calculate LCDIV = ceiling ($\log_2 (f_{SENSORn} \times t_{SAMPLEn})$ – 12), where $f_{SENSORn}$ is the sensor frequency in MHz, $t_{SAMPLEn}$ is the button sampling window in µs.
   - If LCDIV < 0, set it to 0.
   - Adjust SENCYC*n* to get desired $t_{SAMPLEn}$ according to $t_{SAMPLEn} = 128 \times (SENCYCn + 1) \times 2^{LCDIV} / f_{SENSORn}$.

4. Calibrate gain in the appropriate Registers GAIN*n* (Addresses *0x0E*, *0x10*, *0x12*, *0x14*). The gain setting can be used to tune the sensitivity of the touch button. GAIN*n* is a 6-bit field with 64 different gain levels corresponding to normalized gains between 1 and 232. A good mechanical and sensor design typically requires a gain level of around 32 to 50, corresponding to relative gains of 16 to 76 (normalized to gain level of 0). Use the following sequence to determine the appropriate gain for each button:
   - Apply minimum desired force to the button.
   - Read initial DATA*n* value after the button press. Note that the baseline tracking will affect this value.
   - Calculate gain factor required to increase DATA*n* to the programmed threshold (default is 160).
   - Look up the *Gain Table* to find the required gain setting.
5. Enable special features to mitigate button interference if there is any, in Registers BTPAUSE_MAXWIN, TWIST, COMMON_DEFORM (Addresses *0x16*, *0x19*, *0x1A*).

For more information on inductive touch system design, including mechanical design and sensor electrical design, refer to *Inductive Touch System Design Guide*.

8.2.1.3 Application Curves

图 8-16 shows a sequence of button presses of 150 grams force, two presses to Channel 0, then two presses to Channel 1. Each button press response is greater than the threshold.

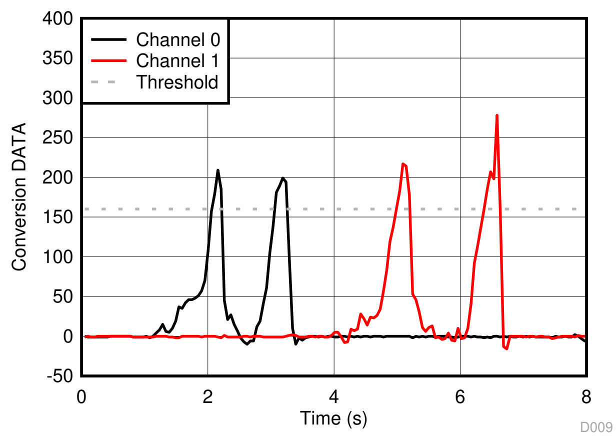


图 8-16. Conversion DATA vs Time for Channels 0 and 1

9 Power Supply Recommendations

The LDC3114-Q1 power supply should be bypassed with a 1-µF and a 0.1-µF pair of capacitors in parallel to ground. The capacitors should be placed as close to the LDC as possible. The smaller value 0.1-µF capacitor should be placed closer to the VDD pin than the 1-µF capacitor. The capacitors should be a low-ESL, low-ESR type.

Refer to *Recommended Operating Conditions* for more details.

10 Layout

10.1 Layout Guidelines

The COM pin must be bypassed to ground with an appropriate value capacitor. For details of how to choose the capacitor value, refer to *Setting COM Pin Capacitor*. C_{COM} should be placed as close as possible to the COM pin. The COM signal should be tied to a small copper fill placed underneath the IN*n* signals. The IN*n* signals should stay clear of other high frequency traces.

Each active channel needs to have an LC resonator connected to the corresponding IN*n* pins. The sensor capacitor should be placed within 10 mm of the corresponding IN*n* pin, and the inductor should be placed at the appropriate location next to (but not touching) the metal target. The IN*n* traces should be at least 6 mil (0.15 mm) wide to minimize parasitic inductances.

10.2 Layout Example

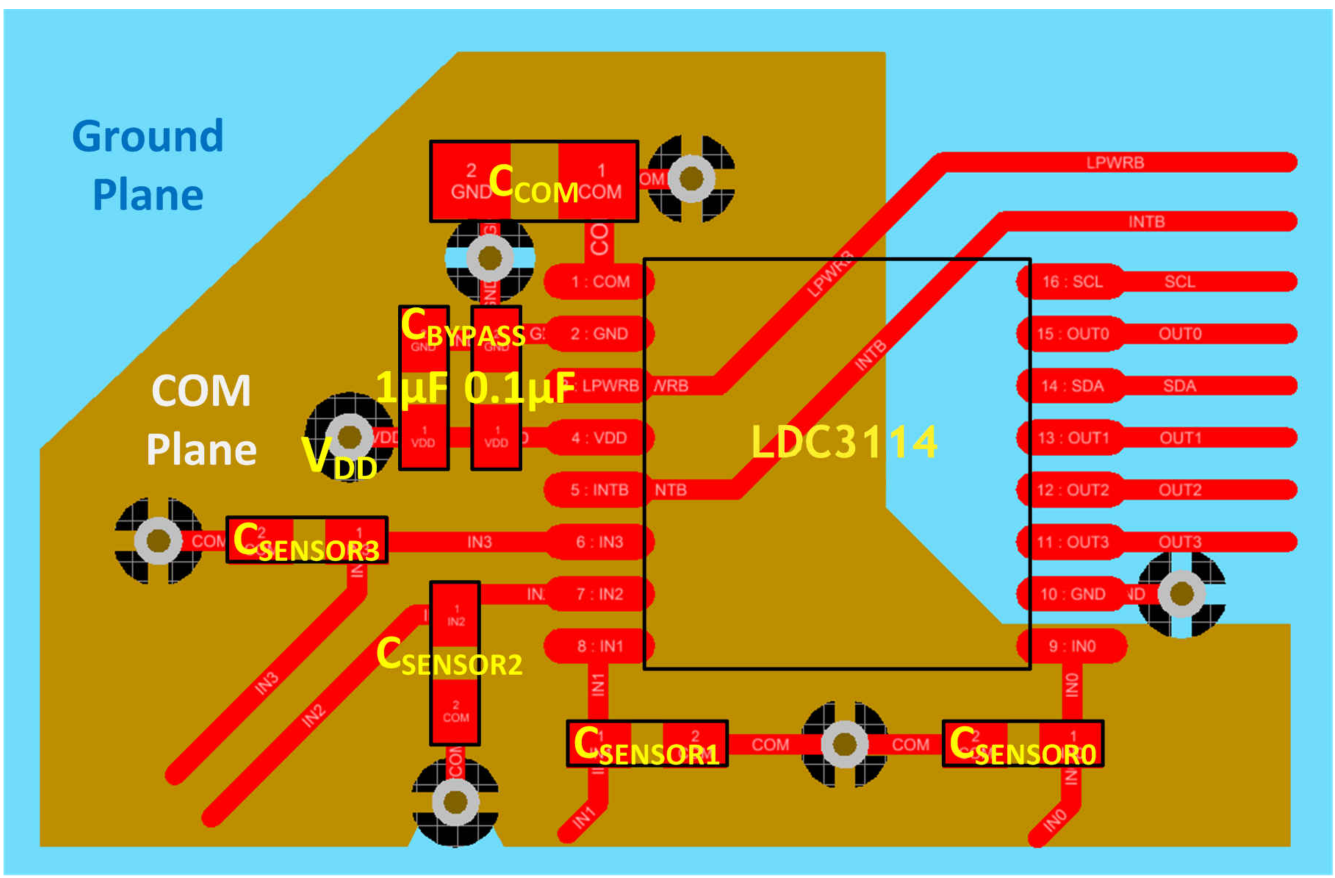


图 10-1. Layout of LDC3114-Q1 (TSSOP-16) With Decoupling Capacitors and Sensor Capacitors

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *LDC Calculations Tool*
- *Inductive Touch System Design Guide*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

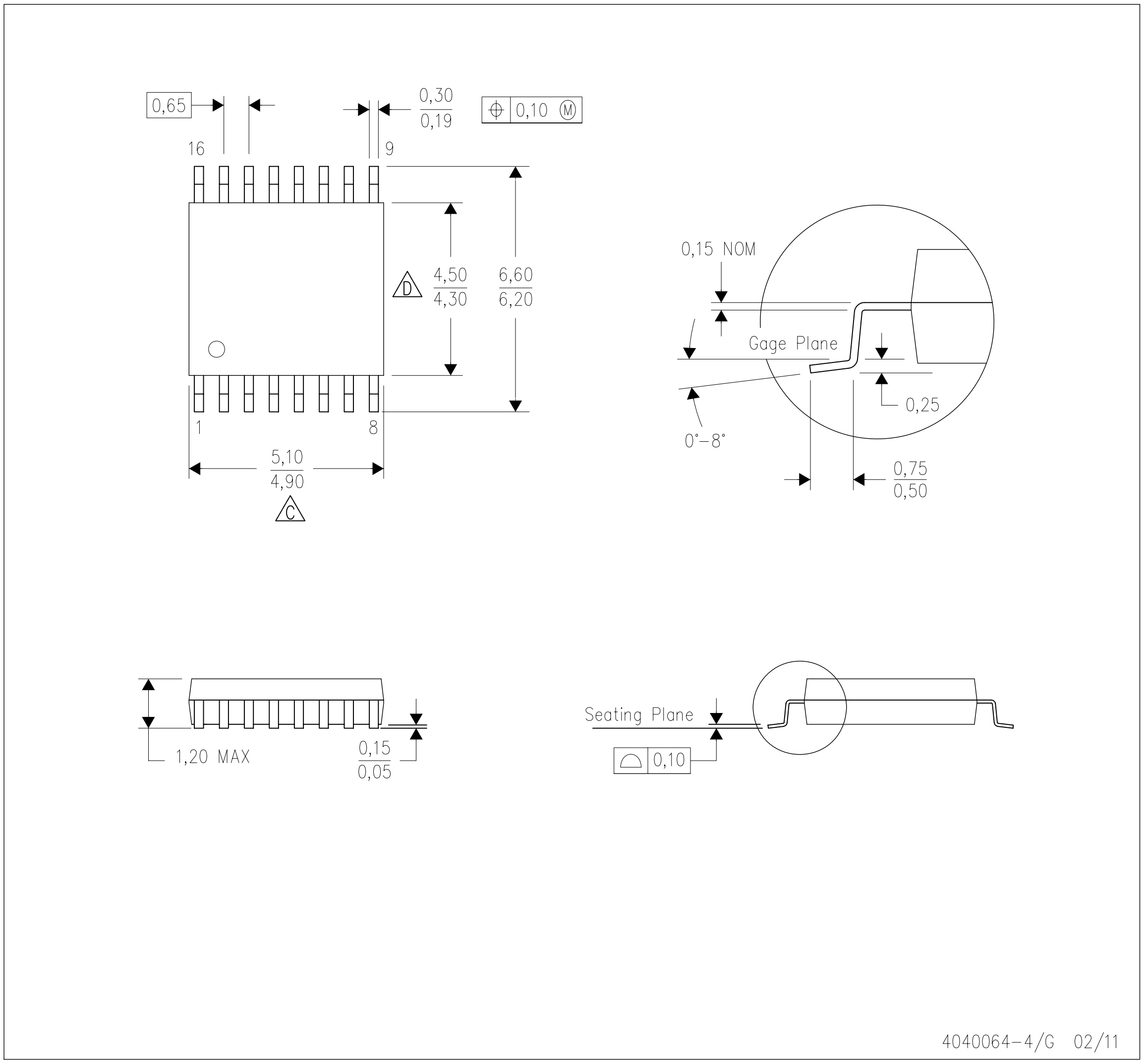
TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

MECHANICAL DATA

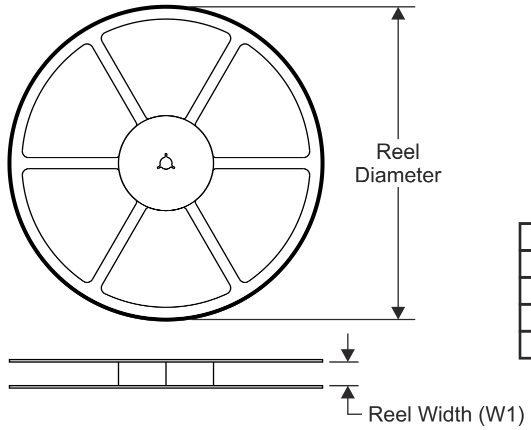
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



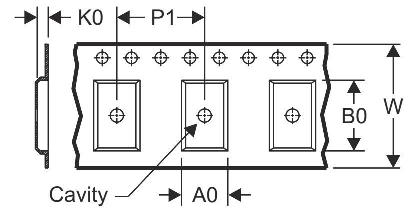
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

12.1 Tape and Reel Information

REEL DIMENSIONS

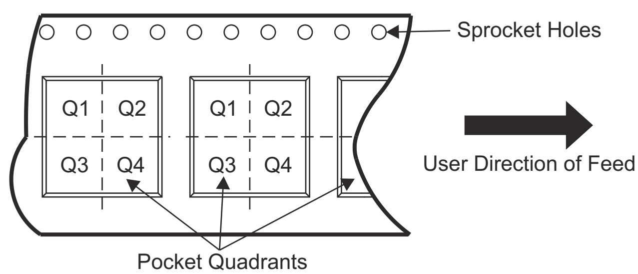


TAPE DIMENSIONS



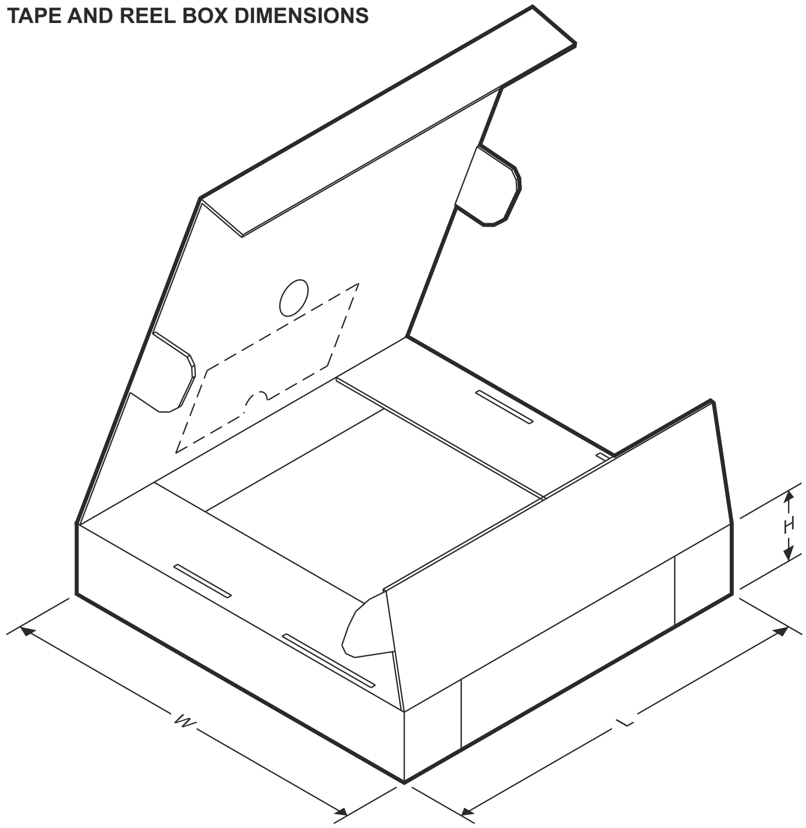
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC3114QPWRQ1	TSSOP	PW	16	2000	330	12.4	6.9	5.6	1.6	8	12	Q1
LDC3114QPWTQ1	TSSOP	PW	16	250	180	12.4	6.9	5.6	1.6	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC3114QPWRQ1	TSSOP	PW	16	2000	350 or 367	350 or 367	43 or 38
LDC3114QPWTQ1	TSSOP	PW	16	250	210	185	35

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LDC3114QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QDC3114	Samples
LDC3114QPWTQ1	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QDC3114	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

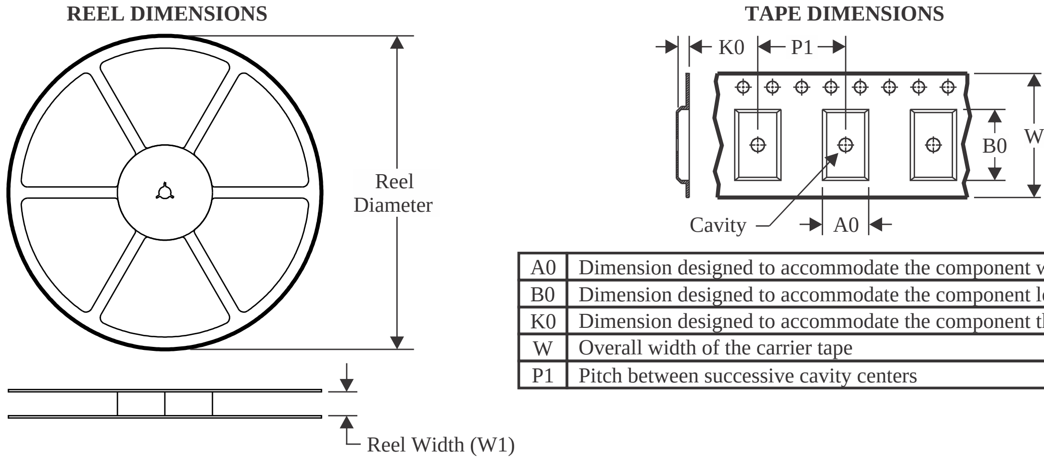
OTHER QUALIFIED VERSIONS OF LDC3114-Q1 :

- Catalog : LDC3114

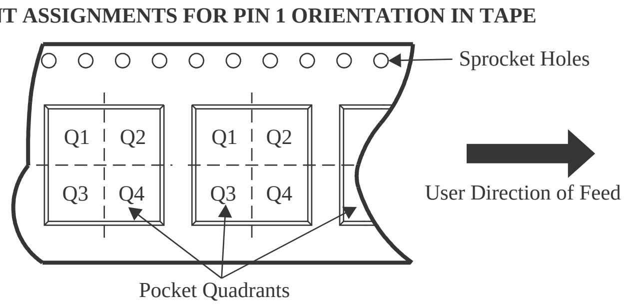
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



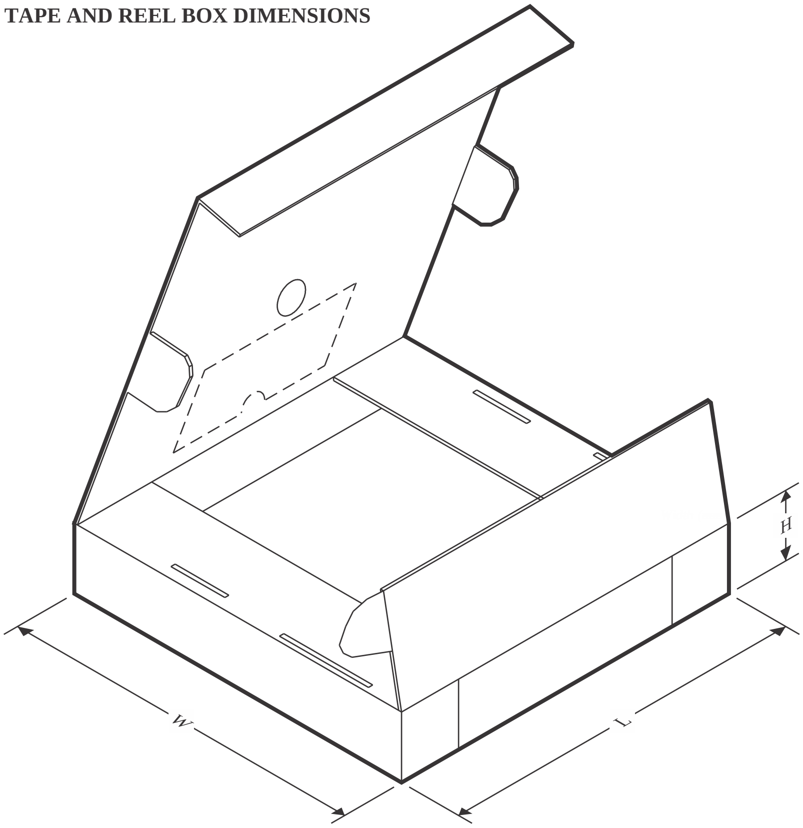
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

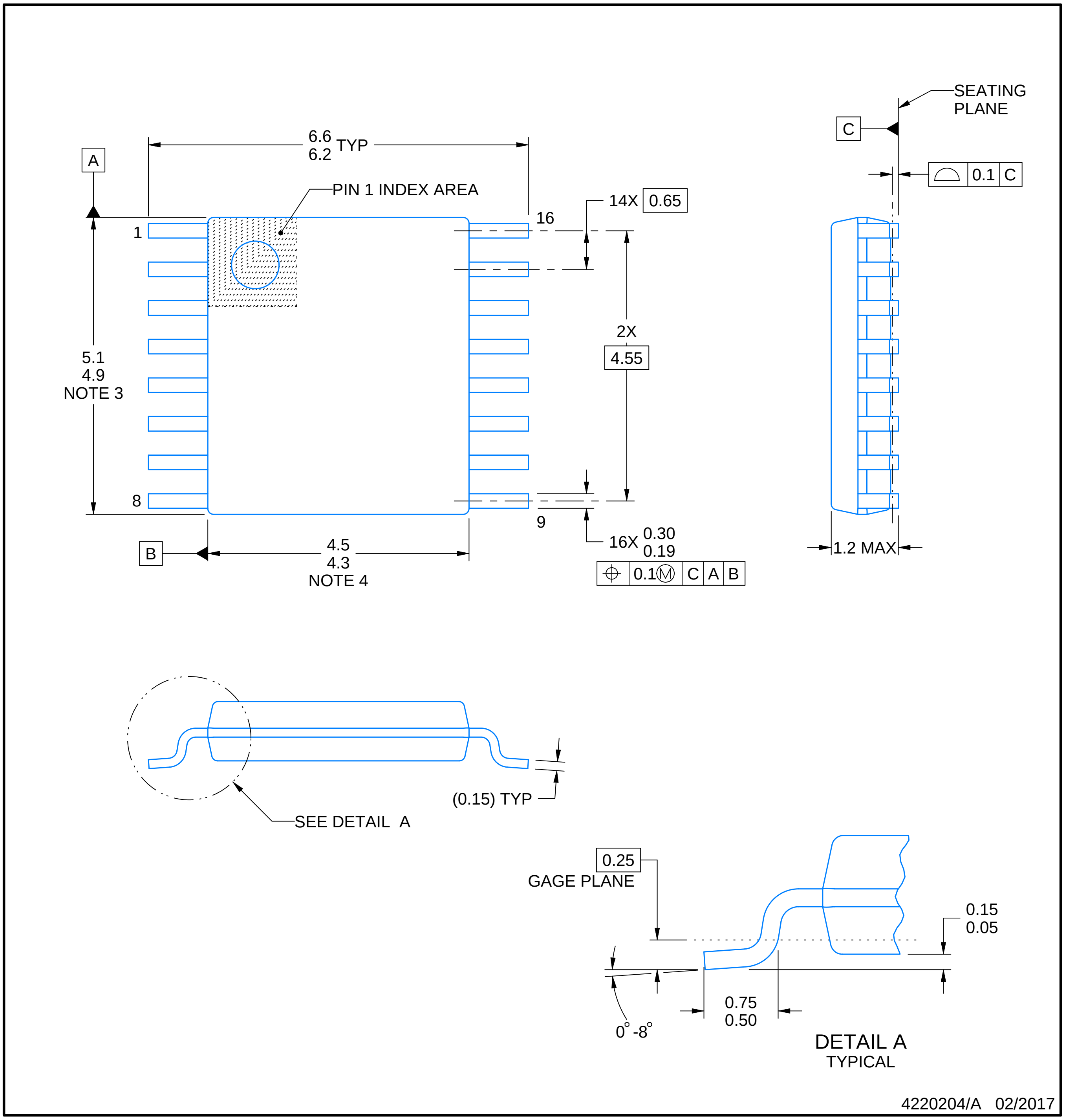
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC3114QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



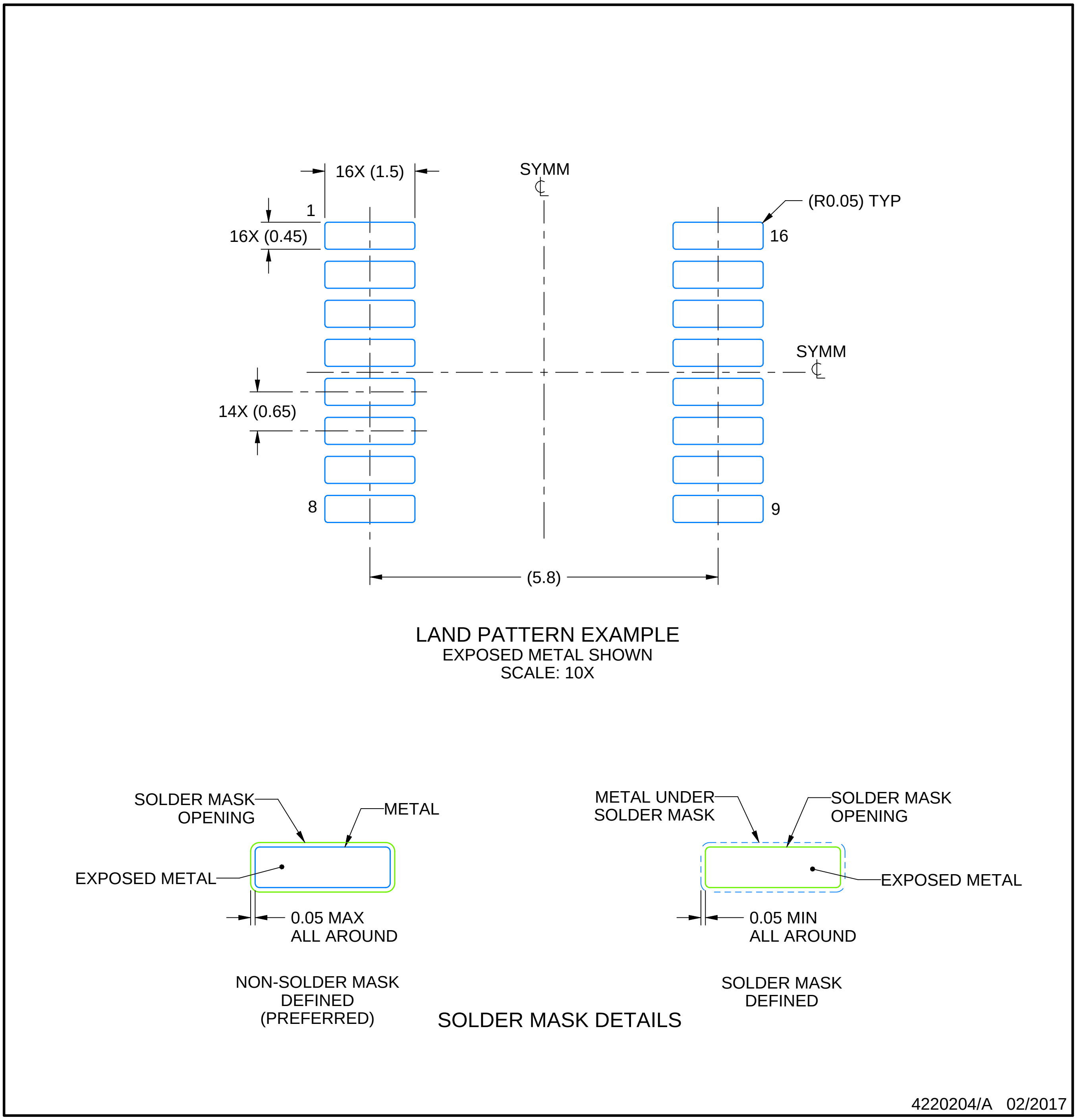
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC3114QPWRQ1	TSSOP	PW	16	2000	350.0	350.0	43.0



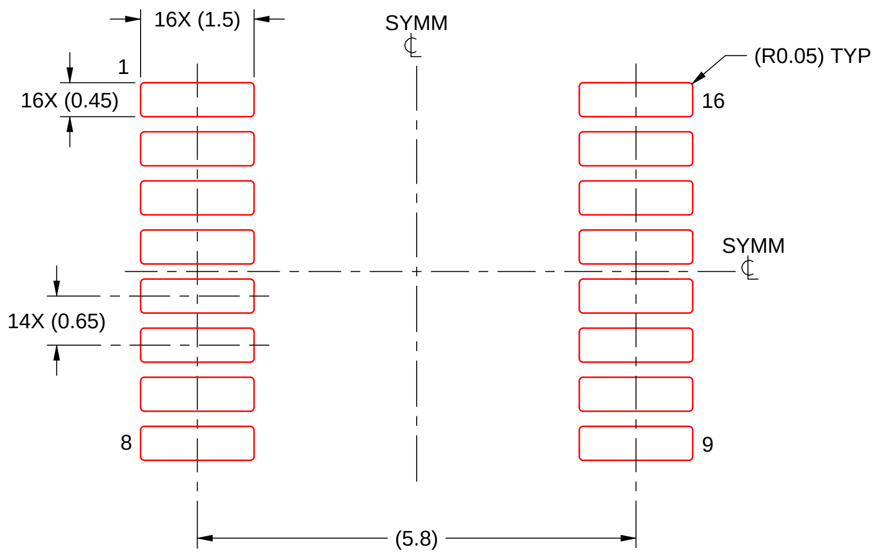
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明