

## 使用漏极开路输出的 SN74HC266 四路 2 输入 XNOR 门

### 1 特性

- 宽工作电压范围：2V 至 6V
- 输出可驱动多达 10 个低功耗肖特基晶体管逻辑电路 (LSTTL) 负载
- 低功耗， $I_{CC}$  最大值为 20 $\mu$ A
- 5V 时，典型  $t_{pd} = 8$ ns
- $\pm 4$  mA 输出驱动（在 5V 时）
- 低输入电流，1 $\mu$ A

### 2 应用

- 可选缓冲器/逆变器
- 时钟相位差检测器

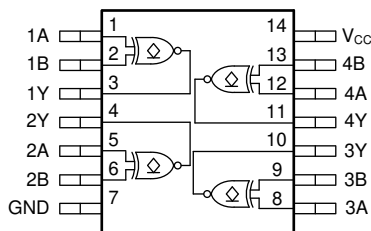
### 3 说明

该器件包含四个具有漏极开路输出的独立 2 输入异或非门。每个逻辑门以正逻辑执行布尔函数  $Y = A \oplus B$ 。

#### 器件信息(1)

| 器件型号        | 封装        | 封装尺寸 (标称值)       |
|-------------|-----------|------------------|
| SN74HC266N  | PDIP (14) | 19.30mm × 6.40mm |
| SN74HC266NS | SO (14)   | 10.20mm × 5.30mm |
| SN74HC266D  | SOIC (14) | 8.70mm × 3.90mm  |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



SN74HC266 的功能引脚排列

## Table of Contents

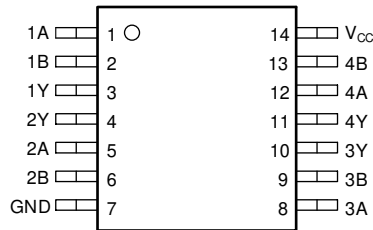
|  |   |  |    |
|--|---|--|----|
| <b>1 特性</b> .....                                | 1 | 8.3 Feature Description.....                                     | 8  |
| <b>2 应用</b> .....                                | 1 | 8.4 Device Functional Modes.....                                 | 9  |
| <b>3 说明</b> .....                                | 1 | <b>9 Application and Implementation</b> .....                    | 10 |
| <b>4 Revision History</b> .....                  | 2 | 9.1 Application Information.....                                 | 10 |
| <b>5 Pin Configuration and Functions</b> .....   | 3 | 9.2 Typical Application.....                                     | 10 |
| Pin Functions.....                               | 3 | <b>10 Power Supply Recommendations</b> .....                     | 12 |
| <b>6 Specifications</b> .....                    | 4 | <b>11 Layout</b> .....   | 12 |
| 6.1 Absolute Maximum Ratings.....                | 4 | 11.1 Layout Guidelines.....                                      | 12 |
| 6.2 Recommended Operating Conditions.....        | 4 | 11.2 Layout Example.....   | 12 |
| 6.3 Thermal Information.....                     | 4 | <b>12 Device and Documentation Support</b> .....                 | 13 |
| 6.4 Electrical Characteristics.....              | 5 | 12.1 Documentation Support.....                                  | 13 |
| 6.5 Switching Characteristics.....               | 5 | 12.2 Related Links.....  | 13 |
| 6.6 Operating Characteristics.....               | 5 | 12.3 支持资源.....   | 13 |
| 6.7 Typical Characteristics.....                 | 6 | 12.4 Trademarks.....   | 13 |
| <b>7 Parameter Measurement Information</b> ..... | 7 | 12.5 静电放电警告.....   | 13 |
| <b>8 Detailed Description</b> .....              | 8 | 12.6 术语表.....  | 13 |
| 8.1 Overview.....                                | 8 | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | 13 |
| 8.2 Functional Block Diagram.....                | 8 |  |    |

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| <b>Changes from Revision F (August 2003) to Revision G (April 2021)</b> | <b>Page</b> |
|---|-------------|
| • 更新了整个文档中的表格、图和交叉参考的编号格式.....  | 1           |
| • 更新为新的 TIS 格式.....   | 1           |

## 5 Pin Configuration and Functions



**图 5-1. D, N, or NS Package  
 14-Pin SOIC, PDIP, or SO  
 Top View**

## Pin Functions

| PIN             |     | I/O    | DESCRIPTION         |
|-----------------|-----|--------|---------------------|
| NAME            | NO. |        |                     |
| 1A              | 1   | Input  | Channel 1, Input A  |
| 1B              | 2   | Input  | Channel 1, Input B  |
| 1Y              | 3   | Output | Channel 1, Output Y |
| 2Y              | 4   | Output | Channel 2, Output Y |
| 2A              | 5   | Input  | Channel 2, Input A  |
| 2B              | 6   | Input  | Channel 2, Input B  |
| GND             | 7   | —      | Ground              |
| 3A              | 8   | Input  | Channel 3, Input A  |
| 3B              | 9   | Input  | Channel 3, Input B  |
| 3Y              | 10  | Output | Channel 3, Output Y |
| 4Y              | 11  | Output | Channel 4, Output Y |
| 4A              | 12  | Input  | Channel 4, Input A  |
| 4B              | 13  | Input  | Channel 4, Input B  |
| V <sub>CC</sub> | 14  | —      | Positive Supply     |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |   | MIN  | MAX | UNIT   |
|------------------|---|--|-----|--------|
| V <sub>CC</sub>  | Supply voltage                                    | - 0.5  | 7   | V      |
| I <sub>IK</sub>  | Input clamp current <sup>(2)</sup>                | V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> |     | ±20 mA |
| I <sub>OK</sub>  | Output clamp current <sup>(2)</sup>               | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> |     | ±20 mA |
| I <sub>O</sub>   | Continuous output current                         | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |     | ±25 mA |
|                  | Continuous current through V <sub>CC</sub> or GND |  |     | ±50 mA |
| T <sub>J</sub>   | Junction temperature <sup>(3)</sup>               |  |     | 150 °C |
| T <sub>stg</sub> | Storage temperature                               | - 65   | 150 | °C     |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

### 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |                                | MIN                     | NOM  | MAX             | UNIT |
|-----------------|--------------------------------|-------------------------|------|-----------------|------|
| V <sub>CC</sub> | Supply voltage                 | 2                       | 5    | 6               | V    |
| V <sub>IH</sub> | High-level input voltage       | V <sub>CC</sub> = 2 V   | 1.5  | V               | V    |
|                 |                                | V <sub>CC</sub> = 4.5 V | 3.15 |                 |      |
|                 |                                | V <sub>CC</sub> = 6 V   | 4.2  |                 |      |
| V <sub>IL</sub> | Low-level input voltage        | V <sub>CC</sub> = 2 V   | 0.5  | V               | V    |
|                 |                                | V <sub>CC</sub> = 4.5 V | 1.35 |                 |      |
|                 |                                | V <sub>CC</sub> = 6 V   | 1.8  |                 |      |
| V <sub>I</sub>  | Input voltage                  | 0                       |      | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                 | 0                       |      | V <sub>CC</sub> | V    |
| t <sub>t</sub>  | Input transition time          | V <sub>CC</sub> = 2 V   |      | 1000            | ns   |
|                 |                                | V <sub>CC</sub> = 4.5 V |      | 500             |      |
|                 |                                | V <sub>CC</sub> = 6 V   |      | 400             |      |
| T <sub>A</sub>  | Operating free-air temperature | - 40                    |      | 85              | °C   |

### 6.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | SN74HC266 |          |          | UNIT |
|-------------------------------|--|-----------|----------|----------|------|
|                               |  | N (PDIP)  | D (SOIC) | NS (SOP) |      |
|                               |  | 14 PINS   | 14 PINS  | 14 PINS  |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 62.5      | 133.6    | 122.6    | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 42.4      | 89.0     | 81.8     | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 50.2      | 89.5     | 83.8     | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 29.8      | 45.5     | 45.4     | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 42.0      | 89.1     | 83.4     | °C/W |

| THERMAL METRIC <sup>(1)</sup> |  | SN74HC266 |          |          | UNIT |
|-------------------------------|--|-----------|----------|----------|------|
|                               |  | N (PDIP)  | D (SOIC) | NS (SOP) |      |
|                               |  | 14 PINS   | 14 PINS  | 14 PINS  |      |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A       | N/A      | N/A      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.4 Electrical Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

| PARAMETER |                           | TEST CONDITIONS            |                           | $V_{CC}$   | Operating free-air temperature ( $T_A$ ) |           |     |               |            |               | UNIT |
|-----------|---------------------------|----------------------------|---------------------------|------------|--|-----------|-----|---------------|------------|---------------|------|
|           |                           |                            |                           |            | 25°C                                     |           |     | -40°C to 85°C |            |               |      |
|           |                           |                            |                           |            | MIN                                      | TYP       | MAX | MIN           | TYP        | MAX           |      |
| $I_{OH}$  | High-level output current | $V_I = V_{IH}$ or $V_{IL}$ | $V_O = V_{CC}$            | 6 V        | 0.01                                     | 0.5       |     |               | 5          | $\mu\text{A}$ |      |
| $V_{OL}$  | Low-level output voltage  | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL} = 20 \mu\text{A}$ | 2 V        | 0.002                                    | 0.1       |     |               | 0.1        | V             |      |
|           |                           |                            |                           | 4.5 V      | 0.001                                    | 0.1       |     |               | 0.1        |               |      |
|           |                           |                            | 6 V                       | 0.001      | 0.1                                      |           |     | 0.1           |            |               |      |
|           |                           |                            | $I_{OL} = 4 \text{ mA}$   | 4.5 V      | 0.17                                     | 0.26      |     |               | 0.33       |               |      |
|           |                           |                            | $I_{OL} = 5.2 \text{ mA}$ | 6 V        | 0.15                                     | 0.26      |     |               | 0.33       |               |      |
| $I_I$     | Input leakage current     | $V_I = V_{CC}$ or 0        |                           | 6 V        | $\pm 0.1$                                | $\pm 100$ |     |               | $\pm 1000$ | nA            |      |
| $I_{CC}$  | Supply current            | $V_I = V_{CC}$ or 0        | $V_I = V_{CC}$ or 0       | 6 V        |  |           | 2   |               | 20         | $\mu\text{A}$ |      |
| $C_i$     | Input capacitance         |                            |                           | 2 V to 6 V | 3  | 10        |     |               | 10         | pF            |      |

## 6.5 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER |                                 | FROM   | TO | $V_{CC}$ | Operating free-air temperature ( $T_A$ ) |     |     |               |     |     | UNIT |
|-----------|---------------------------------|--------|----|----------|--|-----|-----|---------------|-----|-----|------|
|           |                                 |        |    |          | 25°C                                     |     |     | -40°C to 85°C |     |     |      |
|           |                                 |        |    |          | MIN                                      | TYP | MAX | MIN           | TYP | MAX |      |
| $t_{PLH}$ | Propagation delay (Low to High) | A or B | Y  | 2 V      | 60                                       | 125 |     |               | 155 | ns  |      |
|           |                                 |        |    | 4.5 V    | 13                                       | 25  |     |               | 31  |     |      |
|           |                                 |        |    | 6 V      | 10                                       | 23  |     |               | 26  |     |      |
| $t_{PHL}$ | Propagation delay (High to Low) | A or B | Y  | 2 V      | 60                                       | 100 |     |               | 125 | ns  |      |
|           |                                 |        |    | 4.5 V    | 13                                       | 20  |     |               | 25  |     |      |
|           |                                 |        |    | 6 V      | 10                                       | 17  |     |               | 21  |     |      |
| $t_t$     | Transition-time                 |        | Y  | 2 V      | 28                                       | 75  |     |               | 95  | ns  |      |
|           |                                 |        |    | 4.5 V    | 8  | 15  |     |               | 19  |     |      |
|           |                                 |        |    | 6 V      | 6  | 13  |     |               | 16  |     |      |

## 6.6 Operating Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

| PARAMETER |  | TEST CONDITIONS | $V_{CC}$   | MIN | TYP | MAX | UNIT |
|-----------|--|-----------------|------------|-----|-----|-----|------|
| $C_{pd}$  | Power dissipation capacitance per gate | No load         | 2 V to 6 V |     | 35  |     | pF   |

### 6.7 Typical Characteristics

T<sub>A</sub> = 25°C

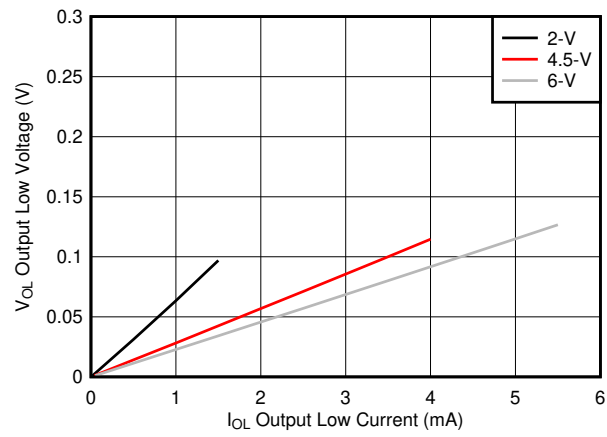
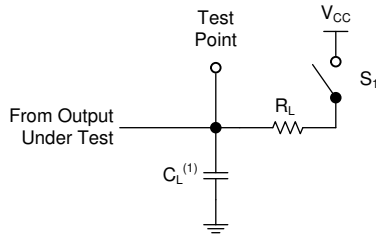


图 6-1. Typical output voltage in the low state (V<sub>OL</sub>)

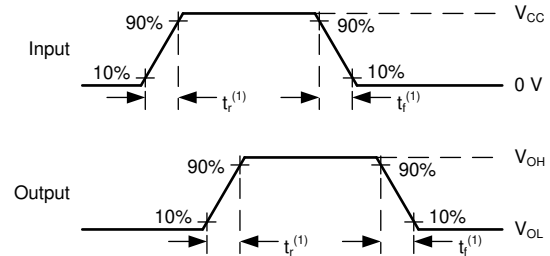
## 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .
- The outputs are measured one at a time, with one input transition per measurement.



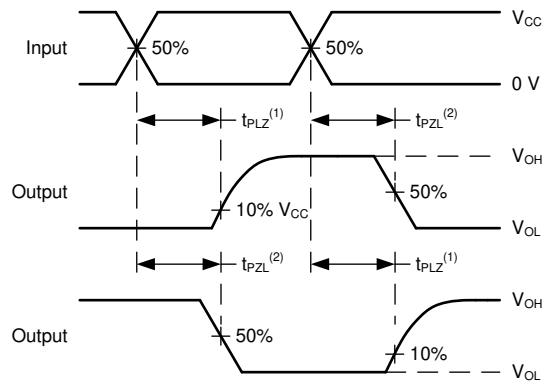
A.  $C_L = 50 \text{ pF}$  and includes probe and jig capacitance.

**图 7-1. Load Circuit**



A.  $t_t$  is the greater of  $t_r$  and  $t_f$ .

**图 7-2. Voltage Waveforms Transition Times**



A. The maximum between  $t_{pLH}$  and  $t_{pHL}$  is used for  $t_{pd}$ .

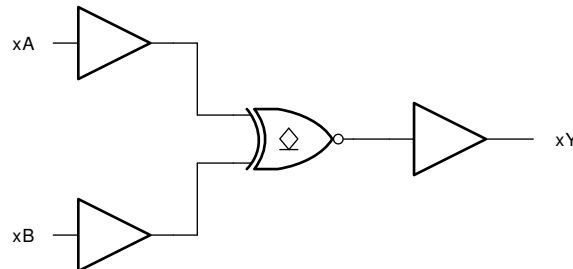
**图 7-3. Voltage Waveforms Propagation Delays**

## 8 Detailed Description

### 8.1 Overview

This device contains four independent 2-input XNOR gates with open-drain outputs. Each gate performs the Boolean function  $Y = \overline{A \oplus B}$  in positive logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 CMOS Open-Drain Outputs

The open-drain output allows the device to sink current to GND but not to source current from  $V_{CC}$ . When the output is not actively pulling the line low, it will go into a high impedance state. This allows the device to be used for a wide variety of applications, including up-translation and down-translation, as the output voltage can be determined by an external pull-up resistor.

The current drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

The SN74HC266 can drive a load with a total capacitance less than or equal to the maximum load listed in the [Switching Characteristics](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Absolute Maximum Ratings](#).

#### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.



### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 图 8-1.

**CAUTION**

Voltages beyond the values specified in the 表 6.1 table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

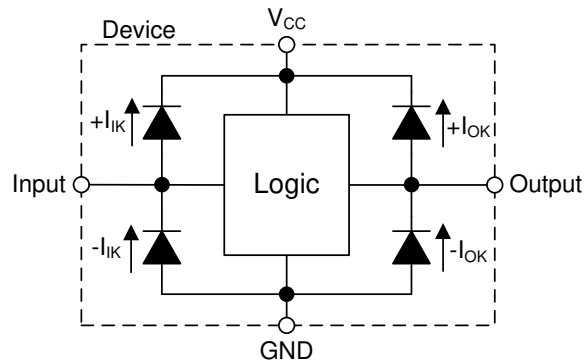


图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.4 Device Functional Modes

表 8-1. Function Table

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| L      | L | Z      |
| L      | H | L      |
| H      | L | L      |
| H      | H | Z      |

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

In this application, one 2-input open-drain XNOR gate is used to create a selectable buffer or inverter as shown in [图 9-1](#). This application allows for using a quad XNOR gate to produce any combination of one to four buffers and inverters. Commonly each channel is permanently connected as either an inverter or buffer, however some systems do require the ability to switch between the two. If some channels are unused, the inputs can be grounded and the outputs left open.

### 9.2 Typical Application

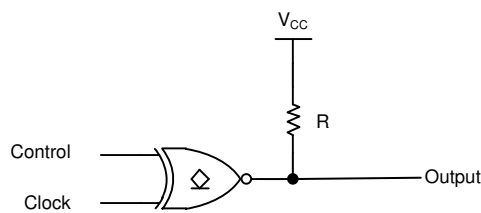


图 9-1. Typical application schematic

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HC266 plus the maximum supply current,  $I_{CC}$ , listed in [Electrical Characteristics](#). The logic device can only sink as much current as is provided by the external pull-up resistor or other supply source. Be sure not to exceed the maximum total current through GND listed in the [Absolute Maximum Ratings](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_J(\text{max})$  listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

##### 9.2.1.2 Input Considerations

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC266, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74HC266 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [Recommended Operating Conditions](#).

Refer to [§ 8.3](#) for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [Electrical Characteristics](#). The plot in the [Typical Characteristics](#) provides a typical relationship between output voltage and current for this device.

Open-drain outputs can be directly connected together to produce a wired-AND. This is possible because the outputs cannot source current, and thus can never be in bus-contention.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to [§ 8.3](#) for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in [§ 11](#).
2. Ensure the capacitive load at the output is  $\leq 70$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC266 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

### 9.2.3 Application Curves

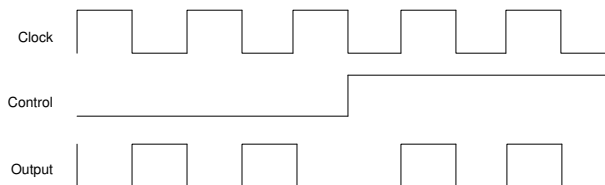


图 9-2. Typical application timing diagram

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [# 6.2](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [图 11-1](#).

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

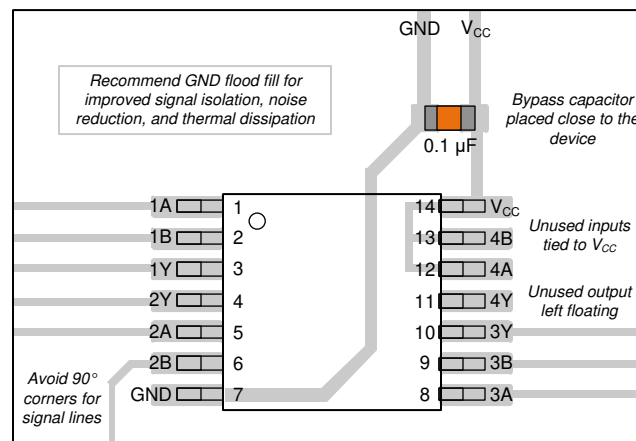


图 11-1. Example layout for the SN74HC266

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

### 12.3 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74HC266D       | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC266                   | <a href="#">Samples</a> |
| SN74HC266DR      | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | HC266                   | <a href="#">Samples</a> |
| SN74HC266DT      | ACTIVE        | SOIC         | D               | 14   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC266                   | <a href="#">Samples</a> |
| SN74HC266N       | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74HC266N              | <a href="#">Samples</a> |
| SN74HC266NSR     | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC266                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC266DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.6     | 9.3     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC266DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC266DT  | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC266NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.45    | 10.55   | 2.5     | 12.0    | 16.2   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC266DR  | SOIC         | D               | 14   | 2500 | 366.0       | 364.0      | 50.0        |
| SN74HC266DR  | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74HC266DT  | SOIC         | D               | 14   | 250  | 210.0       | 185.0      | 35.0        |
| SN74HC266NSR | SO           | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

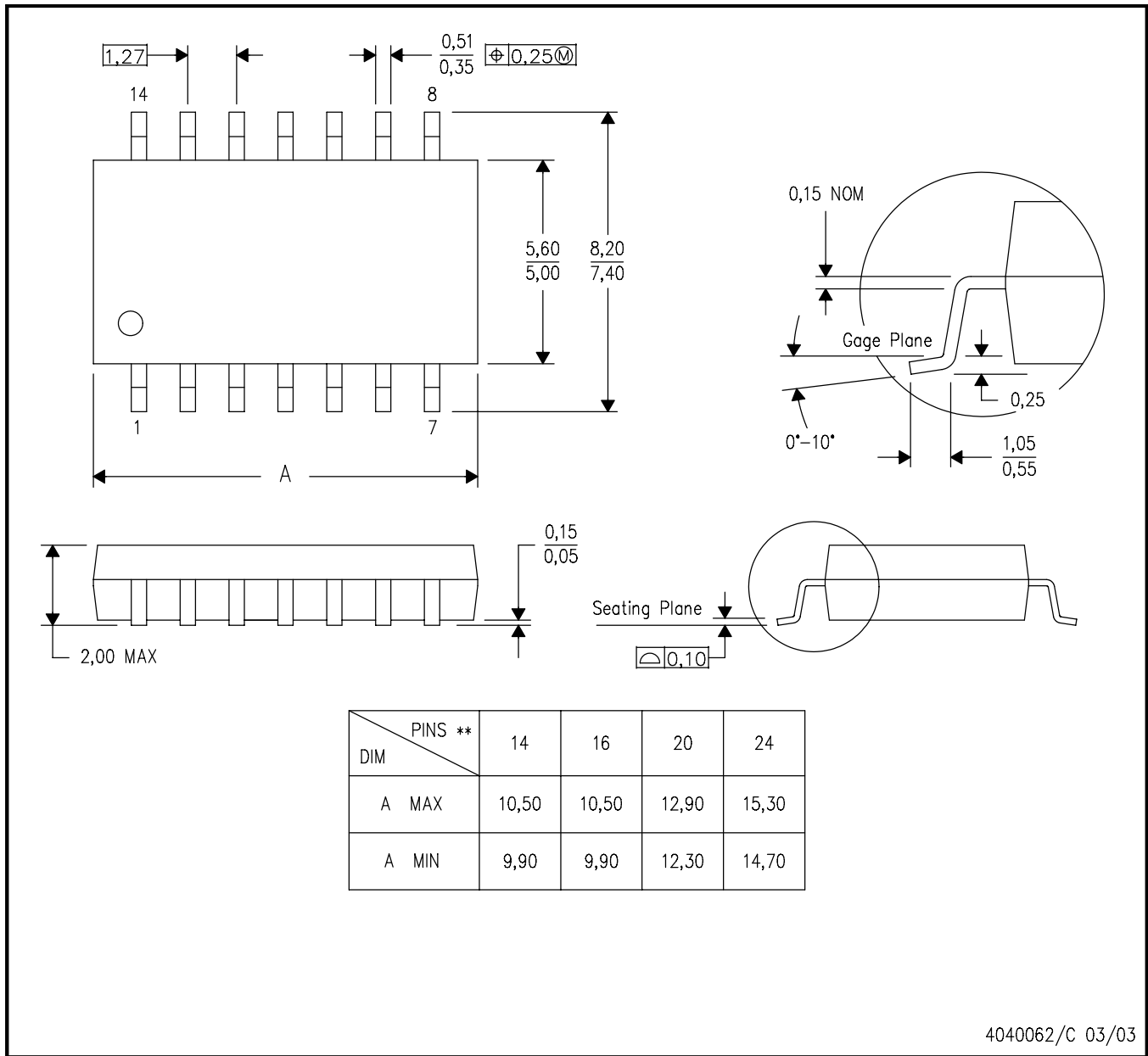
| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74HC266D | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74HC266N | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC266N | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司