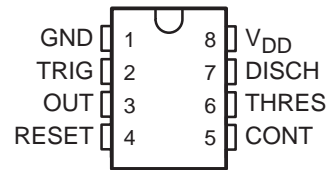
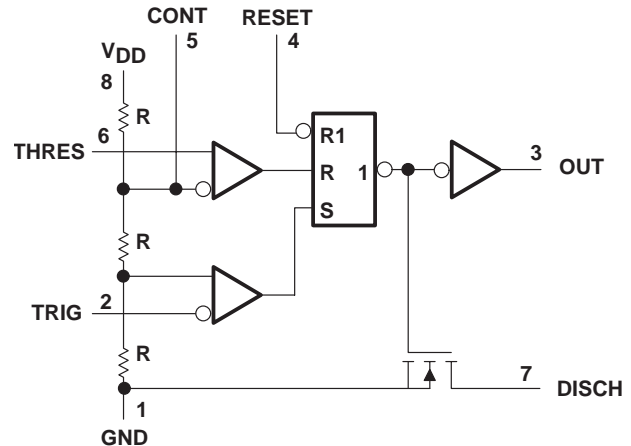


- **Very Low Power Consumption**
1 mW Typ at $V_{DD} = 5\text{ V}$
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
Sink 100 mA Typ
Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **Single-Supply Operation From 1 V to 15 V**
- **Functionally Interchangeable With the NE555; Has Same Pinout**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015.2**

D, DB, P, OR PW PACKAGE
(TOP VIEW)



functional block diagram



RESET can override TRIG, which can override THRES.

description

The TLC551 is a monolithic timing circuit fabricated using the TI LinCMOS™ process. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Compared to the NE555 timer, this device uses smaller timing capacitors because of its high input impedance. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC551 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal (CONT). When the trigger input (TRIG) falls below the trigger level, the flip-flop is set and the output goes high. If TRIG is above the trigger level and the threshold input (THRES) is above the threshold level, the flip-flop is reset and the output is low. The reset input (RESET) can override all other inputs and can be used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between DISCH and GND. All unused inputs should be tied to an appropriate logic level to prevent false triggering.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC551 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

The TLC551C is characterized for operation from 0°C to 70°C.



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either supply voltage or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

TLC551, TLC551Y LinCMOS™ TIMERS

SLFS044A – FEBRUARY 1984 – REVISED MAY 1997

AVAILABLE OPTIONS

PACKAGED DEVICES						CHIP FORM (Y)
T _A	V _{DD} RANGE	SMALL OUTLINE (D)	SSOP (DB)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	1 V to 16 V	TLC551CD	TLC551CDBLE	TLC551CP	TLC551CPWLE	TLC551Y

The D package is available taped and reeled. Add the suffix R (e.g., TLC551CDR). The DB and PW packages are only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TLC551CDBLE). Chips are tested at 25°C.

FUNCTION TABLE

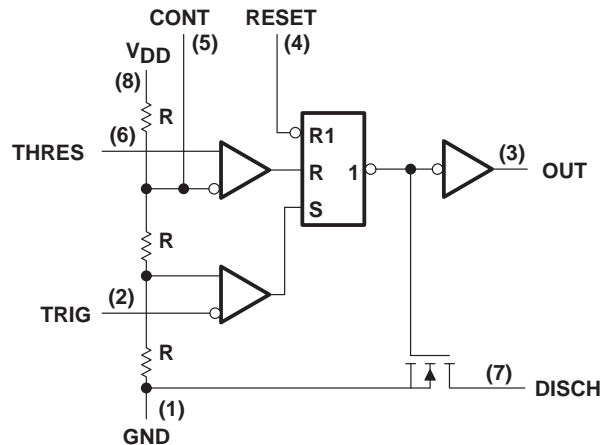
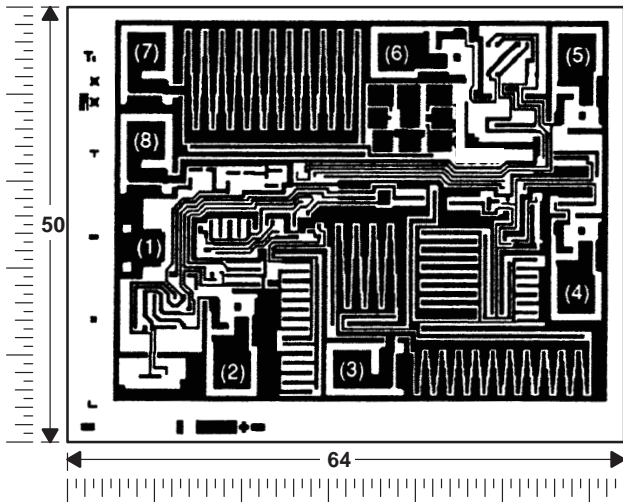
RESET VOLTAGE †	TRIGGER VOLTAGE †	THRESHOLD VOLTAGE †	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

TLC551Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC551. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



RESET can override TRIG, which can override THRES.

CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{Jmax} = 150°C

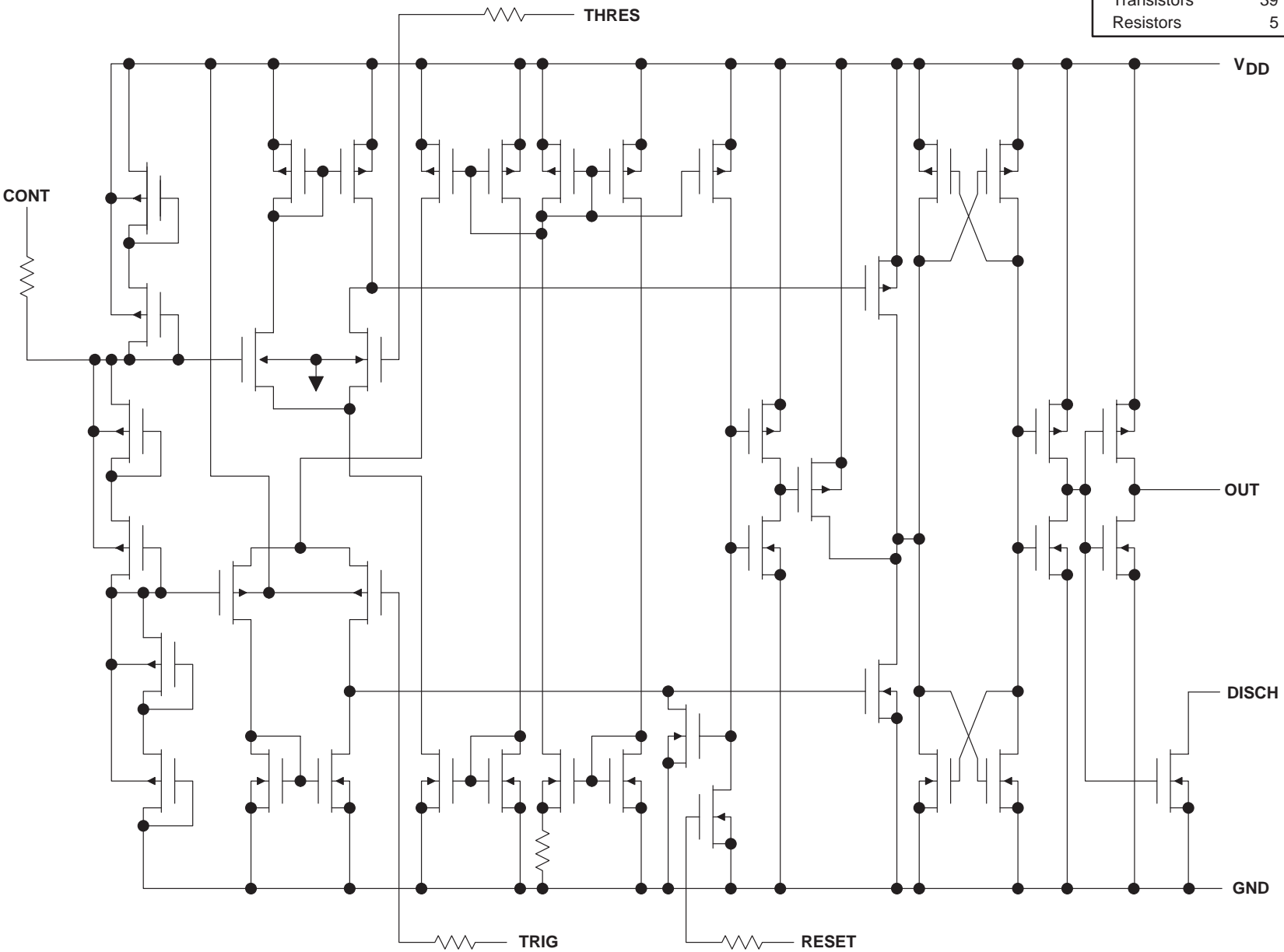
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (1) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

COMPONENT COUNT	
Transistors	39
Resistors	5

equivalent schematic



TLC551, TLC551Y LinCMOS™ TIMERS

SLFS044B – FEBRUARY 1984 – REVISED SEPTEMBER 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Input voltage range, V_I (any input)	-0.3 to V_{DD}
Sink current, discharge or output	150 mA
Source current, output, I_O	15 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
DB	525 mW	4.2 mW/°C	336 mW
P	1000 mW	8.0 mW/°C	640 mW
PW	525 mW	4.2 mW/°C	336 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	15	V
Operating free-air temperature range, T_A	0	70	°C



electrical characteristics at specified free-air temperature, $V_{DD} = 1\text{ V}$

PARAMETER		TEST CONDITIONS	T_A^\dagger	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	0.475	0.67	0.85	V
			Full range	0.45		0.875	
I_{IT}	Threshold current		25°C	10			pA
			70°C	75			
$V_{I(TRIG)}$	Trigger voltage		25°C	0.15	0.33	0.425	V
			Full range	0.1		0.45	
$I_{I(TRIG)}$	Trigger current		25°C	10			pA
			70°C	75			
$V_{I(RESET)}$	Reset voltage		25°C	0.4	0.7	1	V
			Full range	0.3		1	
$I_{I(RESET)}$	Reset current		25°C	10			pA
			70°C	75			
	Control voltage (open circuit) as a percentage of supply voltage		70°C	66.7%			
	Discharge switch on-stage voltage	$I_{OL} = 100\ \mu\text{A}$	25°C	0.02	0.15		V
			Full range		0.2		
	Discharge switch off-stage voltage		25°C	0.1			nA
			70°C	0.5			
V_{OH}	High-level output voltage	$I_{OH} = -10\ \mu\text{A}$	25°C	0.6	0.98		V
			Full range	0.6			
V_{OL}	Low-level output voltage	$I_{OL} = 100\ \mu\text{A}$	25°C	0.03	0.2		V
			Full range		0.25		
I_{DD}	Supply current	See Note 2	25°C	15	100		μA
			Full range		150		

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

TLC551, TLC551Y LinCMOS™ TIMERS

SLFS044B – FEBRUARY 1984 – REVISED SEPTEMBER 1997

electrical characteristics at specified free-air temperature, $V_{DD} = 2\text{ V}$

PARAMETER		TEST CONDITIONS	T_A^\dagger	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	0.95	1.33	1.65	V
			Full range	0.85		1.75	
I_{IT}	Threshold current		25°C	10			pA
			70°C	75			
$V_{I(TRIG)}$	Trigger voltage		25°C	0.4	0.67	0.95	V
			Full range	0.3		1.05	
$I_{I(TRIG)}$	Trigger current		25°C	10			pA
			70°C	75			
$V_{I(RESET)}$	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
$I_{I(RESET)}$	Reset current		25°C	10			pA
			70°C	75			
	Control voltage (open circuit) as a percentage of supply voltage		70°C	66.7%			
	Discharge switch on-stage voltage	$I_{OL} = 1\text{ mA}$	25°C	0.03	0.2		V
			Full range		0.25		
	Discharge switch off-stage voltage		25°C	0.1		nA	
			70°C	0.5			
V_{OH}	High-level output voltage	$I_{OH} = -300\ \mu\text{A}$	25°C	1.5	1.9		V
			Full range	1.5			
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{ mA}$	25°C	0.07	0.3		V
			Full range		0.35		
I_{DD}	Supply current	See Note 2	25°C	65	250		μA
			Full range		400		

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS	T_A^\dagger	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	2.8	3.3	3.8	V
			Full range	2.7		3.9	
I_{IT}	Threshold current		25°C	10			pA
			70°C	75			
$V_{I(TRIG)}$	Trigger voltage		25°C	1.36	1.66	1.96	V
			Full range	1.26		2.06	
$I_{I(TRIG)}$	Trigger current		25°C	10			pA
			70°C	75			
$V_{I(RESET)}$	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
$I_{I(RESET)}$	Reset current		25°C	10			pA
			70°C	75			
	Control voltage (open circuit) as a percentage of supply voltage		70°C	66.7%			
	Discharge switch on-stage voltage	$I_{OL} = 10\text{ mA}$	25°C	0.14	0.5		V
			Full range			0.6	
	Discharge switch off-stage voltage		25°C	0.1			nA
			70°C	0.5			
V_{OH}	High-level output voltage	$I_{OH} = -1\text{ mA}$	25°C	4.1	4.8		V
			Full range	4.1			
V_{OL}	Low-level output voltage	$I_{OL} = 8\text{ mA}$	25°C	0.21	0.4		V
			Full range			0.5	
		$I_{OL} = 5\text{ mA}$	25°C	0.13	0.3		
			Full range			0.4	
		$I_{OL} = 3.2\text{ mA}$	25°C	0.08	0.3		
			Full range			0.35	
I_{DD}	Supply current	See Note 2	25°C	170	350		μA
			Full range			500	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

TLC551, TLC551Y LinCMOS™ TIMERS

SLFS044B – FEBRUARY 1984 – REVISED SEPTEMBER 1997

electrical characteristics at specified free-air temperature, $V_{DD} = 15\text{ V}$

PARAMETER		TEST CONDITIONS	T_A †	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	9.45		10.55	V
			Full range	9.35		10.65	
I_{IT}	Threshold current		25°C		10		pA
			70°C		75		
$V_{I(TRIG)}$	Trigger voltage		25°C	4.65	5	5.35	V
			Full range	4.55		5.45	
$I_{I(TRIG)}$	Trigger current		25°C		10		pA
			70°C		75		
$V_{I(RESET)}$	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
$I_{I(RESET)}$	Reset current		25°C		10		pA
			70°C		75		
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%		
	Discharge switch on-stage voltage	$I_{OL} = 100\text{ mA}$	25°C		0.77	1.7	V
			Full range			1.8	
	Discharge switch off-stage voltage		25°C		0.1		nA
			70°C		0.5		
V_{OH}	High-level output voltage	$I_{OH} = -10\text{ mA}$	25°C	12.5	14.2		V
			Full range	12.5			
		$I_{OH} = -5\text{ mA}$	25°C	13.5	14.6		
			Full range	13.5			
		$I_{OH} = -1\text{ mA}$	25°C	14.2	14.9		
			Full range	14.2			
V_{OL}	Low-level output voltage	$I_{OL} = 100\text{ mA}$	25°C		1.28	3.2	V
			Full range			3.6	
		$I_{OL} = 50\text{ mA}$	25°C		0.63	1	
			Full range			1.3	
		$I_{OL} = 10\text{ mA}$	25°C		0.12	0.3	
			Full range			0.4	
I_{DD}	Supply current	See Note 2	25°C		360	600	μA
			Full range			800	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

operating characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Initial error of timing interval‡	$V_{DD} = 5\text{ V to }15\text{ V}$, $C_T = 0.1\text{ }\mu\text{F}$,	$R_A = R_B = 1\text{ k}\Omega\text{ to }100\text{ k}\Omega$, See Note 3		1%	3%	
Supply voltage sensitivity of timing interval				0.1	0.5	%/V
t_r Rise time, output pulse	$R_L = 10\text{ M}\Omega$,	$C_L = 10\text{ pF}$		20	75	ns
t_f Fall time, output pulse				15	60	
f_{max} Maximum frequency in astable mode	$R_A = 470\text{ }\Omega$, $C_T = 200\text{ pF}$	$R_B = 200\text{ }\Omega$, See Note 3	1.2	1.8		MHz

‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A , R_B , and C_T are as defined in Figure 3.



electrical characteristics at $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		2.8	3.3	3.8	V
I_{IT}	Threshold current			10		pA
$V_{I(TRIG)}$	Trigger voltage		1.36	1.66	1.96	V
$I_{I(TRIG)}$	Trigger current			10		pA
$V_{I(RESET)}$	Reset voltage		0.4	1.1	1.5	V
$I_{I(RESET)}$	Reset current			10		pA
	Control voltage (open circuit) as a percentage of supply voltage			66.7%		
	Discharge switch on-state voltage	$I_{OL} = 10\text{ mA}$		0.14	0.5	V
	Discharge switch off-state current			0.1		nA
V_{OH}	High-level output voltage	$I_{OH} = -1\text{ mA}$	4.1	4.8		V
V_{OL}	Low-level output voltage	$I_{OL} = 8\text{ mA}$		0.21	0.4	V
		$I_{OL} = 5\text{ mA}$		0.13	0.3	
		$I_{OL} = 3.2\text{ mA}$		0.08	0.3	
I_{DD}	Supply current	See Note 2		170	350	μA

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

TYPICAL CHARACTERISTICS

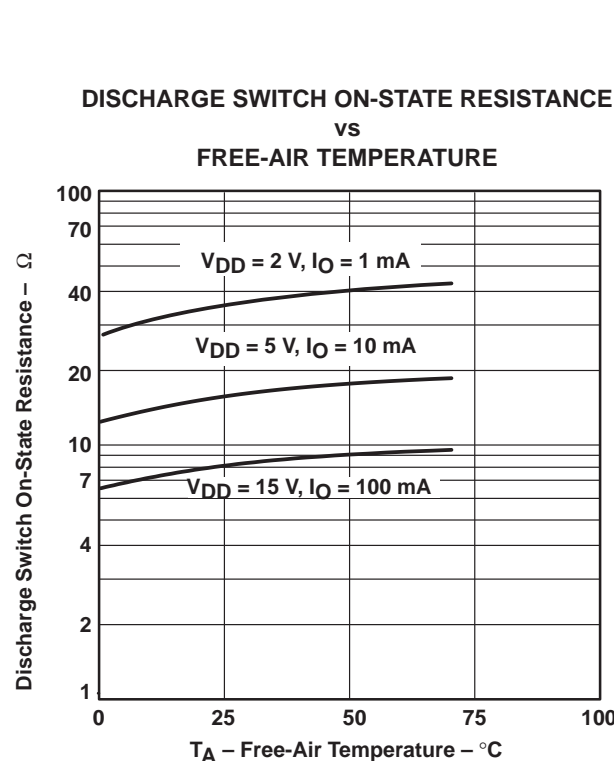
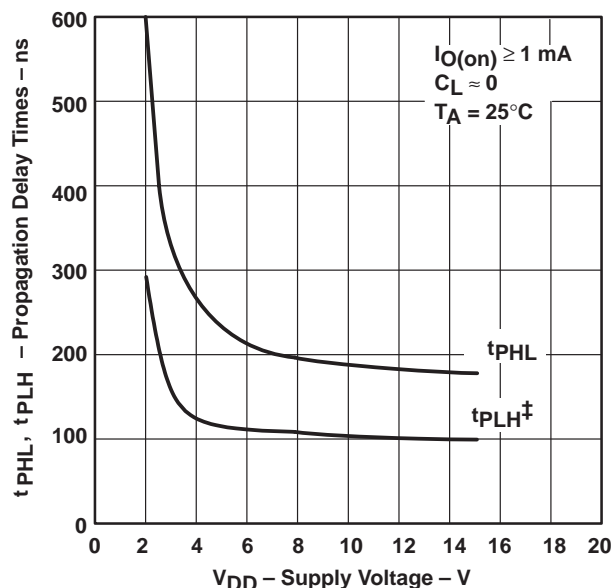


Figure 1

**PROPAGATION DELAY TIMES (TO DISCHARGE
OUTPUT FROM TRIGGER AND THRESHOLD
SHORTED TOGETHER)
vs
SUPPLY VOLTAGE**



† The effects of the load resistance on these values must be taken into account separately.

Figure 2

APPLICATION INFORMATION

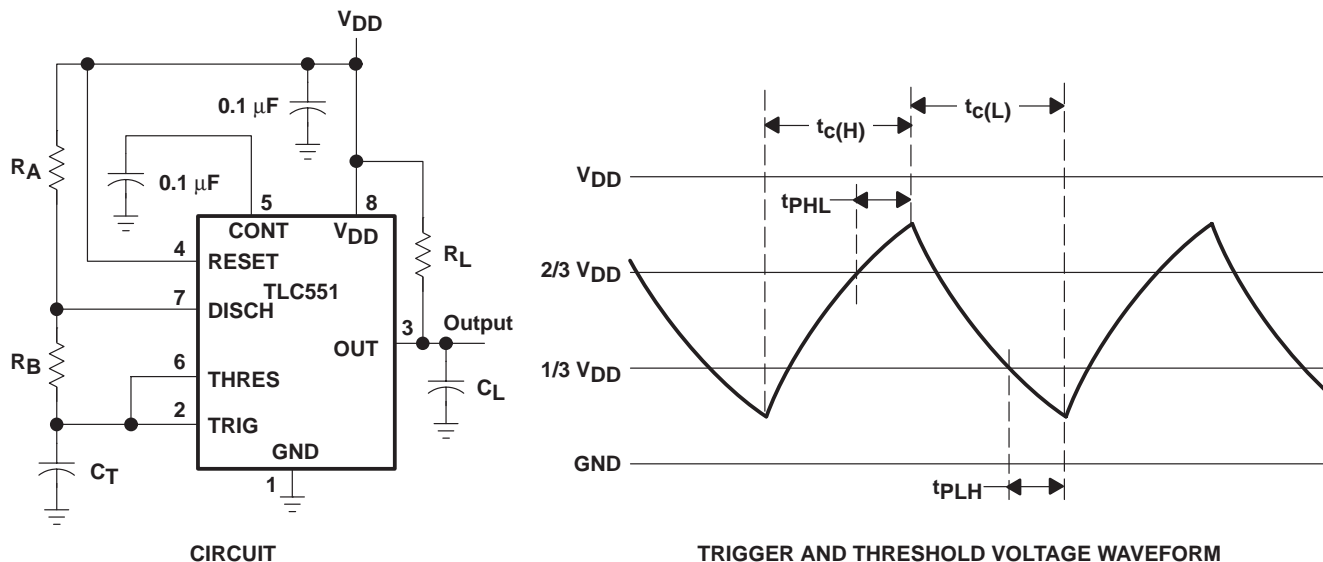


Figure 3. Astable Operation

Connecting TRIG to THRES, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the threshold voltage level (approximately $0.67 V_{DD}$) and then discharges through R_B only to the value of the trigger voltage level (approximately $0.33 V_{DD}$). The output is high during the charging cycle ($t_{c(H)}$) and low during the discharge cycle ($t_{c(L)}$). The duty cycle is controlled by the values of R_A , and R_B , and C_T , as shown in the equations below.

$$t_{c(H)} \approx C_T (R_A + R_B) \ln 2 \quad (\ln 2 = 0.693)$$

$$t_{c(L)} \approx C_T R_B \ln 2$$

$$\text{Period} = t_{c(H)} + t_{c(L)} \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_{c(L)}}{t_{c(H)} + t_{c(L)}} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_{c(H)}}{t_{c(H)} + t_{c(L)}} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1-μF capacitor at CONT in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay times from TRIG and THRES to DISCH. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance r_{on} during discharge adds to R_B to provide another source of timing error in the calculation when R_B is very low or r_{on} is very high.

APPLICATION INFORMATION

The equations below provide better agreement with measured values.

$$t_{c(H)} = C_T (R_A + R_B) \ln \left[3 - \exp \left(\frac{-t_{PLH}}{C_T (R_B + r_{on})} \right) \right] + t_{PLH}$$

$$t_{c(L)} = C_T (R_B + r_{on}) \ln \left[3 - \exp \left(\frac{-t_{PHL}}{C_T (R_A + R_B)} \right) \right] + t_{PHL}$$

These equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between $\ln 2$ at low frequencies and $\ln 3$ at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\frac{t_{c(H)}}{t_{c(H)} + t_{c(L)}}$ require that $\frac{t_{c(H)}}{t_{c(L)}} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

In monostable applications, the trip point of the trigger input can be set by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500- μ A bias provides good results.

TLC551, TLC551Y LinCMOS™ TIMERS

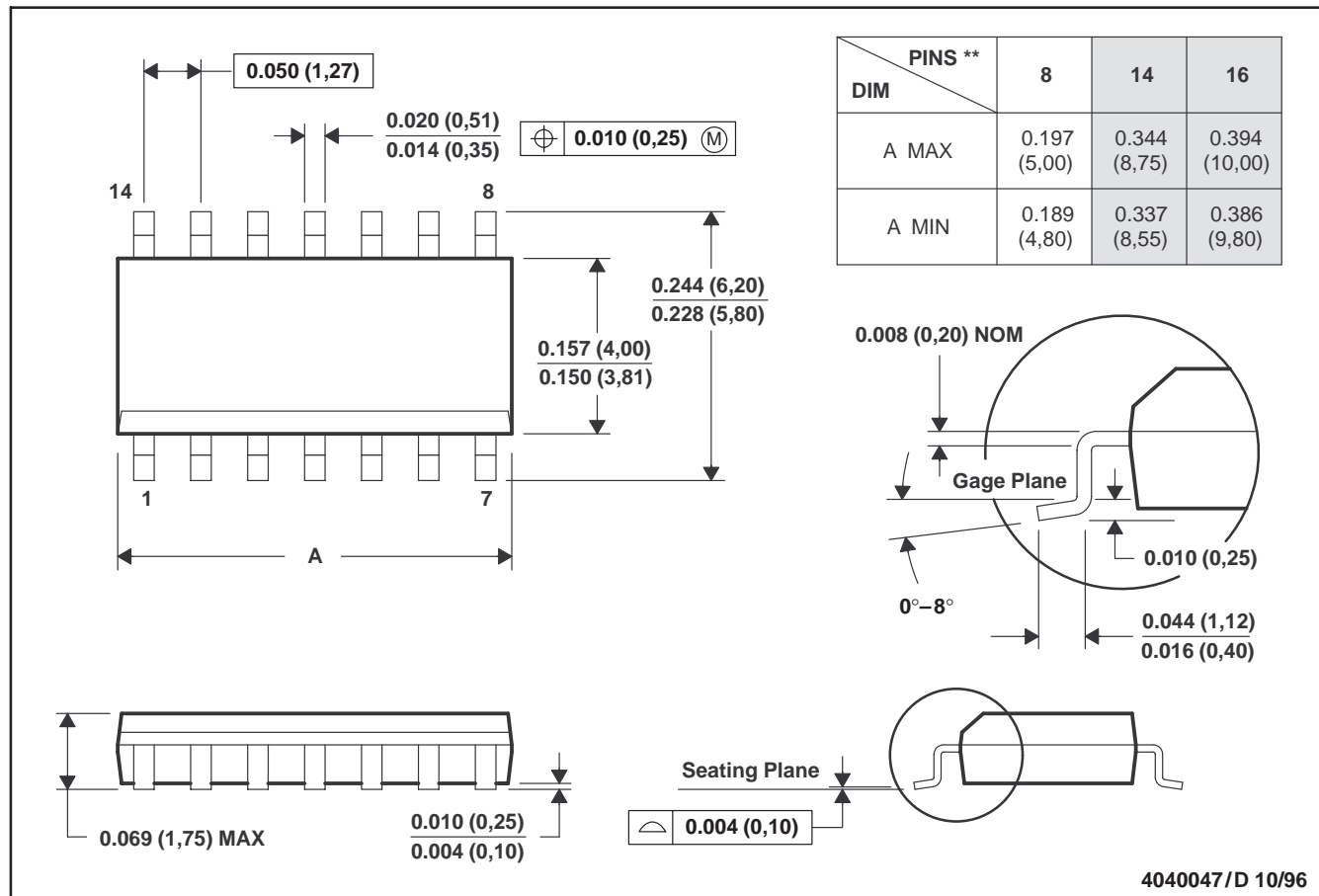
SLFS044B – FEBRUARY 1984 – REVISED SEPTEMBER 1997

MECHANICAL INFORMATION

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



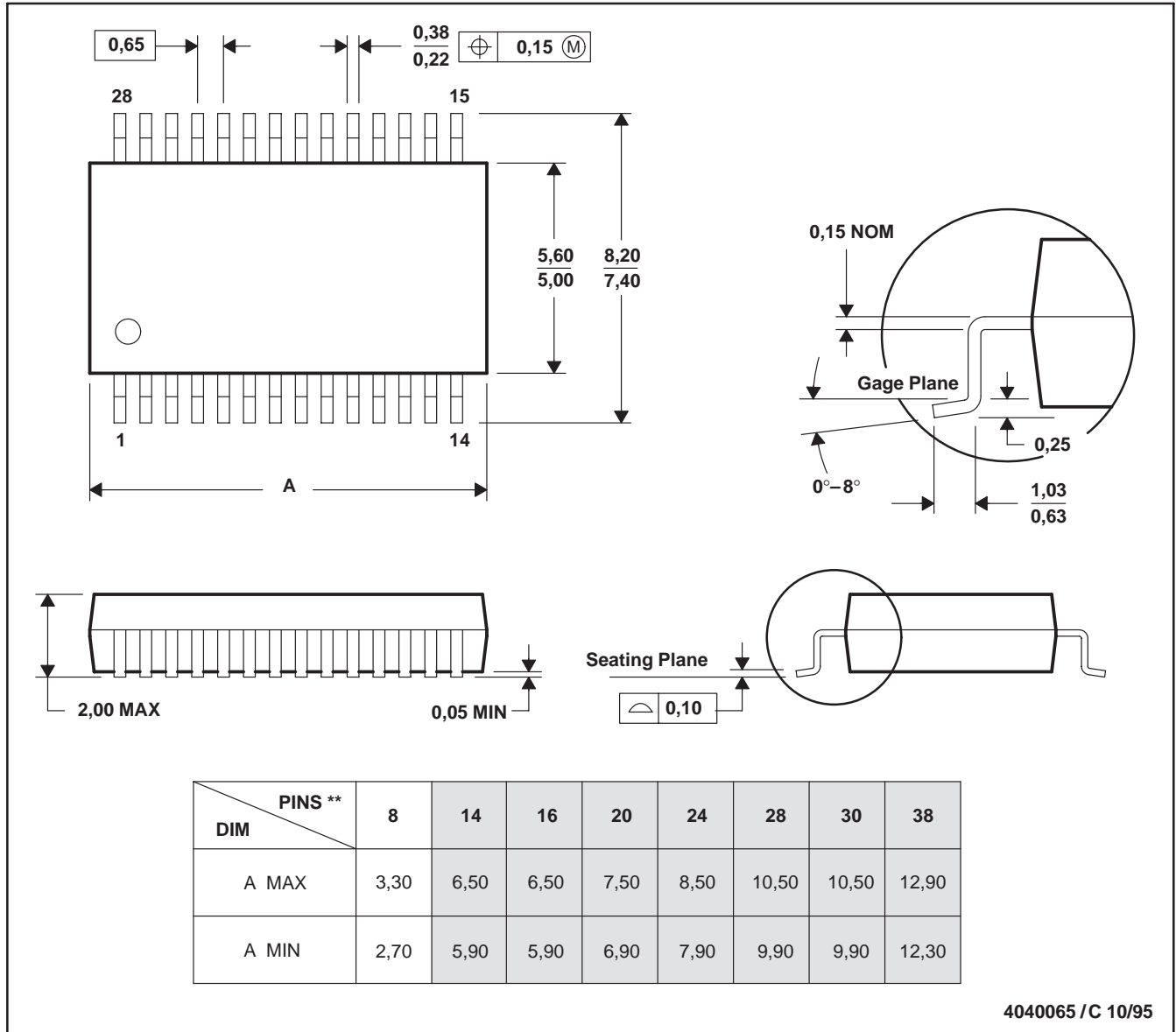
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN

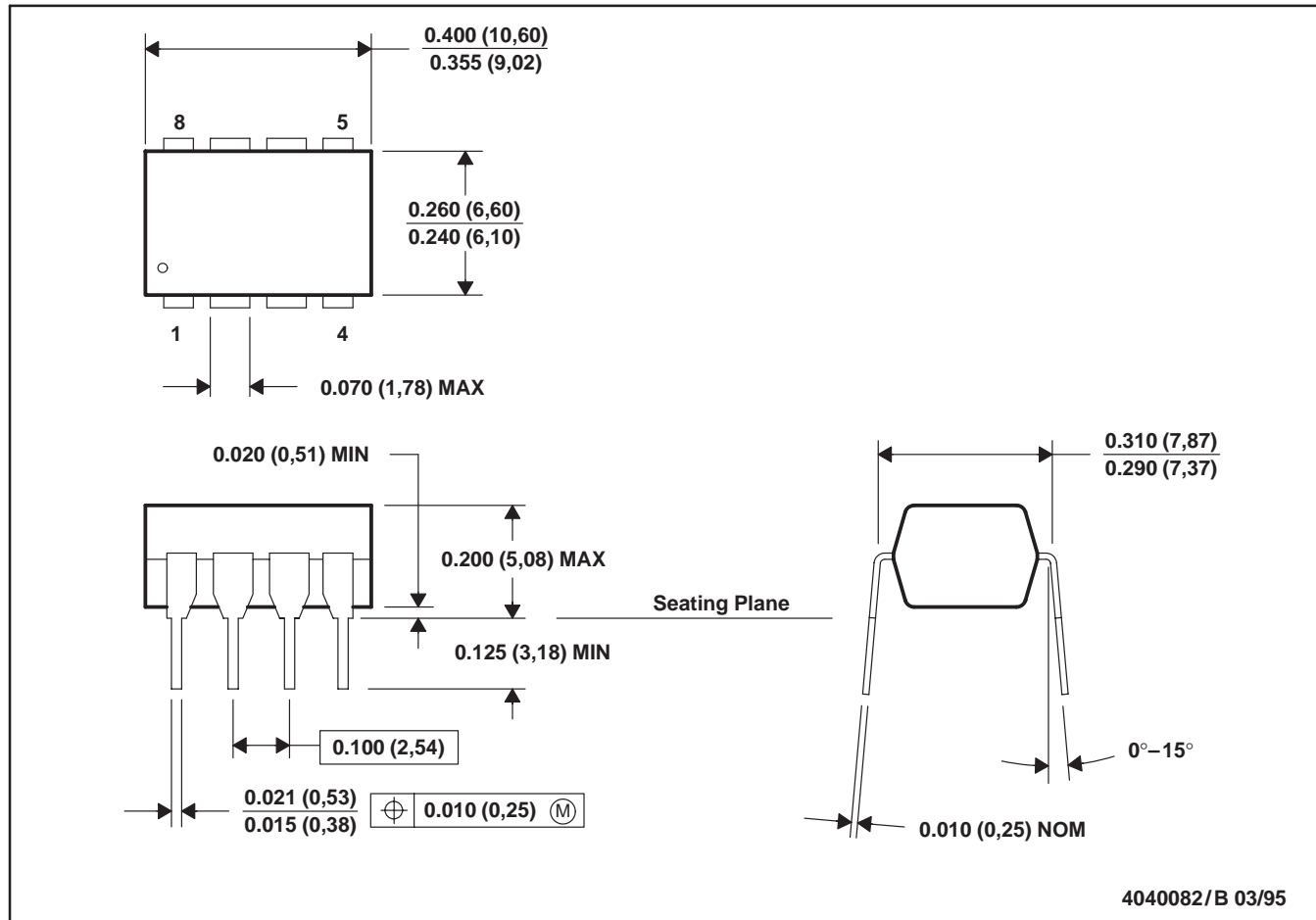


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



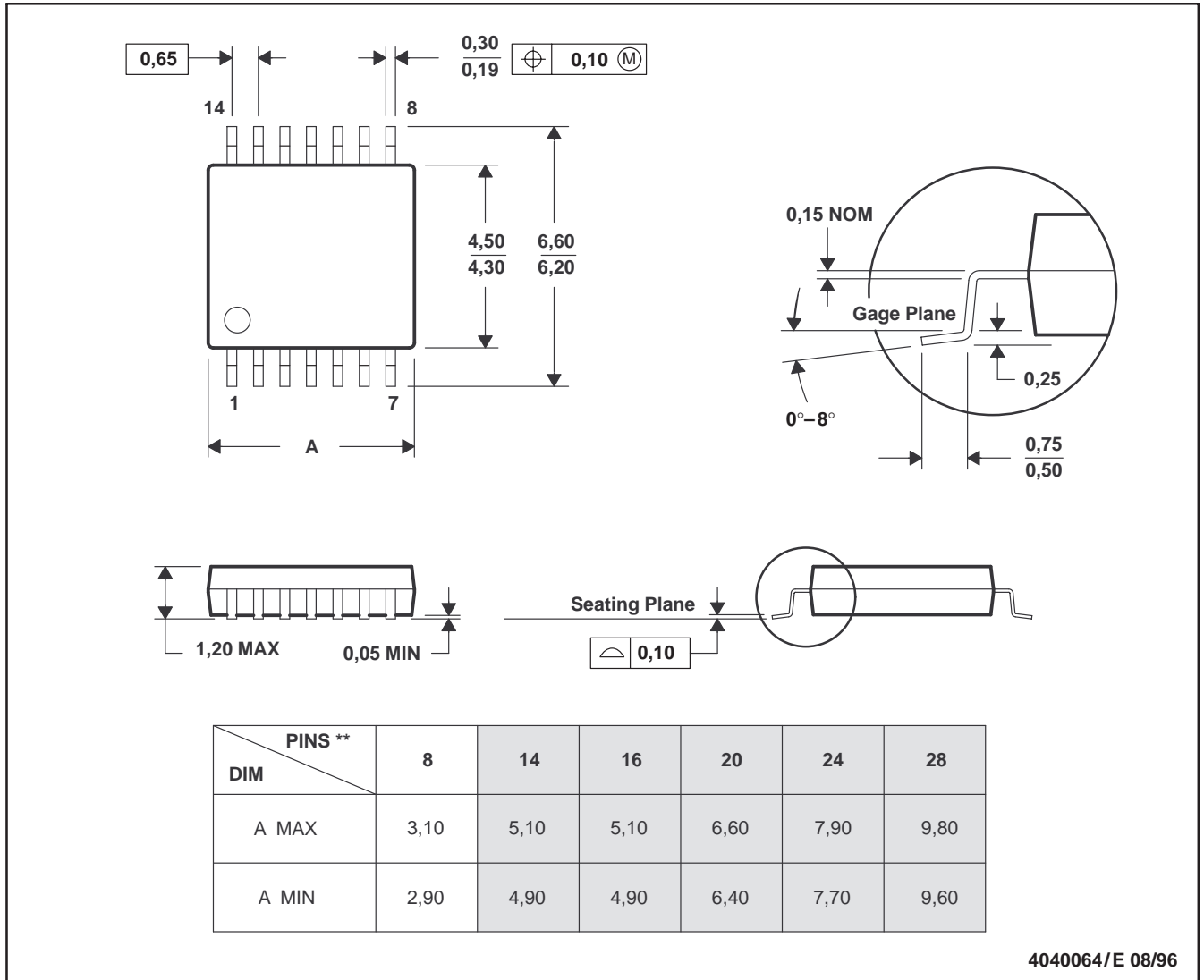
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC551CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	551C	Samples
TLC551CP	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC551CP	
TLC551CPE4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC551CP	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

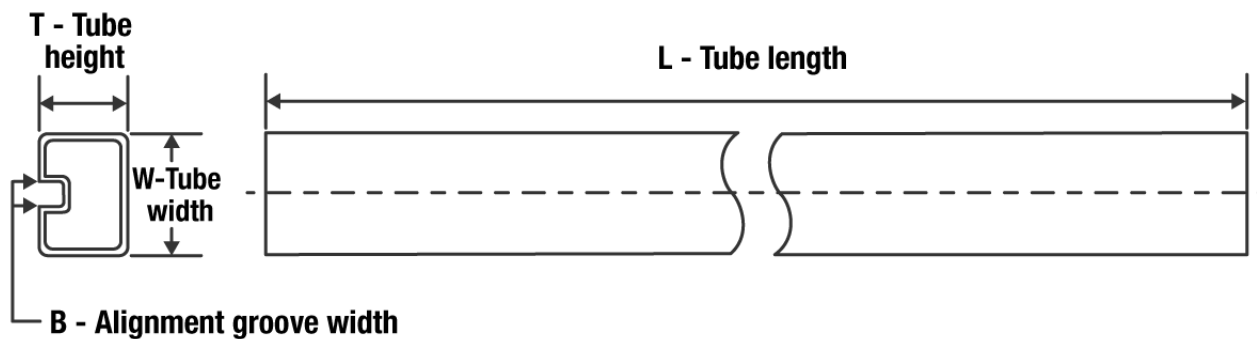
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC551CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC551CD	D	SOIC	8	75	507	8	3940	4.32
TLC551CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC551CPE4	P	PDIP	8	50	506	13.97	11230	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated