TPS1211-Q1 具有保护和诊断功能的 45V 汽车智能高侧驱动器

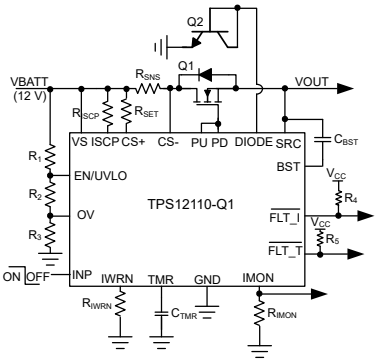
ADVANCE INFORMATION

1 特性

- 具有符合 AEC-Q100 标准的下列特性
  - 器件温度等级 1：
    - –40°C 至 +125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 功能安全型
  - 有助于进行功能安全系统设计的文档
- 3.5V 至 40V 输入范围（绝对最大值 45V）
- 具有 100µA 容量的集成 12V 电荷泵
- 1.7µA 低关断电流（EN/UVLO = 低电平）
- 强大的上拉和下拉栅极驱动器：4A
- 驱动外部背对背 N 沟道 MOSFET
- 具有集成预充电开关驱动器 (TPS12111-Q1) 以驱动容性负载的型号
- 具有可调节响应时间 (TMR) 和故障标志输出 ($\overline{FLT\_I}$) 的两级可调过流保护（IWRN、ISCP）
- 快速短路保护：1.2µs (TPS12111-Q1)、5µs (TPS12110-Q1)
- 精确的模拟电流监测输出 (IMON) – 在 30mV 下为 ±2% (Vsense)
- 可调节欠压锁定 (UVLO) 和过压保护 (OV)
- 具有故障标志输出 ($\overline{FLT\_T}$) 的远程过热检测 (DIODE)
- 与 TPS4811-Q1 引脚对引脚兼容

2 应用

- 配电盒
- 车身控制模块
- 直流/直流转换器



适用于加热器负载的智能高侧驱动器

3 说明

TPS1211-Q1 系列是一款具有保护和诊断功能的 45V 智能高侧驱动器。该器件具有 3.5V 至 40V 的宽工作电压范围，适用于 12V 系统设计。

它具有强大的 4A 灌电流 (PD) 和拉电流 (PU) 栅极驱动器，可在大电流系统设计中使用并联 FET 进行电源开关。将 INP 用作栅极驱动器控制输入。

该器件具有精确的电流检测（在 30mV 下为 ±2%）输出 (IMON) 支持系统，可用于能源管理。该器件集成了具有 $\overline{FLT\_I}$ 输出的两级过流保护，具有完全可调的阈值和响应时间。可以配置自动重试和锁存故障行为。该器件具有远程过热保护，具有 $\overline{FLT\_T}$ 输出。

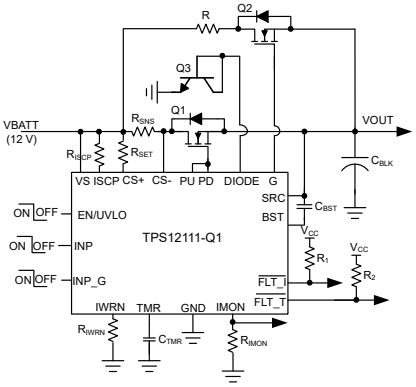
TPS12111-Q1 将预充电驱动器 (G) 与控制输入 (INP_G) 集成，此功能支持必须驱动大容性负载的设计。在关断模式下 (EN/UVLO < 0.3V)，控制器的 IQ 为 1.7µA。

TPS1211-Q1 可采用 19 引脚 VSSOP 封装。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
TPS12110-Q1、TPS12111-Q1	DGX（VSSOP、19）	5.10mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



适用于直流/直流转换器的断路器

ADVANCE INFORMATION

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2022) to Revision A (September 2022)	Page
• 进行了全面更新以包含 TPS12110-Q1 可订购产品	1

5 Device Comparison Table

	TPS12110-Q1	TPS12111-Q1
Overvoltage protection	Yes	No
Precharge driver	No	Yes
Short-circuit protection response time	5 µs	1.2 µs
Overtemperature fault response	Auto-retry with fixed 512-ms timer	Latch-off

6 Pin Configuration and Functions

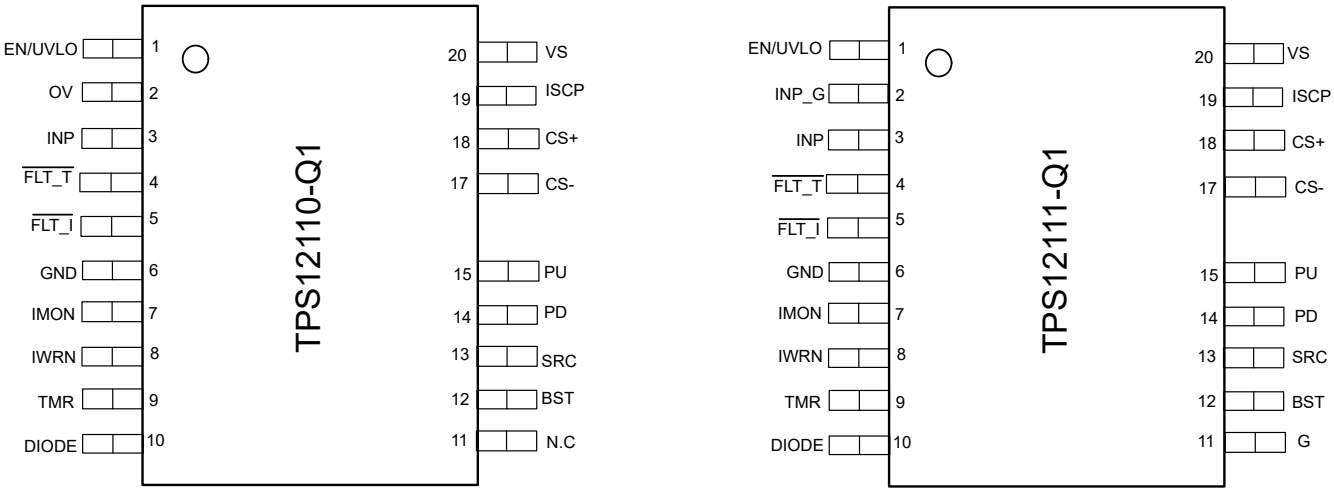


图 6-1. VSSOP 19-Pin DGX Top View

表 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TPS12110-Q1	TPS12111-Q1		
	DGX-19 (VSSOP)			
EN/UVLO	1	1	I	EN/UVLO input. A voltage on this pin above 1.21 V enables normal operation. Forcing this pin below 0.3 V shuts down the TPS1211x-Q1, reducing quiescent current to approximately 3 µA (typical). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pulldown of 100 nA pulls EN/UVLO low and keeps the device in OFF state.
OV	2	—	I	Adjustable overvoltage threshold input. Connect a resistor ladder from input supply, OV to GND. When the voltage at OVP exceeds the over voltage cutoff threshold then the PD is pulled down to SRC turning OFF the external FET. When the voltage at OV goes below OV falling threshold then PU gets pulled up to BST, turning ON the external FET. OV must be connected to GND when not used. When OV is left floating an internal pulldown of 100 nA pulls OV low and keeps PU pulled up to BST.
INP_G	—	2	I	Input signal. CMOS compatible input reference to GND that sets the state of G pin. INP_G has an internal pulldown to GND to keep G pulled to SRC when INP_G is left floating.
INP	3	3	I	Input S=signal. CMOS compatible input reference to GND that sets the state of PD and PU pins. INP has an internal pulldown to GND to keep PD pulled to SRC when INP is left floating.

ADVANCE INFORMATION

ADVANCE INFORMATION

表 6-1. Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	TPS12110-Q1	TPS12111-Q1		
	DGX-19 (VSSOP)			
$\overline{FLT\_T}$	4	4	O	Open drain fault output. This pin asserts low when overtemperature fault is detected.
$\overline{FLT\_I}$	5	5	O	Open drain fault output. This pin asserts low after the voltage on the TMR pin has reached the fault threshold of 1.1V. this pin indicates the pass transistor is about to turn off due to an overcurrent condition. The $\overline{FLT\_I}$ pin does not go to a high-impedance state until the overcurrent condition and the auto-retry time expire.
GND	6	6	G	Connect GND to system ground
IMON	7	7	O	Analog current monitor output. This pin sources a scaled down ratio of current through the external current sense resistor RSNS. A resistor from this pin to GND converts current to proportional voltage. If unused, connect it to GND.
IWRN	8	8	I	Overcurrent detection setting. A resistor across IWRN to GND sets the over current comparator threshold. Connect IWRN to GND if over current protection feature is not desired.
TMR	9	9	I	Fault timer input. A capacitor across TMR pin to GND sets the times for fault warning, fault turn-off ($\overline{FLT\_I}$) and retry periods. Leave it open for fastest setting. Connect TMR to GND to disable overcurrent protection.
DIODE	10	10	I	Diode connection for temperature sensing. Connect it to base and collector of an MMBT3904 NPN BJT. Connect DIODE to GND, if remote over temperature sensing and protection feature is not desired.
G	—	11	O	GATE of external Precharge FET. Connect to the GATE of the external FET
N.C	11	—	—	No connect
BST	12	12	O	High-side bootstrapped supply. An external capacitor with a minimum value of > Qg(tot) of the external FET must be connected between this pin and SRC.
SRC	13	13	O	Source connection of the external FET
PD	14	14	O	High current gate driver pulldown. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.
PU	15	15	O	High current gate driver pullup. This pin pulls up to BST. Connect this pin to PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the inrush current during turn-on.
CS-	17	17	I	Current sense negative input
CS+	18	18	I	Current sense positive input. Connect a 100-Ω resistor across CS+ to the external current sense resistor.
ISCP	19	19	I	I short-circuit detection threshold setting. Connect ISCP to CS – if short-circuit protection is not desired.
VS	20	20	Power	Supply pin of the controller

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	VS, CS+, CS – , ISCP to GND	– 1	45	V
	VS, CS+, CS – to SRC	– 60	45	
	SRC to GND	– 30	45	
	PU, PD, G, BST to SRC	– 0.3	16	
	TMR, IWRN, DIODE to GND	– 0.3	5.5	
	OV, EN/UVLO, INP, INP_G, $\overline{FLT\_I}$, $\overline{FLT\_T}$ to GND	– 1	20	
	CS+ to CS –	– 0.3	0.3	
	$I_{(FLT\_I)}$, $I_{(FLT\_T)}$		10	mA
	$I_{(CS+)}$ to $I_{(CS-)}$, 1ms	– 100	100	
Output Pins	PU, PD, G, BST to GND	– 30	60	V
	IMON to GND	– 1	5.5	
Operating junction temperature, T_j (2)		– 40	150	°C
Storage temperature, T_{stg}		– 40	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, DIODE, G, VS)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	VS, CS+, CS- to GND	0		40	V
	EN/UVLO, OV to GND	0		15	
Output Pins	$\overline{FLT\_I}$, $\overline{FLT\_T}$ to GND	0		15	
	IMON to GND	0		5	
External Capacitor	VS, SRC to GND	22			nF
	BST to SRC	0.1			µF
Tj	Operating Junction temperature(2)	– 40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

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7.4 Thermal Information

THERMAL METRIC(1)		TPS1211x-Q1 DGX 19 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

7.5 Electrical Characteristics

T_J = – 40 ℃ to +125℃. $V_{(S)} = V_{(CS+)} = V_{(CS-)}$ = 12 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_S	Operating input voltage		3.5		40	V
$V_{(S\_PORR)}$	Input supply POR threshold, rising			3		V
$V_{(S\_PORF)}$	Input supply POR threshold, falling			2.9		V
	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V		500		µA
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V		3		µA
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.16	1.18	1.2	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.11	1.12	1.15	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.3			V
OVER VOLTAGE PROTECTION (OV) INPUT – TPS12110-Q1 Only						
$V_{(OVR)}$	Overvoltage threshold input, risIng	TPS12110-Q1 Only	1.16	1.18	1.2	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.11	1.12	1.15	V
CHARGE PUMP (BST-SRC)						
$I_{(BST)}$	Charge Pump Supply current	$V_{(BST-SRC)}$ = 10 V	70	100		µA
$V_{(BST-SRC)}$	Charge Pump Turn ON voltage		11			V
	Charge Pump Turnoff voltage				13	V
$V_{(BST\ UVLO)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, rising				8	V
	$V_{(BST-SRC)}$ UVLO voltage threshold, falling		6			V
$V_{(BST-SRC)}$	Charge Pump Voltage at $V_{(S)}$ = 3.5 V		8			V
GATE DRIVER OUTPUTS (PU, PD, G)						
$I_{(PU)}$	Peak Source Current			3.7		A
$I_{(PD)}$	Peak Sink Current			4		A
$I_{(G)}$	Gate charge (sourcing) current, on state	TPS12111-Q1 Only		100		µA
	Gate discharge (sinking) current, off state			135		mA
CURRENT SENSE AND OVER CURRENT PROTECTION (CS+, CS-, IMON, ISCP, IWRN)						
$V_{(OS\_SET)}$	Input referred offset (V_{SNS} to V_{IMON} scaling)	R_{SET} = 100Ω, R_{IMON} = 5kΩ, 10kΩ (corresponds to V_{SNS} = 6mV to 30mV) Gain of 45 and 90 respectively.	– 350		350	µV

7.5 Electrical Characteristics (continued)

T_J = –40 ℃ to +125℃. $V_{(S)} = V_{(CS+)} = V_{(CS-)}$ = 12 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SNS\_WRN)}$	OCP threshold threshold	R_{SET} = 100Ω $R_{(IWRN)}$ = 39.7 kΩ	28	30	32	mV
	OCP threshold threshold	R_{SET} = 100Ω $R_{(IWRN)}$ = 120 kΩ		10		mV
I_{SCP}	SCP Input Bias current		13	15	17	µA
$V_{(SNS\_SCP)}$	SCP threshold	$R_{(ISCP)}$ = 2.1 kΩ	35	40	45	mV
		$R_{(ISCP)}$ = 750 Ω		20		mV
DELAY TIMER (TMR)						
$I_{(TMR\_SRC\_CB)}$	TMR source current			77		µA
$I_{(TMR\_SRC\_FLT)}$	TMR source current			2.5		µA
$I_{(TMR\_SNK)}$	TMR sink current			2.5		µA
FAULT FLAG ($\overline{FLT\_I}$, $\overline{FLT\_T}$), INPUT CONTROLS (INP, INP_G)						
$R_{(\overline{FLT\_T})}$	$\overline{FLT}$ Pull-down resistance			70		Ω
$I_{(\overline{FLT\_T})}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 20 V			400	nA
$V_{(INP\_H)}$					2	V
$V_{(INP\_L)}$			0.8			V
$V_{(INP\_G\_H)}$		TPS12111-Q1 Only			2	V
$V_{(INP\_G\_L)}$			0.8			V
TEMPERATURE SENSING AND PROTECTION (DIODE)						
$I_{(DIODE)}$	External diode current source	High level		160		µA
		Low level		10		µA
	Diode current ratio			16		A/A
$T_{(DIODE\_TSD\_rising)}$	DIODE sense TSD rising threshold			155		℃

7.6 Switching Characteristics

T_J = –40 ℃ to +125℃. $V_{(CS+)} = V_{(CS-)}$ = 12 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PU(INP\_H)}$	INP Turn ON propogation Delay	INP ↑ to PU ↑, C_L = 47 nF		2		µs
$t_{PD(INP\_L)}$	INP Turn OFF propogation Delay	INP ↓ to PD ↓, C_L = 47 nF		1		µs
$t_{G(INP\_G\_H)}$	INP_G Turn ON propogation Delay	INP_G ↑ to G ↑, C_L = 1 nF, TPS12111-Q1 Only		25		µs
$t_{G(INP\_G\_L)}$	INP_G Turn OFF propogation Delay	INP_G ↓ to G ↓, C_L = 1 nF, TPS12111-Q1 Only		1		µs
$t_{PD(UVLO\_OFF)}$	UVLO Turn OFF Propogation Delay	UVLO ↓ to PD ↓, C_L = 47 nF		4		µs
$t_{PD(VS\_OFF)}$	PD Turn OFF delay during input supply (Vs) interruption	Vs ↓ $V_{(SPOR\_F)}$ to PD ↓, C_L = 47 nF, INP = EN/UVLO = 2 V		40		µs
$t_{PU(VS\_ON)}$	PU Turn ON delay during input supply (Vs) recovery	VS ↑ $V_{(SPOR\_R)}$ to PU ↑, C_L = 47 nF, INP = EN/UVLO = 2 V, $V_{(BST-SRC)}$ > $V_{(BST\ UVLOR)}$		350		µs
$t_{PU(EN\_ON)}$	PU Turn ON delay during transition from shutdown mode to active mode with C_{BST} pre-biased	EN/UVLO ↑ to PU ↑, C_L = 47 nF, INP = 2 V, $V_{(BST-SRC)}$ > $V_{(BST\ UVLOR)}$		350		µs
$t_{PD(OV\_OFF)}$	OV Turn Off progopation Delay	OV ↑ to PD ↓, C_L = 47 nF, TPS12110-Q1 Only		3		µs
$t_{(SC)}$	Short Circuit Protection propogation Delay	(V_{CS+} – V_{CS-}) ↑ $I_{(SC)}$ to PD ↓, C_L = 47 nF, TPS12110-Q1 Only		5		µs
		(V_{CS+} – V_{CS-}) ↑ $I_{(SC)}$ to PD ↓, C_L = 47 nF, TPS12111-Q1 Only		1.2		µs

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7.6 Switching Characteristics (continued)

T_J = –40 ℃ to +125℃. $V_{(CS+)}$ = $V_{(CS-)}$ = 12 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(OC)}$	Over current protection delay	(V_{CS+} – V_{CS-}) ↑ $I_{(OC)}$ to PD ↓, C_L = 47 nF, $C_{(TMR)}$ = 0 nF		24		µs
		(V_{CS+} – V_{CS-}) ↑ $I_{(OC)}$ to PD ↓, C_L = 47 nF, $C_{(TMR)}$ = 18 nF		312		µs
$t_{FLT\_I(IFLT\_ASSERT)}$	$\overline{FLT}$_I assertion delay			290		µs
$t_{FLT\_I(IFLT\_DE\_ASSERT)}$	$\overline{FLT}$_I de-assertion delay			260		µs
$t_{FLT\_T(AR)}$	TSD Auto-retry	TPS12110-Q1 Only		512		ms

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TPS1211-Q1 family is a 45-V smart high-side drivers with protection and diagnostics. With wide operating voltage range of 3.5 V – 40 V, the device is suitable for 12-V system designs.

The device has a strong 4-A sink (PD) and source (PU) gate driver that enables power switching using parallel FETs in high current system designs. Use INP as the gate driver control input. MOSFET slew rate control (ON and OFF) is possible by placing external R-C components.

The device has accurate current sensing (±2% at 30 mV) output (IMON) enabling systems for energy management. The device has integrated two-level, overcurrent protection with $\overline{FLT\_I}$ output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured.

The device features remote overtemperature protection with $\overline{FLT\_T}$ output enabling robust system protection.

TPS12110-Q1 has an accurate overvoltage protection (±3%), providing robust load protection.

The TPS12111-Q1 integrates a precharge driver (G) with control input (INP_G). This feature enables system designs that must drive large capacitive loads by precharging first and then turning ON the main power FETs.

TPS1211-Q1 has an accurate undervoltage protection (±3%) using the EN/UVLO pin. Pull EN/UVLO low (< 0.3 V) to turn OFF the device and enter into shutdown mode. In shutdown mode, the controller draws a total I_Q of 3 µA (maximum) at 12-V supply input.

8.2 Functional Block Diagram

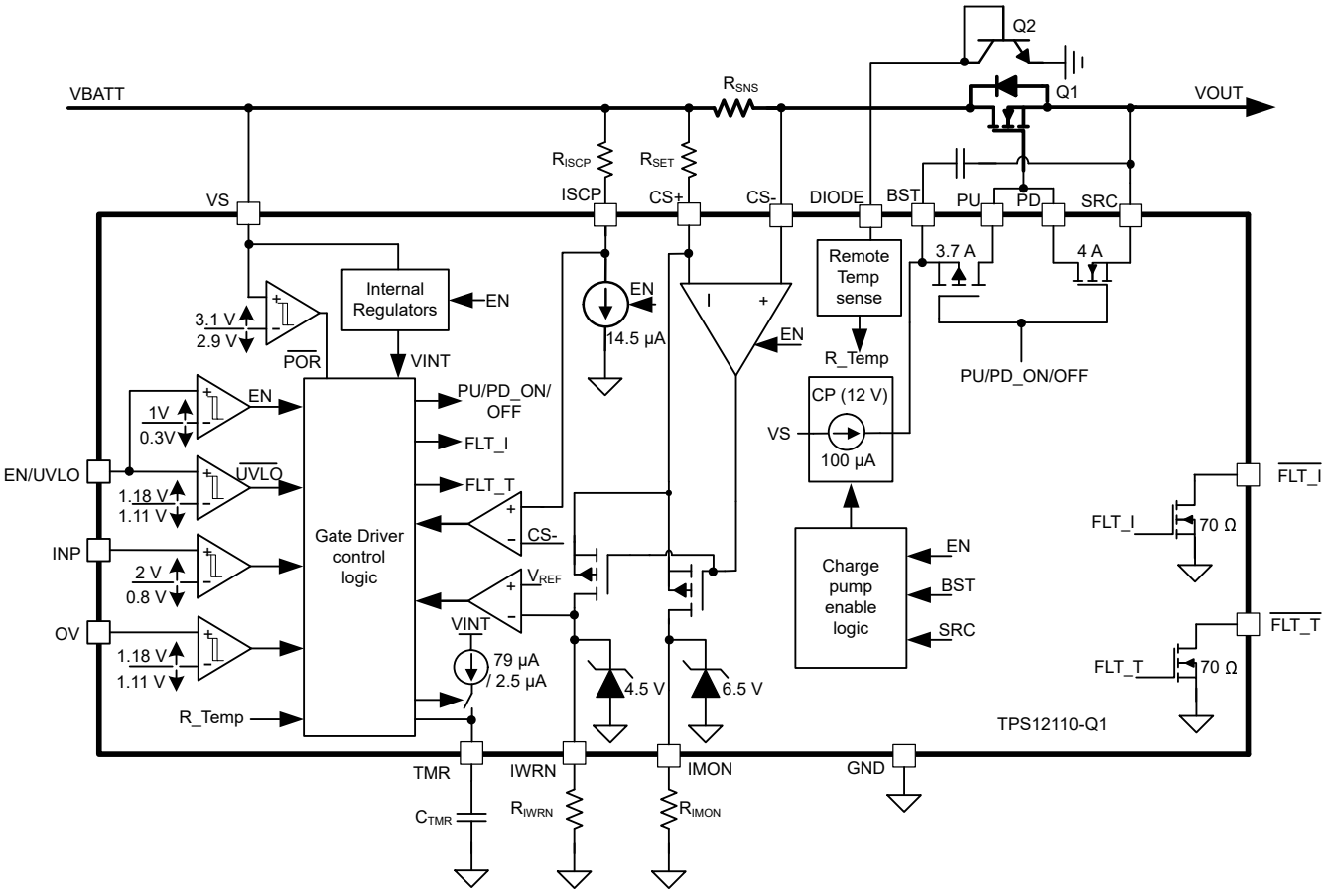

图 8-1. TPS12110-Q1 Functional Block Diagram

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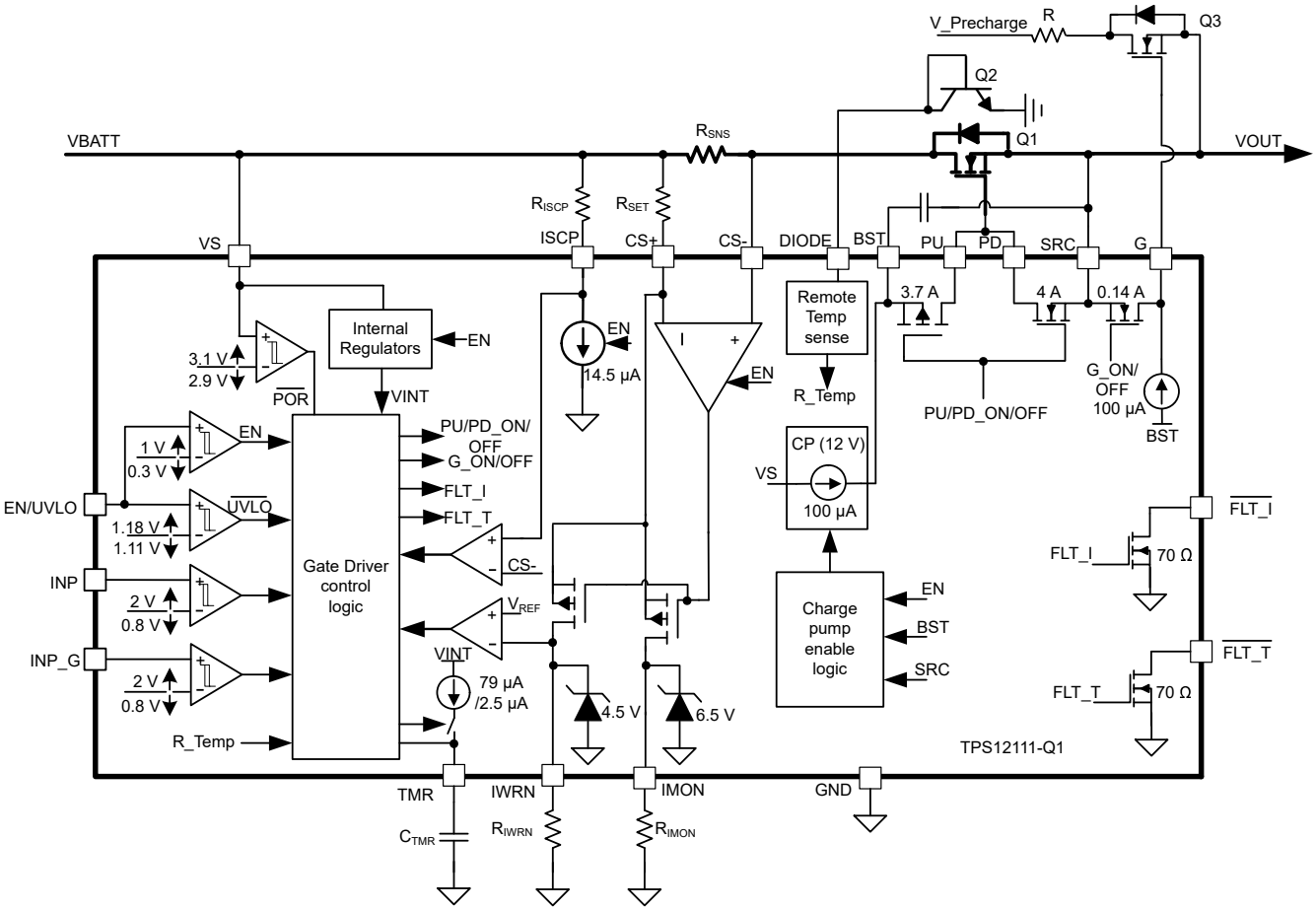

图 8-2. TPS12111-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 Charge Pump and Gate Driver Output (VS, PU, PD, BST, SRC)

图 8-3 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 3.7-A source and 4-A sink gate drivers. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 12-V, 100-µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C_{BST} that is placed across the gate driver (BST and SRC).

In switching applications, if the charge pump supply demand is higher than 100 µA, then supply BST externally using a low leakage diode and 12-V supply as shown in the 图 8-3.

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C_{BST} capacitor. After the voltage across C_{BST} crosses $V_{(BST\_UVLOR)}$, the GATE driver section is activated. The device has a 1-V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C_{BST} based on the external FET QG and allowed dip during FET turn-ON. The charge pump remains enabled until the BST to SRC voltage reaches 12.3 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 11.7 V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 12.3 V and 11.7 V as shown in the 图 8-4.

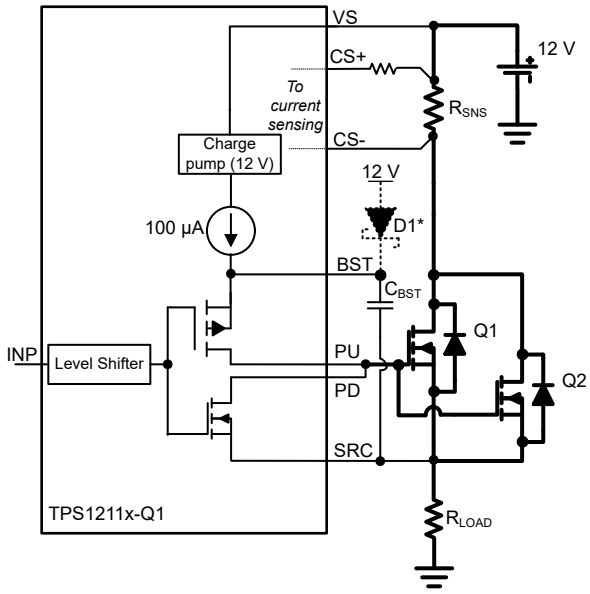

图 8-3. Gate Driver

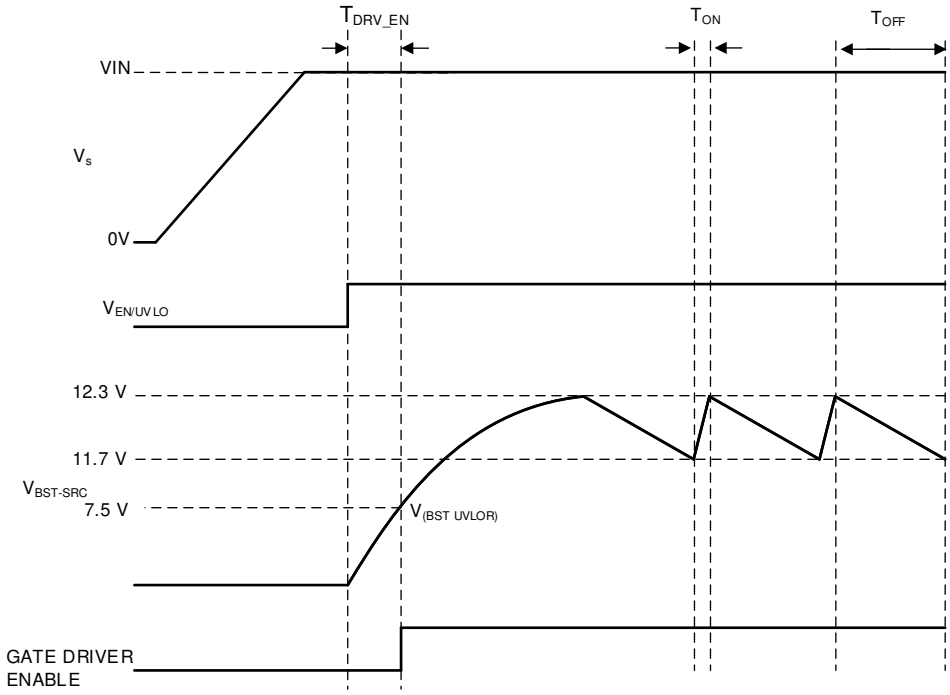

图 8-4. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay.

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{100\ \mu A} \quad (1)$$

Where,

$C_{(BST)}$ is the charge pump capacitance connected across BST and SRC pins.

$V_{(BST\_UVLOR)}$ = 7.5 V (typical).

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If T_{DRV_EN} must be reduced, then pre-bias the BST terminal externally using an external 12-V supply through a low leakage diode D1 as shown in 图 8-3. With this connection, T_{DRV_EN} reduces to 350 µs.

8.3.2 Capacitive Load Driving

Certain end equipments like automotive power distribution unit power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur potentially damaging the power FETs.

To limit the inrush current during capacitive load switching, the following system design techniques can be used with TPS1211x-Q1 devices.

8.3.2.1 FET Gate Slew Rate Control

For limiting inrush current during turn-ON of the FET with capacitive loads, use R_1, R_2, C_1 as shown in 图 8-5. The R_1 and C_1 components slow down the voltage ramp rate at the gate of the FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

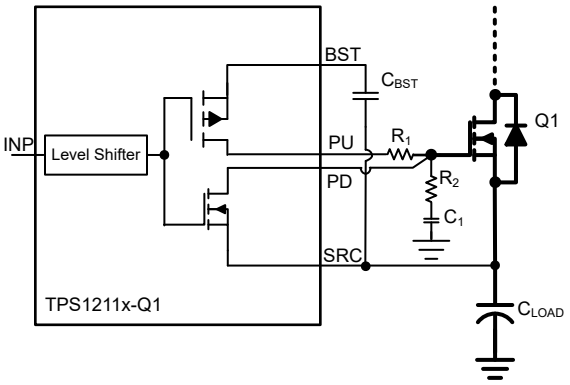

图 8-5. Inrush Current Limiting with FET Gate Slew Rate Control

Use the 方程式 2 to calculate the inrush current during turn-ON of the FET.

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \quad (2)$$

$$I_{INRUSH} = \frac{0.63 \times V_{(BST-SRC)} \times C_{LOAD}}{R_1 \times C_1} \quad (3)$$

Where,

C_{LOAD} is the load capacitance, VBATT is the input voltage and T_{charge} is the charge time, $V_{(BST-SRC)}$ is the charge pump voltage (12 V),

Use a damping resistor R_2 (approximately 10 Ω) in series with C_1. 方程式 3 can be used to compute required C_1 value for a target inrush current. A 100-kΩ resistor for R_1 can be a good starting point for calculations.

Connecting PD pin of TPS1211x-Q1 directly to the gate of the external FET ensures fast turn-OFF without any impact of R_1 and C_1 components.

C_1 results in an additional loading on C_{BST} to charge during turn-ON. Use 方程式 4 to calculate the required C_{BST} value.

$$C_{BST} > Q_{g(total)} + 10 \times C_1 \quad (4)$$

Where, $Q_{g(total)}$ is the total gate charge of the FET.

8.3.2.2 Using Precharge FET - (with TPS12111-Q1 Only)

In high-current applications where several FETs are connected in parallel, the gate slew rate control for the main FETs is not recommended due to unequal distribution of inrush currents among the FETs. This action makes FET selection complex and results in over sizing of the FETs.

The TPS12111-Q1 integrates precharge gate driver (G) with a dedicated control input (INP_G). This feature can be used to drive a separate FET that can be used to precharge the capacitive load. 图 8-6 shows the precharge FET implementation for capacitive load charging using TPS12111-Q1. An external capacitor C_g reduces the gate turn-ON slew rate and controls the inrush current.

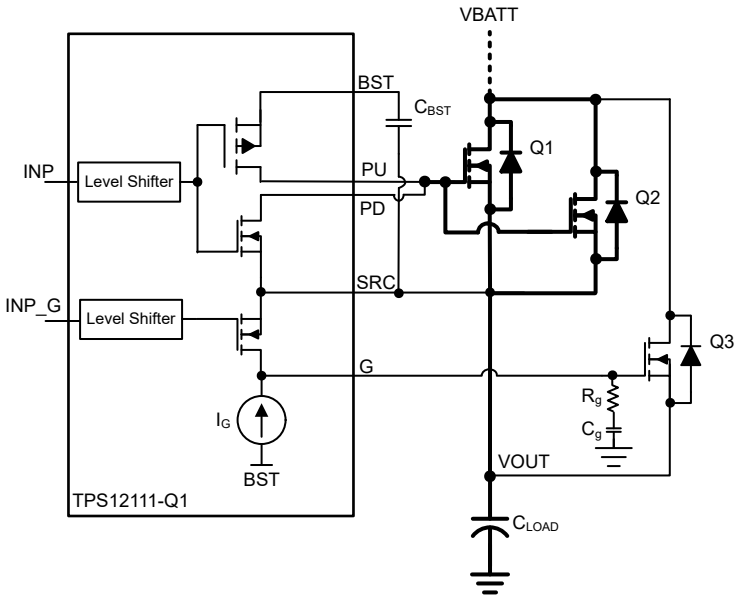

图 8-6. Capacitor Charging Using Gate Slew Rate Control of Precharge FET

During power up with EN/UVLO high and $C_{(BST)}$ voltage above $V_{(BST\_UVLOR)}$ threshold, INP and INP_G controls are active. For the precharge functionality, drive INP low to keep the main FETs OFF and drive INP_G high. G output gets pulled up to BST with I_G. Use 方程式 5 to calculate the required C_g value.

$$I_G = C_g \times \frac{I_{INRUSH}}{C_{OUT}} \quad (5)$$

Where,

I_G is 100 µA (typical),

Use 方程式 2 to calculate the I_{INRUSH}.

A series resistor R_g must be used in conjunction with C_g to limit the discharge current from C_g during turn-off . The recommended value for Rg is between 220 Ω to 470 Ω. After the output capacitor is charged, turn OFF the precharge FET by driving INP_G low. G gets pulled low to SRC with an internal 135-mA pulldown switch. The main FETs can be turned ON by driving INP high.

图 8-7 shows other system design approaches to charge large output capacitors in high current applications. The designs involve an additional power resistor in series in series with precharge FET. The back-to-back FET topology shown is typically used in bi-directional power control applications like battery management systems.

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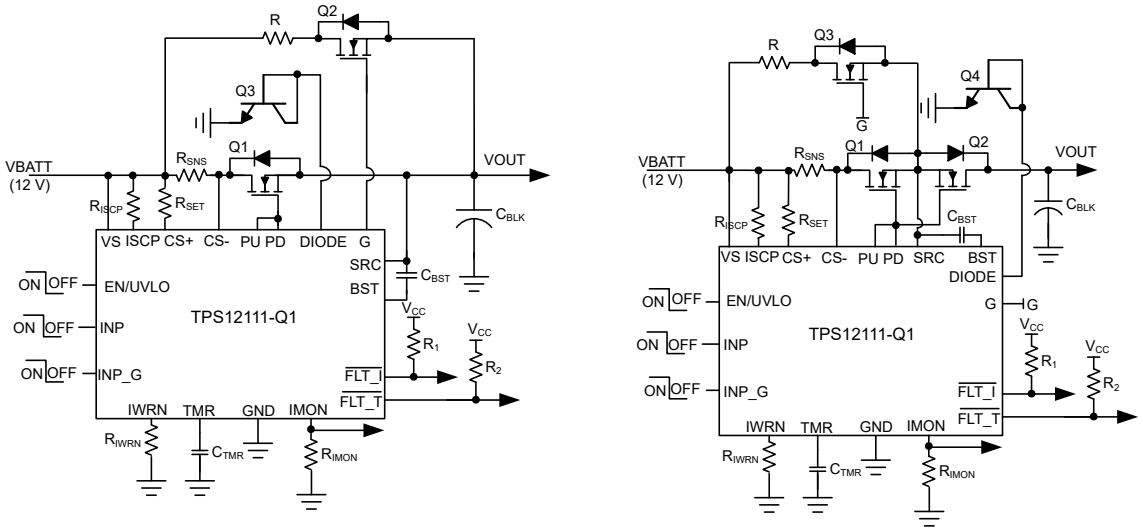

图 8-7. TPS12111-Q1 application Circuits for Capacitive Load Driving Using Precharge FET and a Series Power Resistor

8.3.3 Overcurrent and Short-Circuit Protection

TPS1211x-Q1 has two-level current protection.

- Adjustable overcurrent protection (I_{OC}) threshold and response time (T_{OC}),
- Adjustable short-circuit threshold (I_{SC}) with internally fixed fast response (T_{SC}).

图 8-8 shows the I-T characteristics.

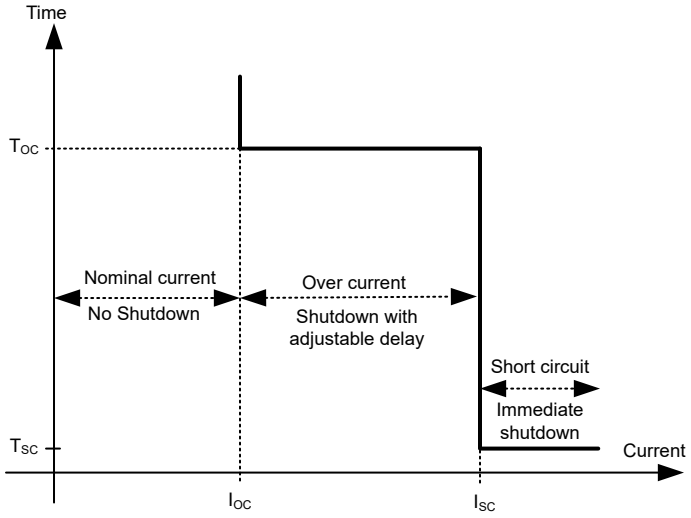

图 8-8. Overcurrent and Short-Circuit Protection Characteristics

The device senses the voltage across the external current sense resistor through CS+ and CS–. Set the overcurrent protection threshold using an external resistor R_{IWRN} across IWRN and GND. Use 方程式 6 to calculate the required R_{IWRN} value.

$$R_{IWRN}\ (\Omega) = \frac{11.9 \times R_{SET}}{R_{SNS} \times I_{OC}} \tag{6}$$

Where, R_{SET} is the resistor connected across CS+ and VS, R_{SNS} is the current sense resistor, and I_{OC} is the overcurrent level.

8.3.3.1 Overcurrent Protection with Auto-Retry

The $C_{(TMR)}$ programs the over current protection delay (T_{OC}) and auto-retry time (T_{RETRY}). Once the voltage across CS+ and CS – exceeds the set point, the $C_{(TMR)}$starts charging with 77-µA pullup current. After the $C_{(TMR)}$charges up to $V_{(TMR\_FLT)}$, $\overline{FLT\_I}$ asserts low providing warning on impending FET turn OFF. After $C_{(TMR)}$ charges to $V_{(TMR\_OC)}$, PD pulls low to SRC turning OFF the FET. Post this event, the auto-retry behavior starts. The $C_{(TMR)}$ capacitor starts discharging with 2.5-uA pulldown current. After the voltage reaches $V_{(TMR\_Low)}$ level, the capacitor starts charging with 2.5-uA pullup. After 32 charging, discharging cycles of $C_{(TMR)}$the FET turns ON back and $\overline{FLT\_I}$ de-asserts after de-assertion delay of 260 µs.

Use 方程式 7 to calculate the T_{OC} duration.

$$T_{OC} = \frac{1.2 \times C_{TMR}}{77.5\ \mu} \tag{7}$$

Where, T_{OC} is the delay to turn OFF the FET, C_{TMR} is the capacitance across TMR to GND.

Use 方程式 8 to calculate the T_{FLT} duration.

$$T_{FLT} = \frac{1.1 \times C_{TMR}}{77.5\ \mu} \tag{8}$$

Where, T_{FLT} is the $\overline{FLT\_I}$ assertion delay.

The auto-retry time can be computed as, $T_{RETRY} = 22.7 \times 10^6 \times C_{TMR}$.

If the overcurrent pulse duration is below $T_{(OC)}$, then the FET remains ON and $C_{(TMR)}$ gets discharged using internal pulldown switch.

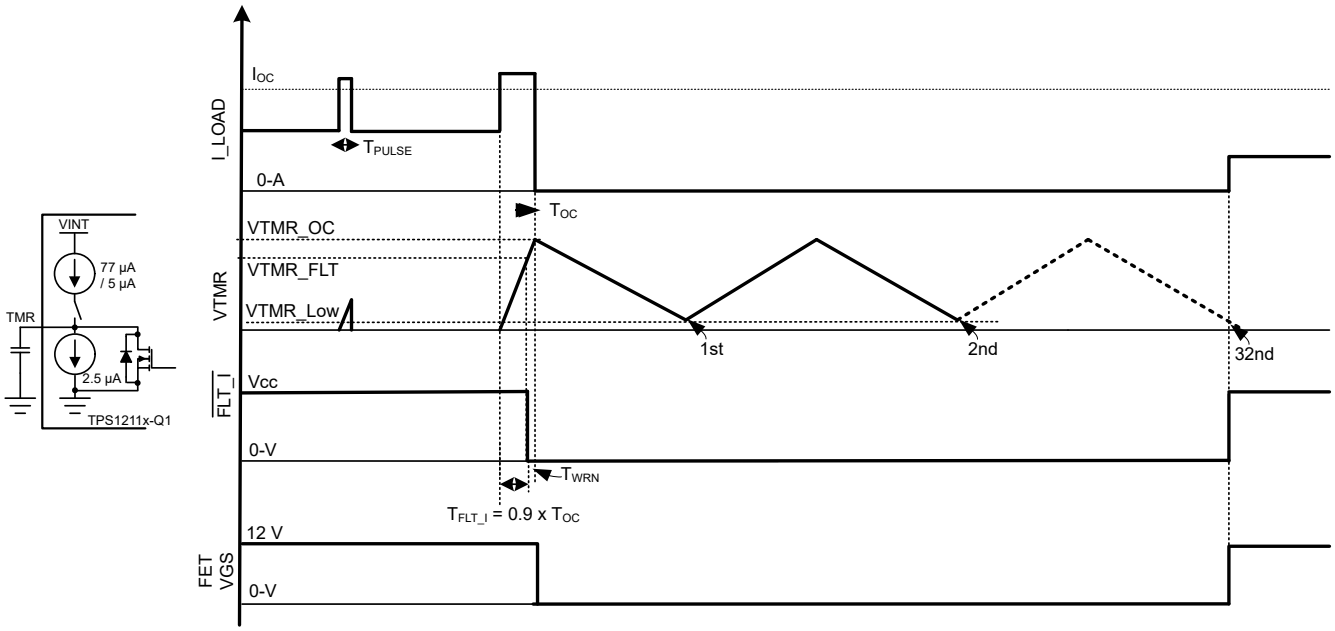

图 8-9. *Overcurrent Protection with Auto-Retry*

8.3.3.2 Overcurrent Protection with Latch-Off

Connect an approximately 100-kΩ resistor across $C_{(TMR)}$ as shown in the following figure. With this resistor, during the charging cycle, the voltage across $C_{(TMR)}$ gets clamped to a level below $V_{(TMR\_OC)}$ resulting in a latch-off behavior.

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Toggle INP or EN/UVLO (below ENF) or power cycle Vs below V_{SPORF} to reset the latch. At low edge, the timer counter is reset and $C_{(TMR)}$ is discharged. PU pulls up to BST when INP is pulled high.

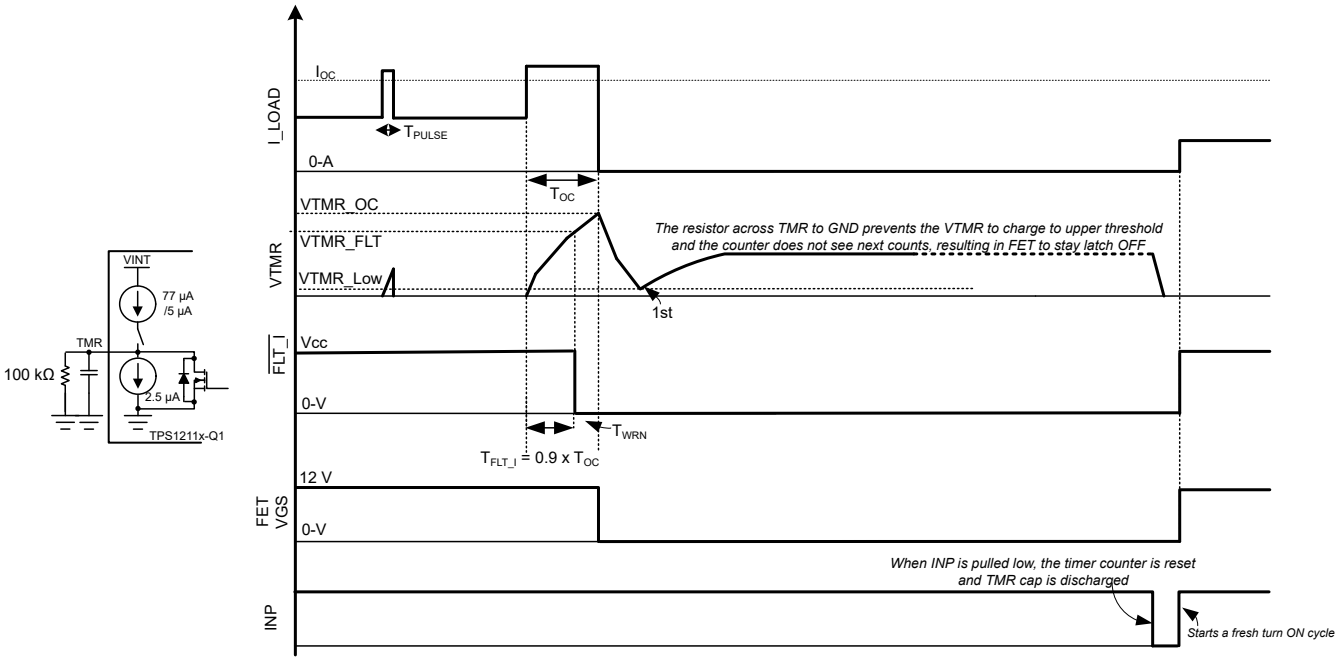

图 8-10. *Overcurrent Protection with Latch-Off*

8.3.3.3 Short-Circuit Protection

Connect a resistor, R_{ISCP}, as shown in 图 8-11.

Use 方程式 9 to calculate the required R_{ISCP} value.

$$R_{ISCP}\ (\Omega) = \frac{I_{SC} \times R_{SNS}}{14.5\ \mu} - 600 \quad (9)$$

Where, RSNS is the current sense resistor, and I_{SC} is the desired short-circuit protection level. After the current exceeds the I_{SC} threshold then, PD pulls low to SRC within 1.2 µs in TPS12111-Q1 and 5 µs in TPS12110-Q1, protecting the FET. $\overline{FLT\_I}$ asserts low at the same time. Subsequent to this event, the charge and discharge cycles of $C_{(TMR)}$ starts similar to the behavior post FET OFF event in the over current protection scheme.

Latch-off can also achieved in the similar way as explained in the overcurrent protection scheme.

8.3.4 Analog Current Monitor Output (IMON)

TPS1211x-Q1 features an accurate analog load current monitor output (IMON) with adjustable gain. The current source at IMON terminal is configured to be proportional to the current flowing through the RSNS current sense resistor. This current can be converted to a voltage using a resistor R_{IMON} from IMON terminal to GND terminal. This voltage, computed using 方程式 10 can be used as a means of monitoring current flow through the system.

Use 方程式 10 to calculate the V_{IMON}.

$$V_{IMON} = (V_{SNS} + V_{OS\_SET}) \times \text{Gain} \quad (10)$$

Where V_{SNS} = ILOAD × R_{SNS} and V_{OS_SET} is the input referred offset (± 350 µV) of the current sense amplifier (V_{SNS} to V_{IMON} scaling). Use the following equation to calculate gain.

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$$\text{Gain} = \frac{0.9 \times R_{IMON}}{R_{SET}} \quad (11)$$

Where 0.9 is the current mirror factor between the current sense amplifier and the IMON pass FET.

The maximum voltage range for monitoring the current (V(IMONmax)) is limited to minimum([V(VS) – 0.5V], 5.5V) to ensure linear output. This puts limitation on maximum value of R_{IMON} resistor. The IMON pin has an internal clamp of 6.5 V (typical).

Accuracy of the current mirror factor is < ± 1%. Use the following equation to calculate the overall accuracy of V_{IMON}.

$$\%\ V_{IMON} = \frac{V_{OS\_SET}}{V_{SNS}} \times 100 \quad (12)$$

图 8-11 shows external connections and simplified block diagram of current sensing and overcurrent protection implementation.

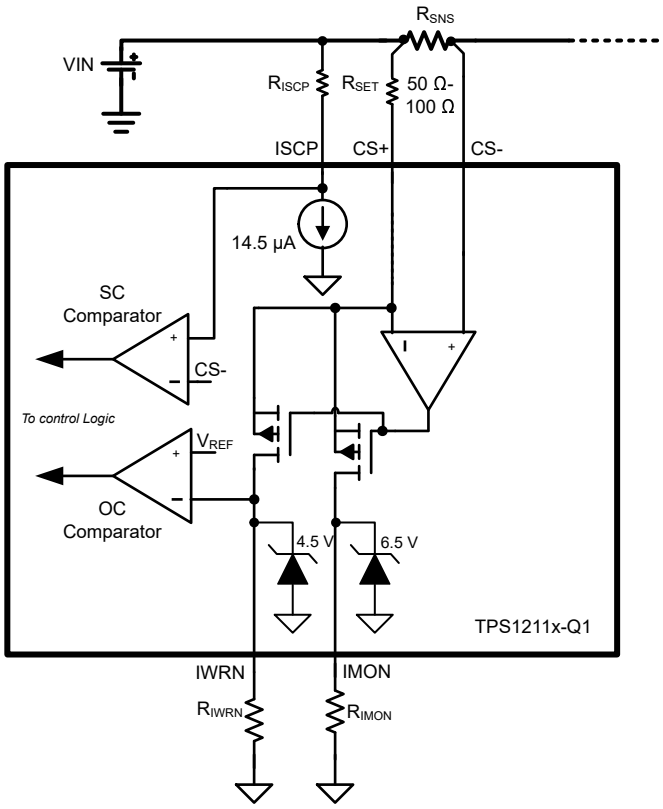

图 8-11. Current Sensing and Overcurrent Protection

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8.3.5 Overvoltage (OV) and Undervoltage Protection (UVLO)

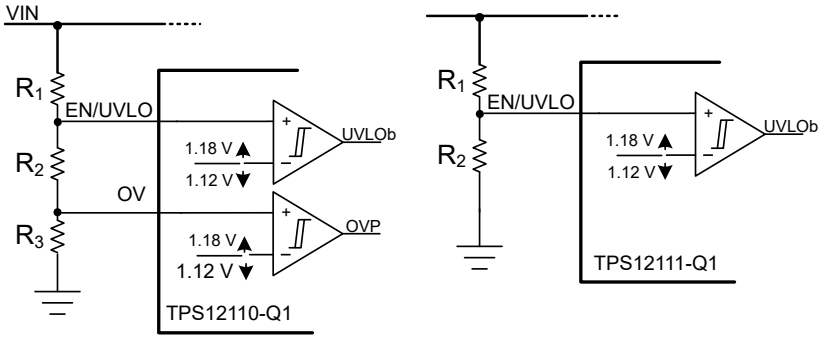

图 8-12. Programming Overvoltage and Undervoltage Protection Threshold

8.3.6 Remote Temperature Sensing and Protection (DIODE)

The device features an integrated remote temperature sensing, protection and dedicated fault output. With a companion BJT, MMBT3904 as a remote temperature sense element, the controller gets the temperature information of the sense point. Connect the DIODE pin of TPS1211-Q1 to the collector, base of a MMBT3904 BJT. After the sensed temperature reaches approximately 155ºC, the device pulls PD low to SRC, turning off the external FET and also asserts $\overline{FLT\_T}$ low. After the temperature reduces to 125ºC (minimum), an internally fixed auto-retry cycle of 512 ms commences. $\overline{FLT\_T}$ de-asserts and the external FET turns ON after the re-try duration of 512 ms is lapsed.

In TPS12111-Q1, after the sensed temperature crosses 155°C, PD and G get pulled low to SRC. After the TSD hysteresis, PU and G stays latched OFF. The latch gets reset by toggling EN/UVLO below $V_{(ENF)}$ or by power cycling Vs below V_{SPORF}.

8.3.7 TPS1211x-Q1 as a Simple Gate Driver

图 8-13 shows application schematics of TPS1211x-Q1 as a simple gate driver in load disconnect switch as well as back-to-back FETs driving topologies. The protection features like two-level overcurrent protection, overvoltage protection, and overtemperature protection are disabled.

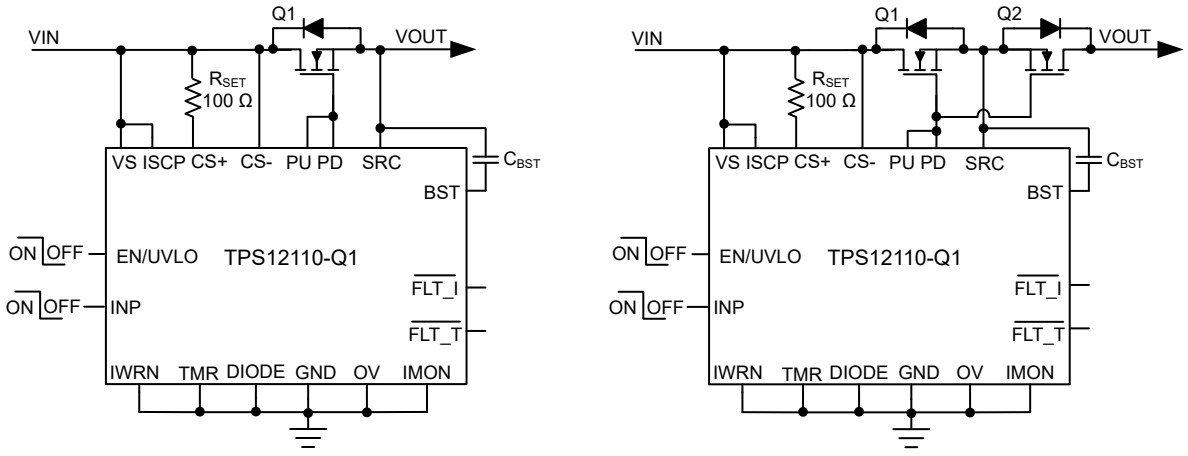

图 8-13. Connection Diagram of TPS12110-Q1 for Simple Gate Driver Design

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8.4 Device Functional Modes

The TPS1211-Q1 has two modes of operation. Active mode and low IQ shutdown mode. If the EN/UVLO pin voltage is greater than the rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers and all the protection and diagnostic features are enabled. If the EN/UVLO voltage is pulled < 0.3 V, the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The external FETs turn OFF. The TPS1211-Q1 consumes low IQ of 1.7 µA (typical) in this mode.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPS1211x-Q1 family is a 45-V smart high-side driver with protection and diagnostics. The TPS1211x-Q1 device controls external N-channel MOSFETs and its drive architecture is suitable to drive back-to-back N-Channel MOSFETs. The strong gate 4-A source and sink capabilities enable switching parallel MOSFETs in high current applications such as circuit breaker in powertrain (DC/DC converter), driving loads in power distribution unit, electric power steering, driving PTC heater loads, and so forth. The TPS1211x-Q1 device provides two-level, adjustable, overcurrent protection with adjustable circuit breaker timer, fast short-circuit protection, accurate analog current monitor output, and remote overtemperature protection.

The variant TPS12111-Q1 features a separate precharge driver (G) with independent control input (INP_G). This feature enables system designs that must precharge the large output capacitance before turning ON the main power path.

The following design procedure can be used to select the supporting component values based on the application requirement.

9.2 Typical Application: Driving Zonal Controller Loads on 12-V Line in Power Distribution Unit

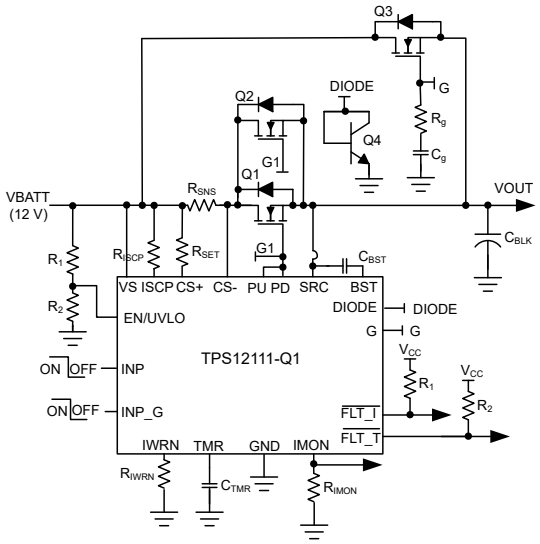

图 9-1. Typical Application Schematic: Driving Zonal Controller Loads with Precharging the Output Capacitance

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9.2.1 Design Requirements

表 9-1 shows the design parameters for this application example.

表 9-1. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{IN}	12 V
Undervoltage lockout set point, VIN_{UVLO}	6.5 V
Maximum load current, I_{OUT}	25 A
Overcurrent protection threshold, I_{OC}	30 A
Short-circuit protection threshold, I_{SC}	35 A
Fault timer period (T_{OC})	1 ms
Fault response	Auto-retry
Load capacitance, C_{OUT}	1 mF
Charging time, T_{start}	10 ms

9.2.2 Detailed Design Procedure

Selection of Current Sense Resistor, R_{SNS}

The recommended range of the overcurrent protection threshold voltage, $V_{(SNS\_WRN)}$, extends from 10 mV to 30 mV. Values near the low threshold of 10 mV can be affected by the system noise. Values near the upper threshold of 30 mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 25 mV is selected as the overcurrent protection threshold voltage. Use the following equation to calculate the current sense resistor, R_{SNS}.

$$R_{SNS} = \frac{V_{(SNS\text{-}WRN)}}{I_{OC}} = \frac{25\ mV}{30\ A} = 833\ \mu\Omega \quad (13)$$

The next smaller available sense resistor 800 μΩ, 1% is chosen.

To improve signal to noise ratio or for better overcurrent protection accuracy, higher overcurrent protection threshold voltage, $V_{(SNS\_WRN)}$ can be selected. The maximum allowed $V_{(SNS\_WRN)}$ voltage is 250 mV.

Selection of Scaling Resistor, R_{SET}

R_{SET} is the resistor connected between VS and CS+ pins. This resistor scales the overcurrent protection threshold voltage and coordinates with R_{IWRN} and R_{IMON} to determine the overcurrent protection threshold and current monitoring output. The recommended range of R_{SET} is 50 Ω – 100 Ω.

R_{SET} is selected as 100 Ω, 1% for this design example.

Programming the Overcurrent Protection Threshold – R_{IWRN} Selection

The R_{IWRN} sets the overcurrent protection threshold, whose value can be calculated using 方程式 14.

$$R_{IWRN}\ (\Omega) = \frac{11.9 \times R_{SET}}{R_{SNS} \times I_{OC}} \quad (14)$$

To set 30 A as overcurrent protection threshold, R_{IWRN} value is calculated to be 49.5 kΩ.

Choose the closest available standard value: 49.9 kΩ, 1%

ADVANCE INFORMATION

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Programming the Short-Circuit Protection Threshold – R_{ISCP} Selection

The R_{ISCP} sets the short-circuit protection threshold. Use the following equation to calculate the value.

$$R_{ISCP}\ (\Omega) = \frac{I_{SC} \times R_{SNS}}{14.5\ \mu} - 600 \quad (15)$$

To set 35 A as overcurrent protection threshold, R_{ISCP} value is calculated to be 1.33 kΩ.

Choose the closest available standard value: 1.43 kΩ, 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between I_{SCP} and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1 nF across I_{SCP} and CS– pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

Programming the Fault timer Period – C_{TMR} Selection

For the design example under discussion, overcurrent transients are allowed for 1-ms duration. This blanking interval, T_{OC} can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. Use the following equation to calculate the value of C_{TMR} to set 1 ms for T_{OC}.

$$C_{TMR} = \frac{T_{OC} \times 77.5\ \mu A}{1.2} = 64.58\ nF \quad (16)$$

Choose closest available standard value: 68 nF, 10%.

Selection of MOSFETs, Q_1 and Q_2

For selecting the MOSFET Q_1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON-resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 35 V as the maximum application voltage, MOSFETs with V_{DS} voltage rating of 40 V is suitable for this application.

The maximum V_{GS} TPS1211-Q1 can drive is 13 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred.

Based on the design requirements, BUK7S0R5-40HJ is selected and its ratings are:

- 40-V $V_{DS(MAX)}$ and 20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 0.47-mΩ typical at 10-V V_{GS}
- MOSFET $Q_{g(total)}$ is 190 nC

Selection of Bootstrap Capacitor, C_{BST}

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 100 µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two parallel BUK7S0R5-40HJ MOSFETs.

ADVANCE INFORMATION

$$C_{BST} = \frac{Q_{g(total)}}{1\ V} = 380\ nF \quad (17)$$

Choose closest available standard value: 470 nF, 10 %.

Setting the Undervoltage Lockout

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider network of R_1 and R_2 connected between VS, EN/UVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving 方程式 18.

$$V_{(UVLOR)} = \frac{R_2}{(R_1 + R_2)} \times VIN_{UVLO} \quad (18)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R_1 and R_2. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I(R_{12})$ must be chosen to be 20 times greater than the leakage current of UVLO pin.

From the device electrical specifications, $V_{(UVLOR)}$ = 1.18 V. From the design requirements, VIN_{UVLO} is 6.5 V. To solve the equation, first choose the value of R_1 = 470 kΩ and use 方程式 18 to solve for R_2 = 104.24 kΩ. Choose the closest standard 1% resistor values: R_1 = 470 kΩ, and R_2 = 105 kΩ.

Selection of Precharge Path Components, C_g and R_g

For charging the large capacitors on output, the output slew rate can be controlled by using a capacitor on the gate (G) of the precharge FET Q3. The target inrush current to charge 1 mF of output capacitance to 12-V in 10 ms can be estimated by 方程式 19. The required gate capacitance Cg to limit the inrush current to 1.2 A can be calculated by using 方程式 16, where I_g = 100 µA (typical) is the gate charging current of pin 'G'. By solving 方程式 20, we get C_g as 83.33 nF.

Choose the closest available standard value: 82 nF, 10%.

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{T_{start}} = 1.2\ A \quad (19)$$

$$I_g = C_g \times \frac{I_{INRUSH}}{C_{OUT}} \quad (20)$$

A series resistor R_g must be used in conjunction with C_g to limit the discharge current from C_g during turn-off and to stabilize the gate 'G' during slew rate control. The recommended value for R_g is between 220 Ω to 470 Ω.

Choosing the Current Monitoring Resistor, R_{IMON}

Voltage at IMON pin V_{IMON} is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The R_{IMON} must be selected based on the maximum load current and the input voltage range of the ADC used. R_{IMON} is set using 方程式 21.

$$V_{IMON} = (V_{SNS} + V_{OS\_SET}) \times \frac{0.9 \times R_{IMON}}{R_{SET}} \quad (21)$$

Where $V_{SNS} = I_{OC} \times R_{SNS}$ and V_{OS_SET} is the input referred offset (± 350 µV) of the current sense amplifier.

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The maximum voltage range for monitoring the current (V(IMONmax)) is limited to minimum([V(VS) – 0.5V], 5.5V) to ensure linear output. This puts a limitation on the maximum value of R_{IMON} resistor. The IMON pin has an internal clamp of 6.5 V (typical).

For I_{OC} = 30 A and considering the operating range of ADC to be 0 V to 3.3 V (for example, V_{IMON} = 3.3 V), R_{IMON} can be calculated as

$$R_{IMON} = \frac{V_{IMON} \times R_{SET}}{(V_{SNS} + V_{OS\_SET}) \times 0.9} = 16.52\ k\Omega \quad (22)$$

Selecting R_{IMON} value less than shown in 方程式 22 ensures that ADC limits are not exceeded for maximum value of load current. Choose the closest available standard value: 16.5 kΩ, 1%.

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9.2.3 Application Curves

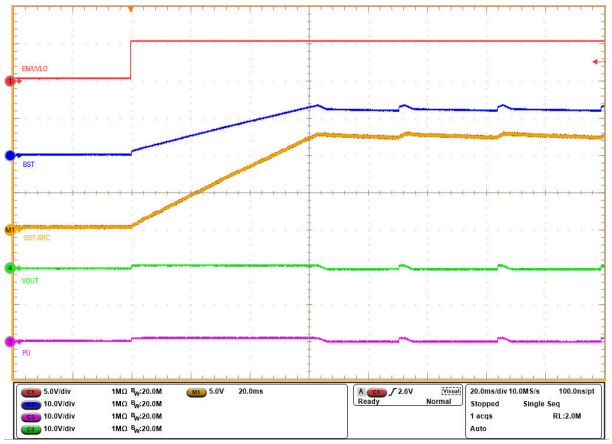


图 9-2. Start-Up Profile of Bootstrap Voltage for INP = GND

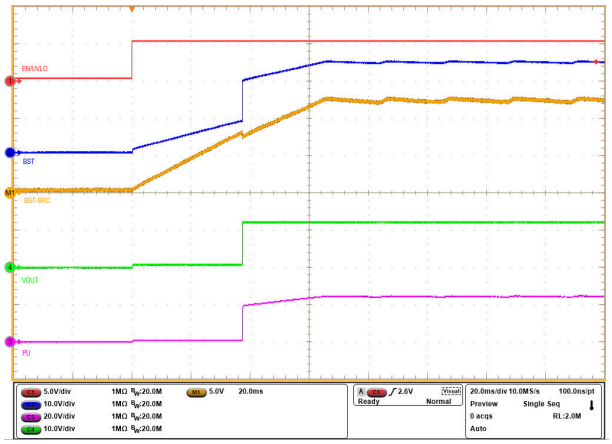


图 9-3. Start-Up Profile of Bootstrap Voltage for INP = HIGH

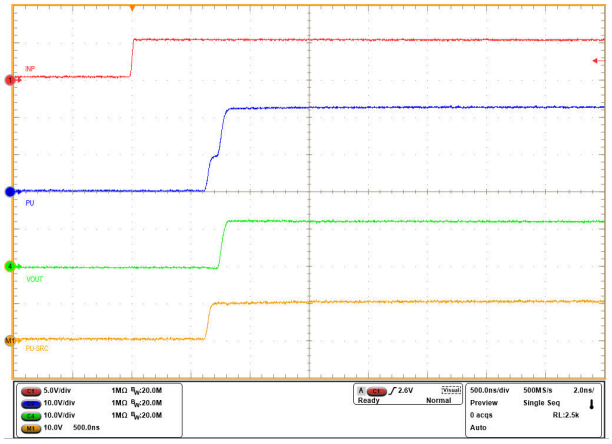


图 9-4. Turn-ON Response of TPS12111-Q1 for INP -> LOW to HIGH

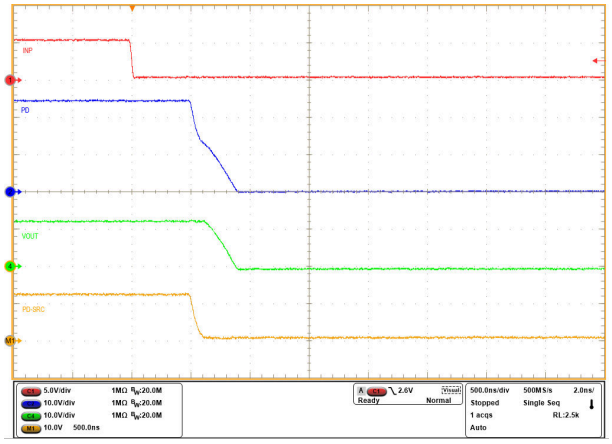


图 9-5. Turn-OFF Response of TPS12111-Q1 for INP -> HIGH to LOW

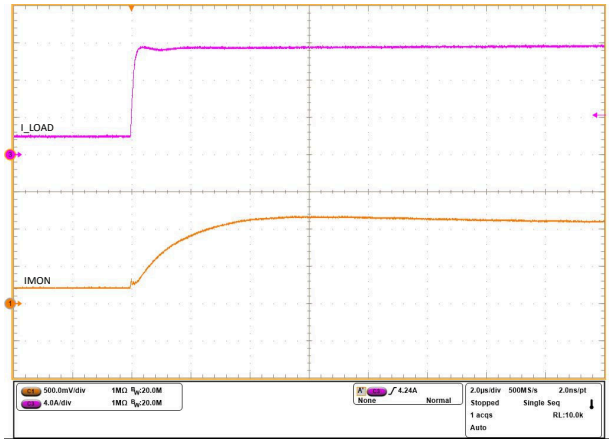


图 9-6. IMON Response During 12-A Load Step

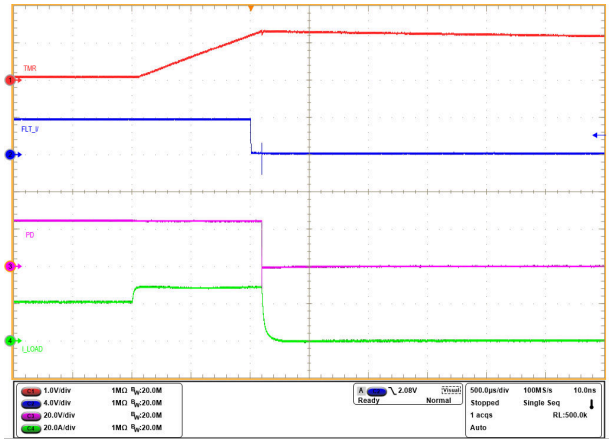


图 9-7. Overcurrent Response of TPS12111-Q1 for a Load Step from 20 A to 32 A with 30-A Overcurrent Protection Setting

ADVANCE INFORMATION

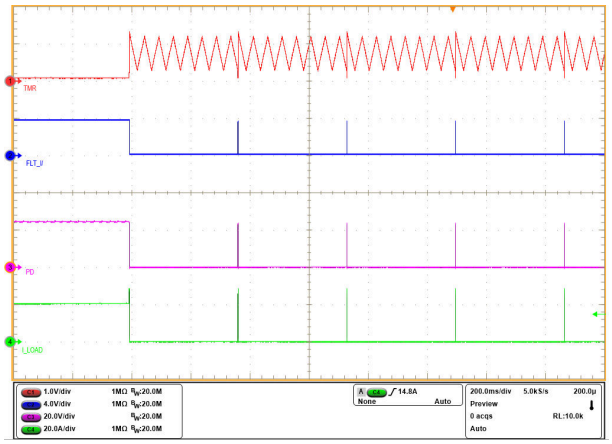


图 9-8. Auto-Retry Response of TPS12111-Q1 for an Overcurrent Fault

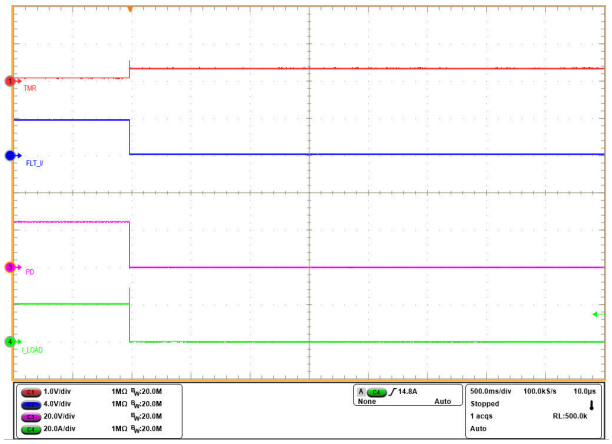


图 9-9. Latch-Off Response of TPS12111-Q1 for an Overcurrent Fault

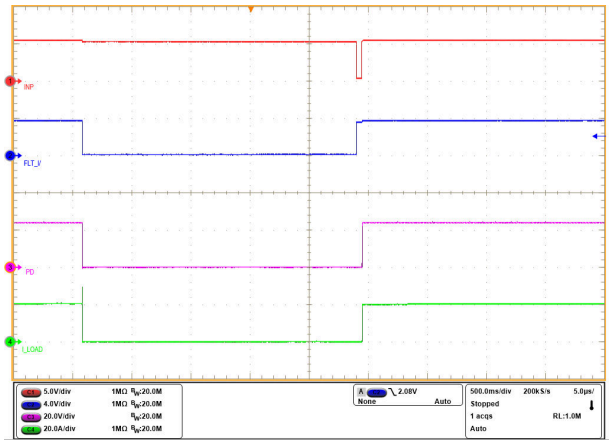


图 9-10. Response During Coming out of Overload Fault with INP Reset

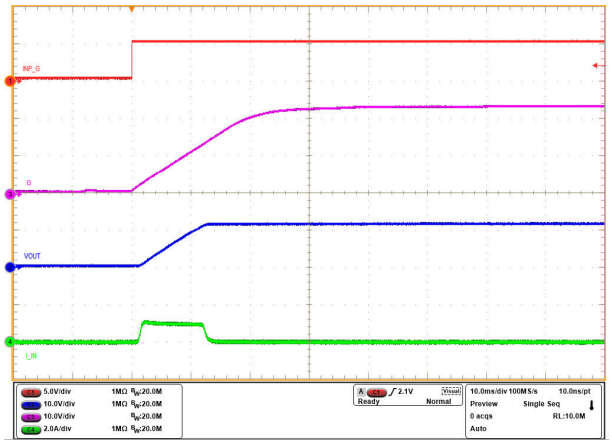


图 9-11. Precharge Profile of the Output Capacitance (VIN = 12 V, C_{OUT} = 1 mF, No Load)

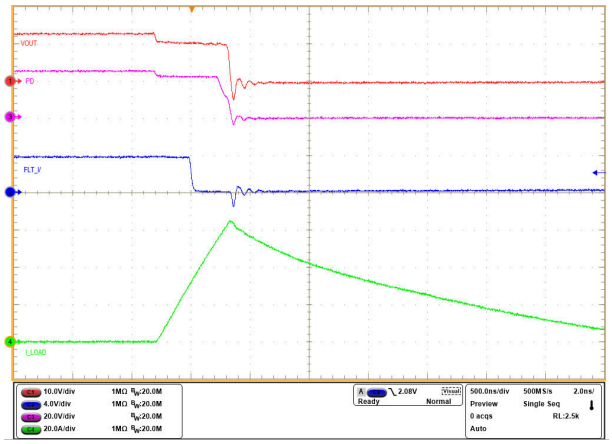


图 9-12. Output Hot-Short Response of the TPS12111-Q1 Device

9.3 Typical Application: Reverse Polarity Protection with TPS12110-Q1

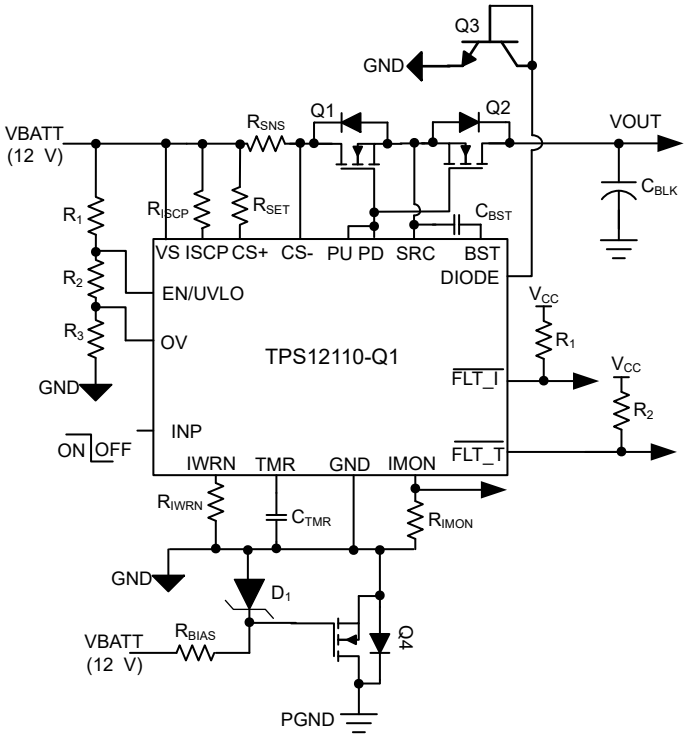


图 9-13. Typical Application Schematic: TPS12110-Q1 High-Side Driver with Input Reverse Polarity Protection

For applications such as powering electronic power steering (EPS) system, the input must be protected from any possible reverse polarity scenarios. The TPS12110-Q1 configured as shown in 图 9-13 meets the system requirements. The back-to-back FET (Q_1 and Q_2) configuration blocks reverse current flow and provides protection for the load against static input reverse polarity event. The N-MOSFET (Q_4) in the ground path protects the TPS12110-Q1 controller, and Zener diode D_1 is added for V_{GS} protection of Q_4.

9.3.1 Design Requirements

表 9-2 shows the design parameters for this application example.

表 9-2. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{IN}	12 V
Undervoltage lockout set point, VIN_{UVLO}	6.5 V
OV set point, VIN_{OVP}	36 V
Maximum load current, I_{OUT}	20 A
Overcurrent protection threshold, I_{OC}	24 A
Short-circuit protection threshold, I_{SC}	30 A
Fault timer period (T_{OC})	1 ms
Fault response	Auto-retry
Input reverse polarity protection	Yes

ADVANCE INFORMATION

9.3.2 External Component Selection

By following similar design procedure as outlined in *Detailed Design Procedure*, the external component values are calculated as below:

- R_{SNS} = 1 mΩ.
- R_{SET} = 100 Ω.
- R_{IWRN} = 49.9 kΩ to set 24 A as overcurrent protection threshold.
- R_{ISCP} = 1.468 kΩ to set 30 A as short-circuit protection threshold.
- C_{TMR} = 68 nF to set 1-ms over current protection time.
- R_1 , R_2 and R_3 are selected as 390 kΩ, 71.5 kΩ and 15.8 kΩ respectively to set VIN undervoltage lockout threshold at 6.5 V and overvoltage cutoff threshold at 36 V.
- R_{IMON} = 15 kΩ to limit maximum $V_{(IMON)}$ voltage to 3.3 V at full-load current of 24 A.
- To reduce conduction losses, BUK7S0R5-40HJ MOSFET is selected. Two FETs are used in back-to-back configuration for reverse current blocking.
  - 40-V $V_{DS(MAX)}$ and 20-V $V_{GS(MAX)}$.
  - $R_{DS(ON)}$ is 0.47-mΩ typical at 10-V V_{GS}.
  - Q_g of each MOSFET is 190 nC.
- C_{BST} = (2 × Q_g) / 1 V = 380 nF; Choose the closest available standard value: 470 nF, 10 %.
- Q_4 selection: Any signal N-MOSFET with 40-V V_{DS} support is sufficient. DMN601WKQ-7 is selected for the current design and a 12-V Zener diode SZMM3Z12VST1G is used for V_{GS} protection.

9.3.3 Application Curves

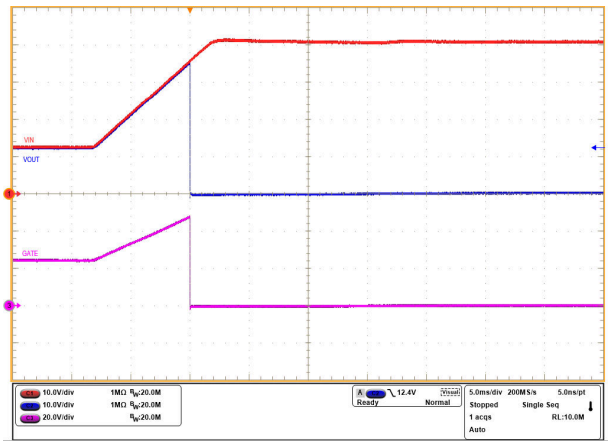


图 9-14. Overvoltage Cutoff Response of TPS12110-Q1 at 36-V Level

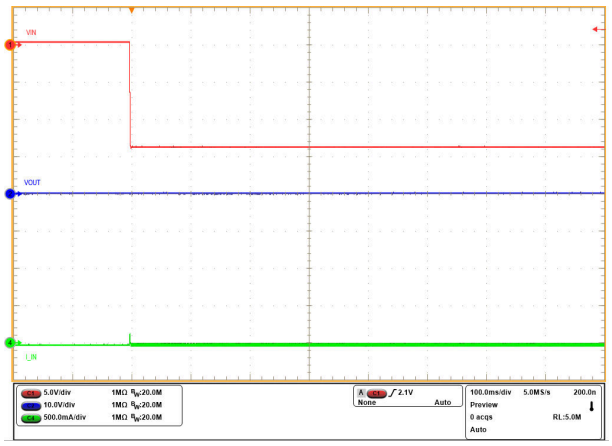


图 9-15. Input Reverse Polarity Protection with TPS12110-Q1

9.4 Power Supply Recommendations

When the external MOSFETs turn OFF during the conditions such as INP control, overvoltage cutoff, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS1211-Q1 gets powered from the Vs pin. Voltage at this pin must be maintained above $V_{(S\_POR)}$ level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place

a R_{VS}-C_{VS} filter between the input supply line and Vs pin to filter out the supply noise. TI recommends R_{VS} value around 100 Ω.

The following figure shows the circuit implementation with optional protection components.

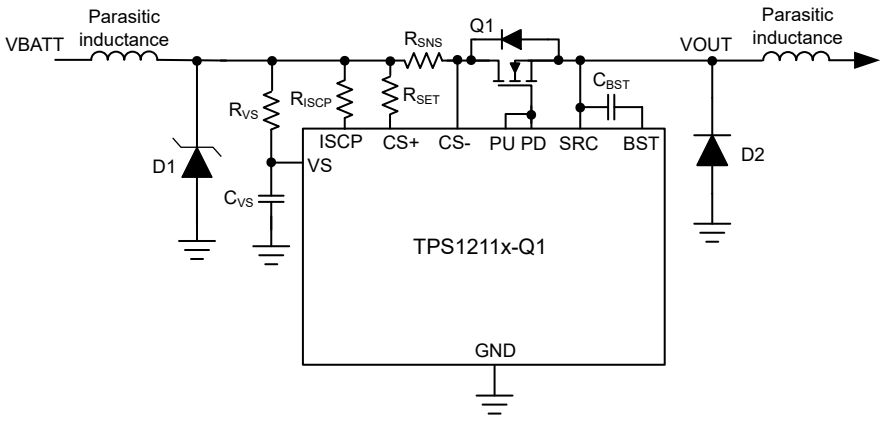


图 9-16. Circuit Implementation with Optional Protection Components for TPS1211-Q1

9.5 Layout

9.5.1 Layout Guidelines

- The sense resistor (R_{SNS}) must be placed close to the TPS1211x-Q1 and then connect R_{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.
- For all the applications, TI recommends a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- The high-current path from the board input to the load, and the return path, must be parallel and close to each other to minimize loop inductance.
- The external MOSFETs must be placed close to the controller such that the GATE of the MOSFETs are close to PU/PD pins to form short GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- The external boot-strap capacitor must be placed close to BST and SRC pins to form very short loop.
- The ground connections for the various components around the TPS1211x-Q1 must be connected directly to each other, and to the TPS1211x-Q1 GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- The DIODE pin sources current to measure the temperature. TI recommends BJT MMBT3904 to use as a remote temperature sense element. Take care in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. In addition, TI recommends to make a Kelvin connection from the emitter of the MMBT3904 to the GND of the part to ensure an accurate measurement. Additionally, a small 1000=pF bypass capacitor must be placed in parallel with the MMBT3904 to reduce the effects of noise.

ADVANCE INFORMATION

ADVANCE INFORMATION

9.5.2 Layout Example

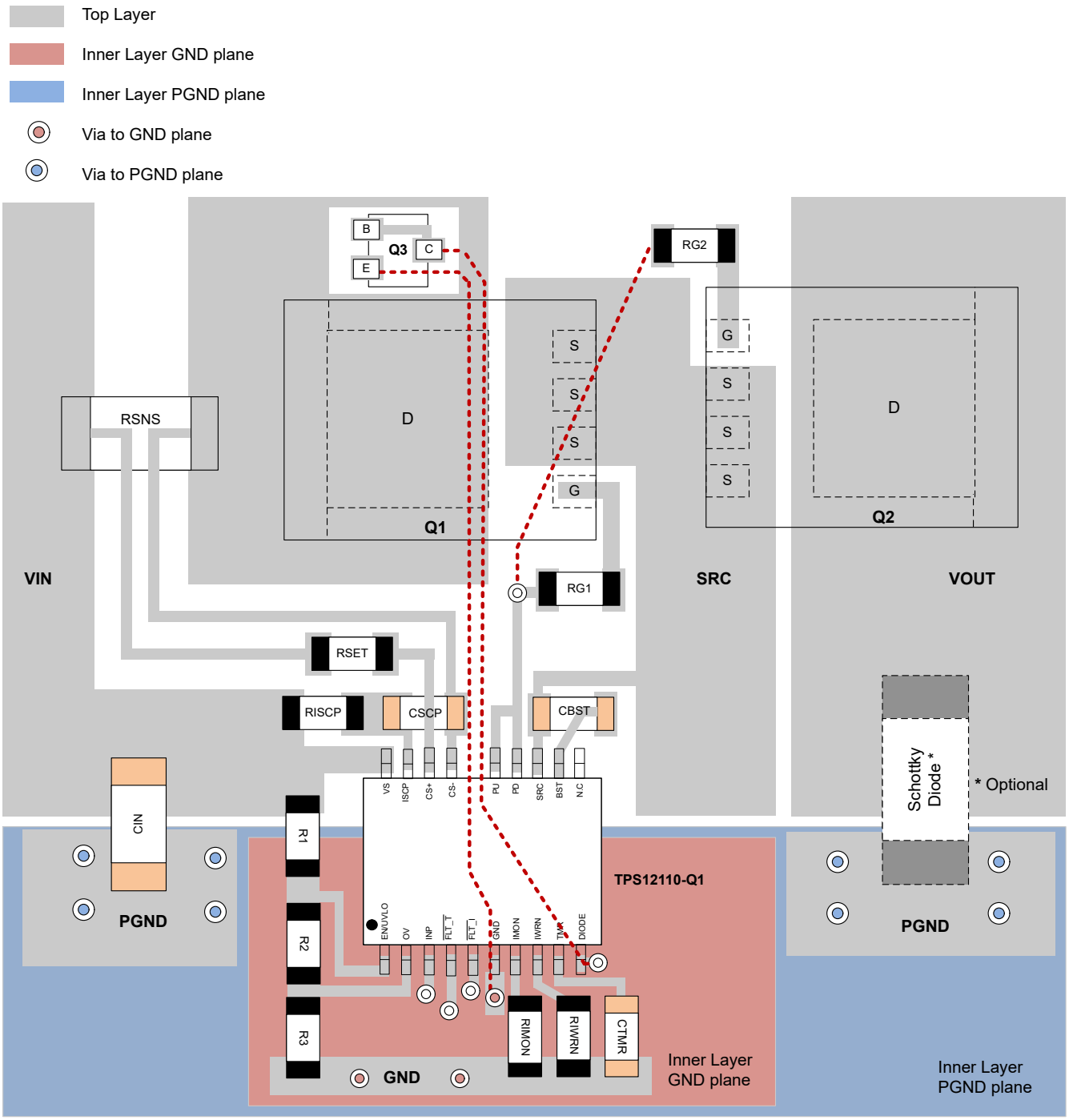


图 9-17. Typical PCB Layout Example for TPS12110-Q1 with B2B MOSFETs

10 Device and Documentation Support

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

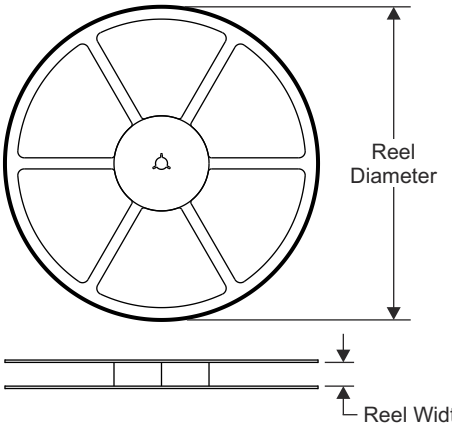
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

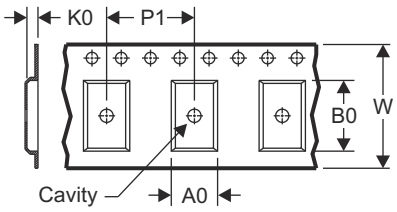
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

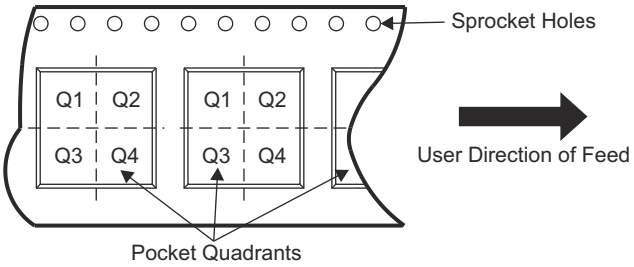


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

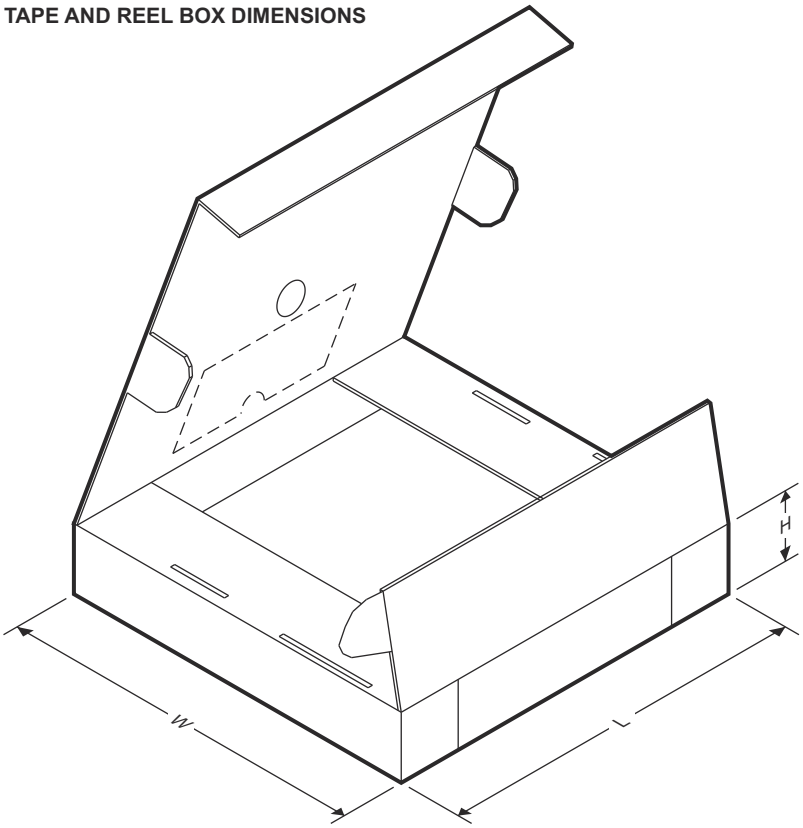
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS12110AQDGXRQ1	VSSOP	DGX	19	5000	330	16.0	5.4	5.4	1.45	8	12	Q1
PTPS12111LQDGXRQ1	VSSOP	DGX	19	5000	330	16.0	5.4	5.4	1.45	8	12	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS12110AQDGXRQ1	VSSOP	DGX	19	5000	853.0	449.0	35
PTPS12111LQDGXRQ1	VSSOP	DGX	19	5000	853.0	449.0	35

ADVANCE INFORMATION

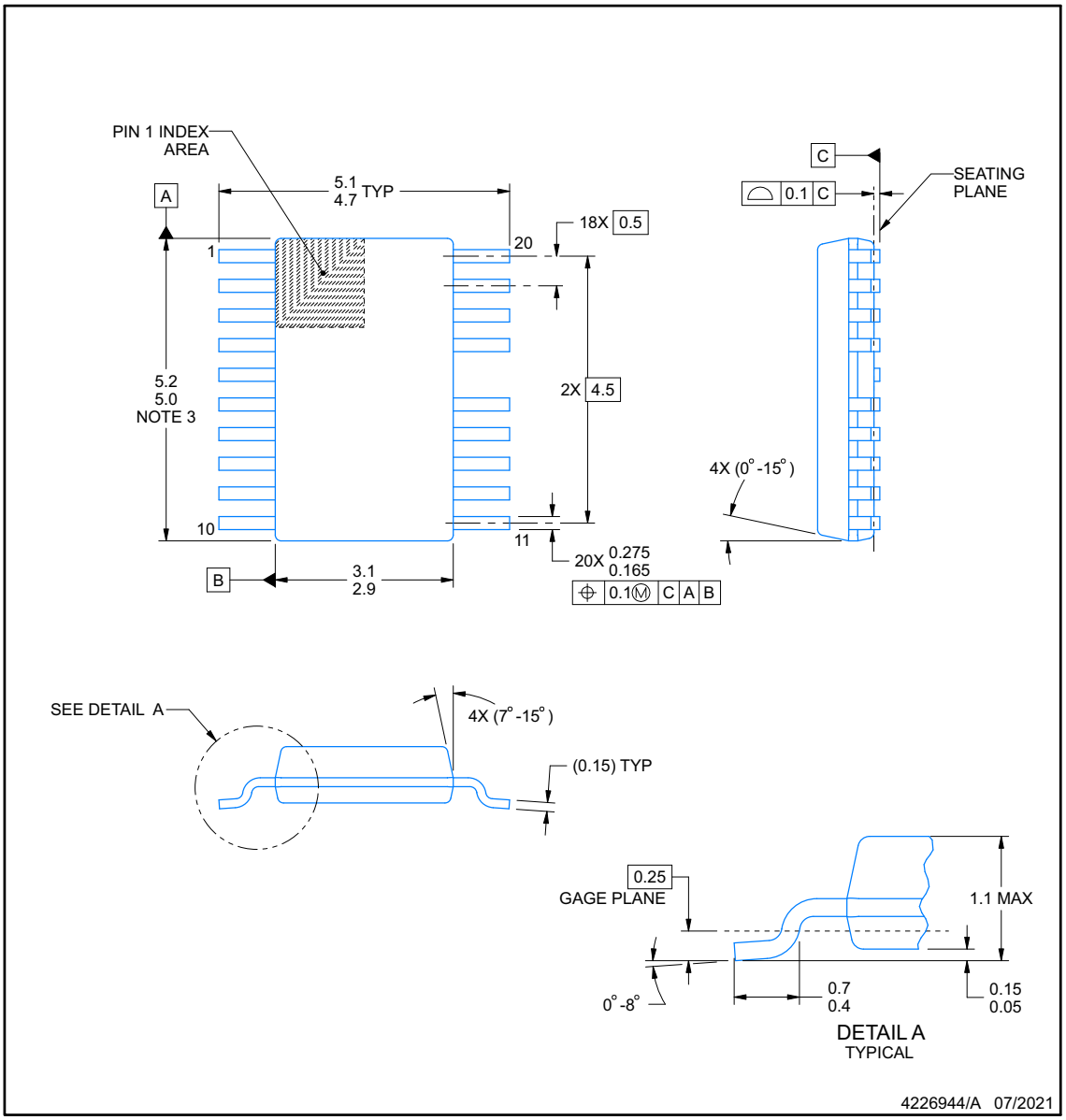
ADVANCE INFORMATION

PACKAGE OUTLINE

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

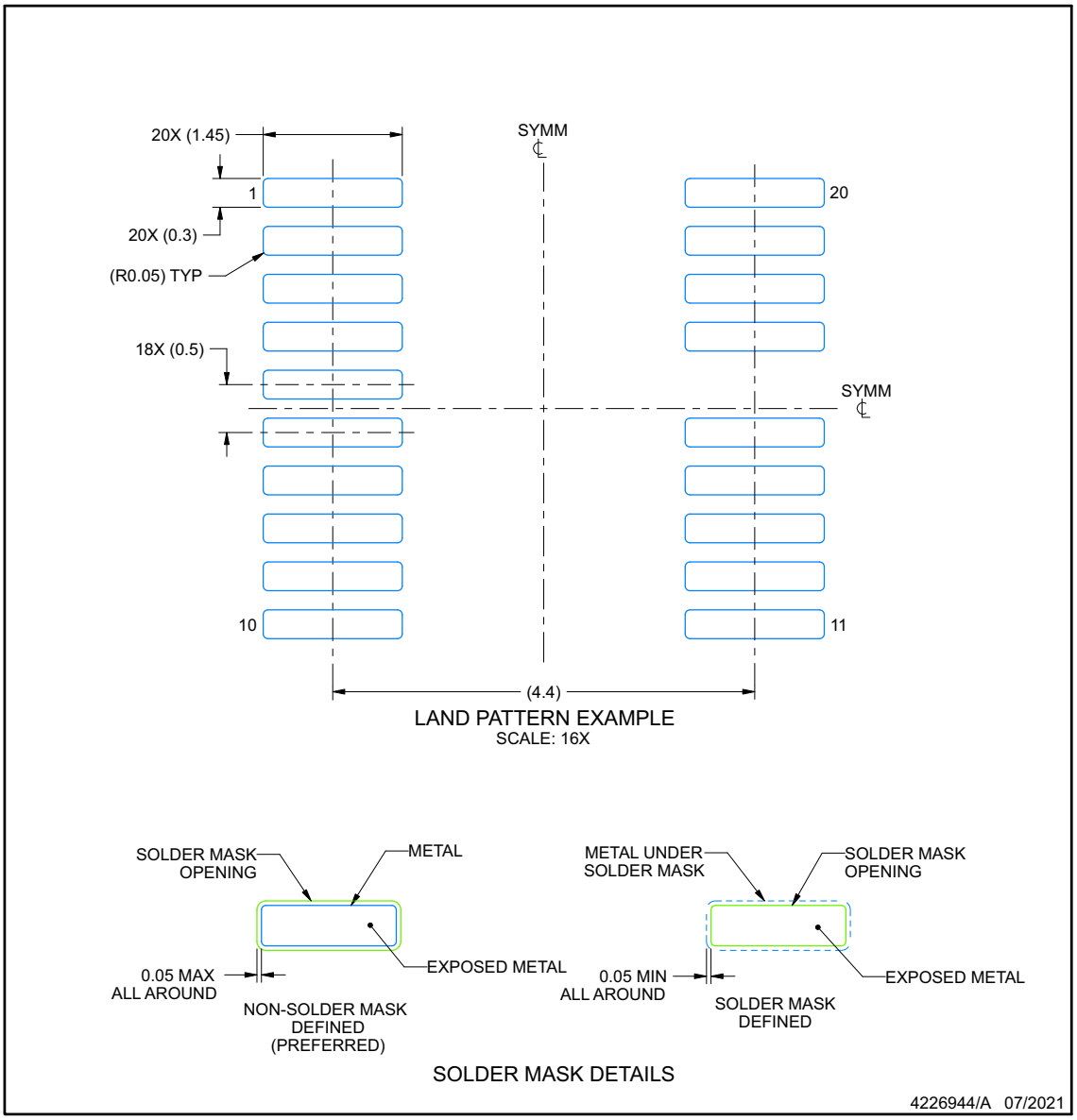
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

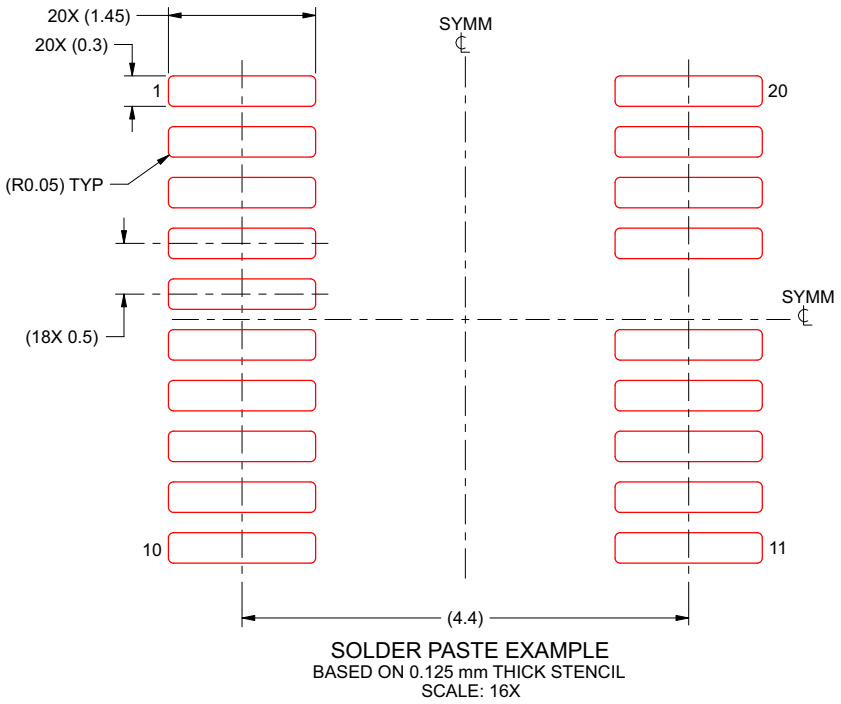
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226944/A 07/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS12110AQDGXRQ1	ACTIVE	VSSOP	DGX	19	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2ZAS	Samples
TPS12111LQDGXRQ1	ACTIVE	VSSOP	DGX	19	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2Z9S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

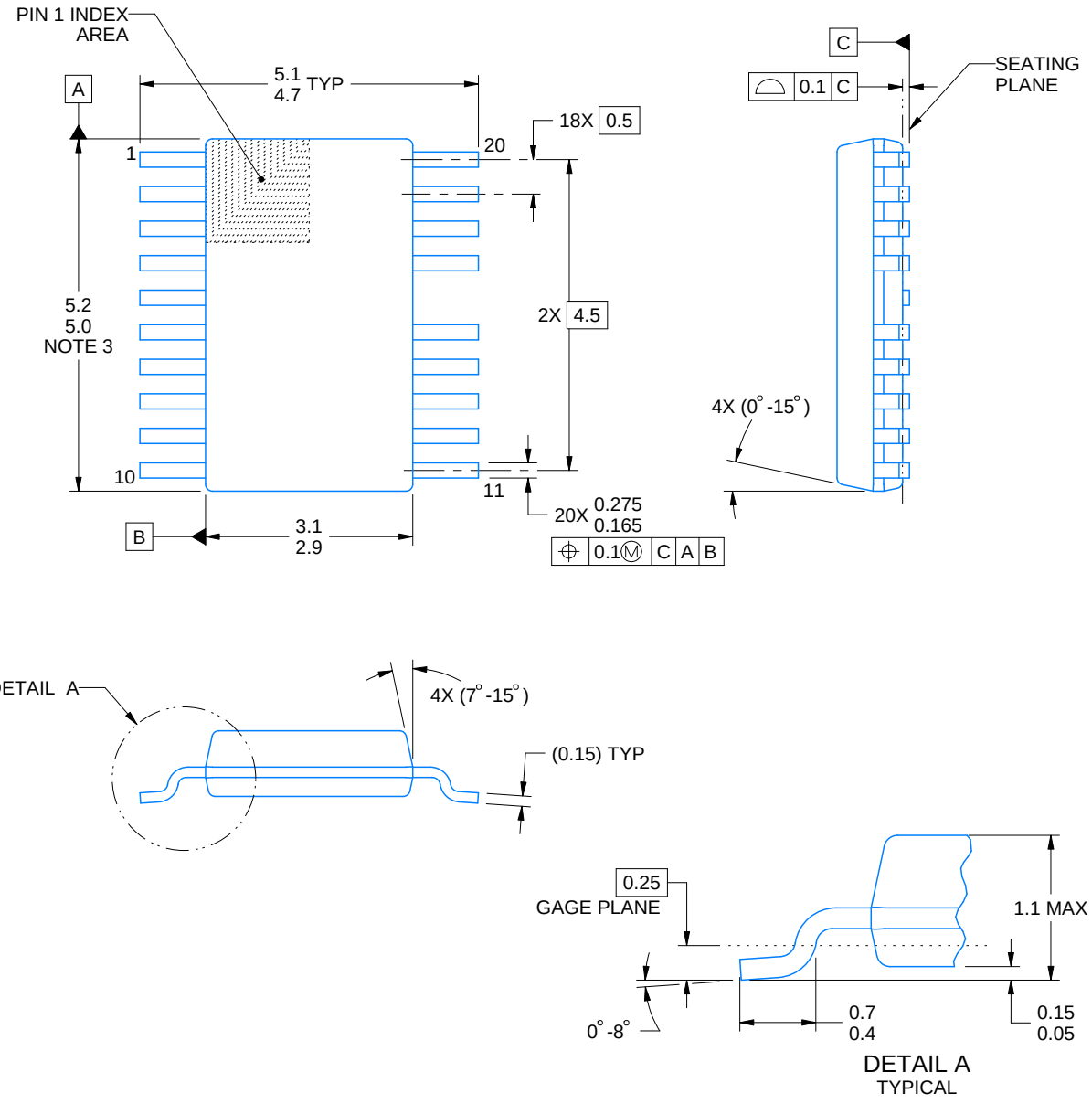
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DGX0019A

VSSOP - 1.1 mm max height

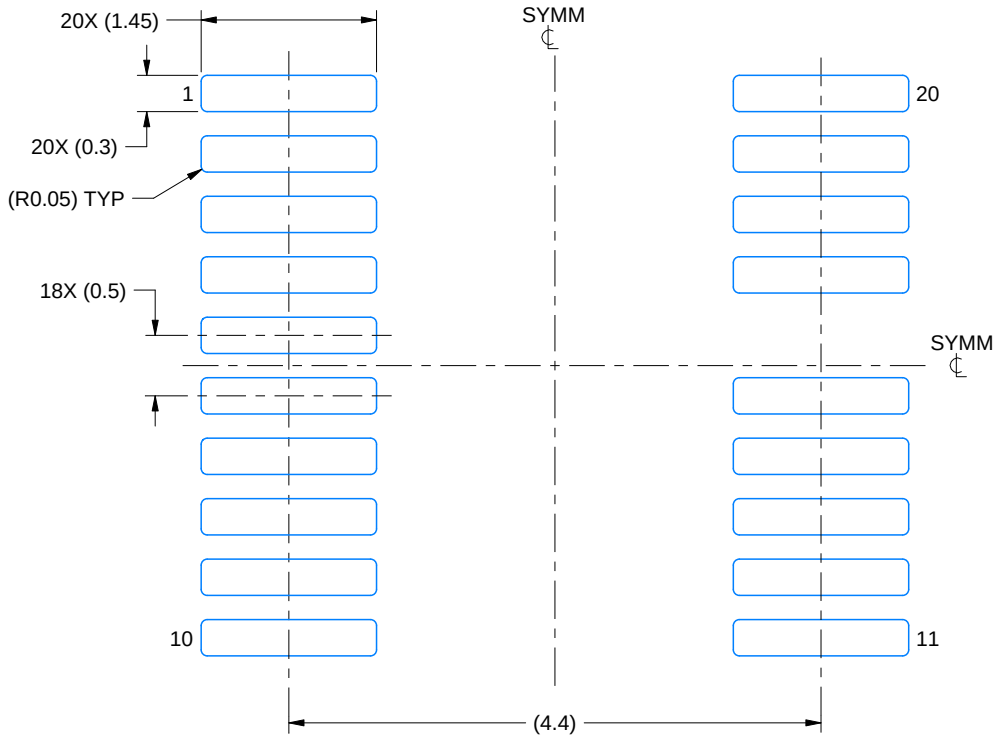
SMALL OUTLINE PACKAGE



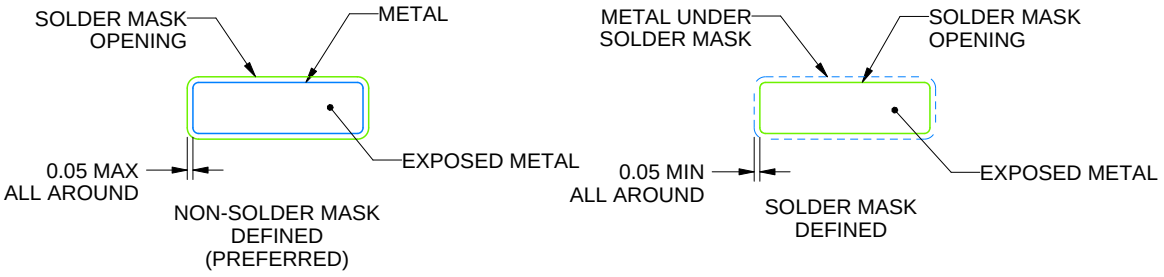
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

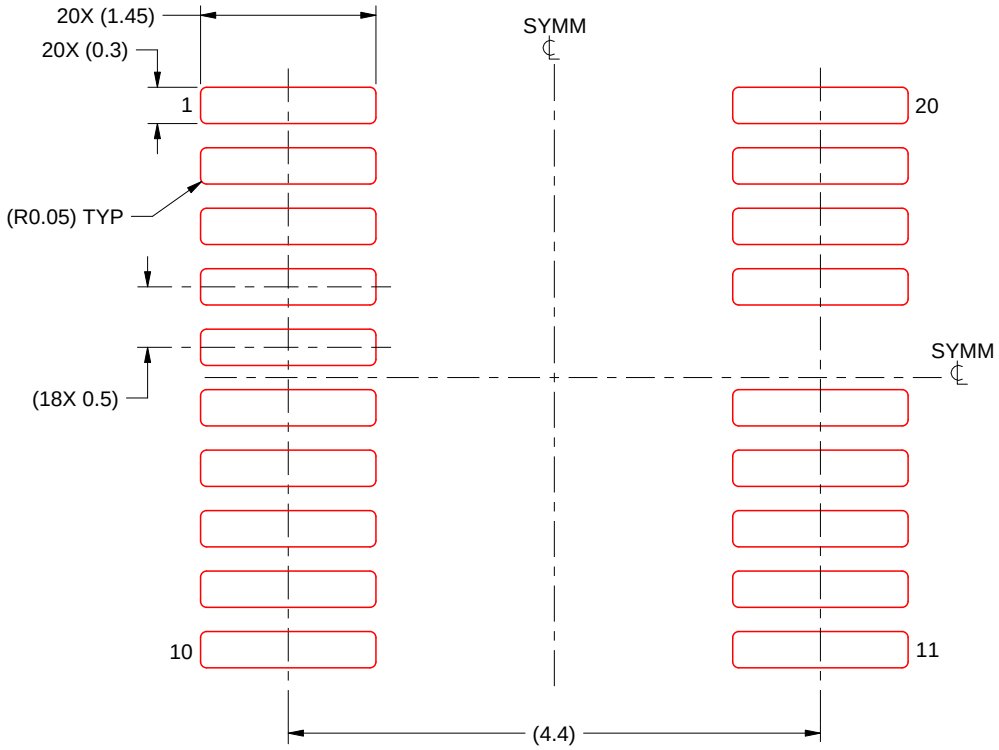


SOLDER MASK DETAILS

4226944/A 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226944/A 07/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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